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A transformer based 60 GHz CMOS LNA for mm-wave applications

Rajendra Chikkanagouda[1], Cyril Prasanna Raj P[2]

[1]*Research Scholar, Department of Electronics and Communication Engineering, M. S. Engineering College, Bengaluru, India.*
[2]*Senior Member, IEEE, Research and Development Centre, M. S. Engineering College, Bengaluru, India.*

Correspondence Author: Rajendra Chikkanagouda, Research Scholar, Department of Electronics and Communication Engineering, M. S. Engineering College, Bengaluru, India.
E-mail:- rajendracg@gmail.com

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Abstract

Applications in the range of 60 GHz are emerging during the last years especially in the field of millimeter-wave (mm-wave) systems for short-range wireless links. It requires low noise receiver, which needs to use high performances for reliable mm-wave technology. A CMOS Low Noise Amplifier (LNA) has been designed in 65 nm for mm-wave applications at (57-64) GHz using the technique of the transformer based cascode topology. This architecture achieves gain enhancement and input matching in cascode amplifier. The proposed method enables us to acknowledge impedance matching by exploiting a transformer. The designed LNA exhibits - 23.5 dB input matching and 4.9 dB Noise Figure (NF) at 60 GHz. Biased under 1.2V, this two-stage LNA reaches a peak gain of 26.15 dB at 54 GHz, 23.16 dB at 60 GHz and 20 dB from (57-64) GHz and S_{11} is less than -15 dB in the frequency range of (57-64) GHz. The power consumption of the device is 18 mW. These performances are among the best reported up to now for 60 GHz transformer based LNA.

Key words: 65 nm, CMOS, LNA, mm-wave, 60 GHz, Transformer Feedback.

INTRODUCTION

Recently, the expanding interest in unlicensed band of 60 GHz for wireless communications has led to the development of RFICs operating up to the range of millimeter wave. High data rate wireless systems such as WPANs and point-to-point links can be implemented due to the availability of large bandwidth.

In spite of the fact that millimeter-wave (mm-wave) radio frontend ICs have customarily been the space of III-V compound semiconductors, for example, GaAs and InP, the most recent advances in silicon innovation enable us to manage the realization of CMOS building blocks and systems (Floyd, B.A., et al., 2005 and Huang, C. Y., et al 2018). The CMOS is preferred for its robustness and low cost. IF and baseband circuitry can be easily implemented and integrated in CMOS technology (Lee, T. H., 1998).

This paper discusses on a transformer based two-stage cascode LNA topology with good input matching and improved gain performance in mm-wave applications. Besides it demonstrates the empowering of lumped component design approach in the 60 GHz range extend consequently preparing to bring down silicon region circuits. The paper is organized as follows. The proposed input matching technique, namely transformer feedback is explained in Section II. Section III gives the brief description of the design methodology adopted for 60 GHz LNA. Simulation results are discussed in Section IV and the conclusion is given in Section V.

LOW NOISE AMPLIFIER DESIGN

The cascode LNA topology with transformer feedback is as shown in Fig. 1 offers simultaneously input matching and noise impedances of the first stage of the LNA (typically 50 Ohms). This topology fits an algorithmic structure strategy (S. P. Voinigescu et al., 1996) even at mm-waves (Yao, T., et al., 2006, Nicolson, S. T., et al., 2006, Gordon, M., et al., 2004). The impedance matching for noise performance is accomplished by input stage transistor's dimensions (Yao, T., et al., 2006).

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Neglecting the impact of gate-drain capacitance (C_{gd}), R_{in} is the real part of input matching and X_{in} is the imaginary part of input matching respectively, shown in equations (1) and (2).

$$R_{in} = \frac{g_m}{C_{gs}}(L_S + M) \quad (1)$$

$$X_{in} = \omega\left(L_g + L_s + 2M\right) - \frac{1}{\omega C_{gs}} \quad (2)$$

Where C_{gs} is the gate to source capacitance, the transconductance is g_m and coupling coefficient between inductors L_g and L_s is k, which lies between -1 to +1. To provide impedance matching the real part R_{in} must be equal to 50 Ohms and imaginary part must be equal to zero Ohms respectively. The transformer must be designed, represented by its mutual inductance M defined in equations (1) and (2) to fulfil these requirements. Common Source (CS) and cascode topologies without feedback i.e., with $L_S = 0$ as well as Common Gate (CG) topology, cannot achieve simultaneous noise and impedance matching, except by accident, at a single frequency. The LNA exploits the mutual coupling between the spirals of an integrated transformer. The primary side is connected between the gate of the transistor and input of the CS stage, whereas the secondary side is connected to the source of the same transistor. In order to explain the working principle of the proposed method, we considered the small-signal equivalent model of the LNA as shown in Fig. 2 and Fig. 3. The input impedance of the amplifier (Z_{IN}) results equal to

$$Z_{IN}(\omega) = j\omega L_g + \frac{1}{j\omega C_{GS}} + \frac{Mg_m}{C_{GS}} \quad (3)$$

Where M is the mutual coupling of the spirals L_g and L_s ($M = k\sqrt{L_g L_s}$), where k is the coupling coefficient between the spirals.

LNA DESIGN

A two-stage cascode LNA has been designed in 65 nm CMOS by Predictive Technology Model (PTM). The cascode topology reduces the C_{gd} effects, thus by improving the reverse isolation and gain performance. Two stage LNA consists of four transistors and first stage is for simultaneous noise and input matching and second stage is for gain improvement. The schematic is as shown in Fig. 1. The DC-blocking capacitor C_C is inserted between these two stages. Series inductors L_{M1} and L_{M2} are placed between CS and CG circuit. The two stages of the LNA enable us to obtain a gain more than 15 dB.

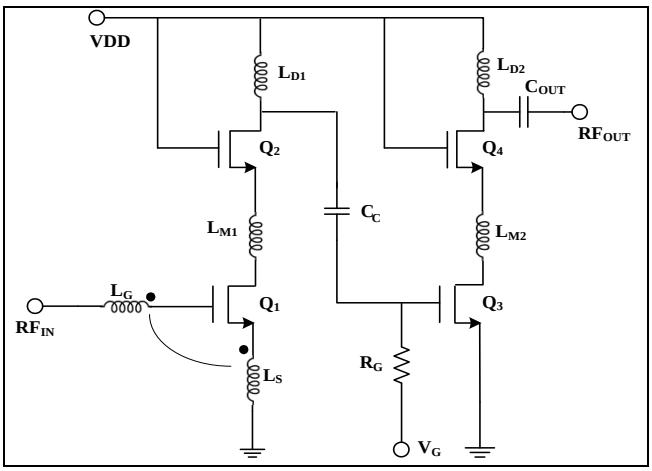

Fig. 1: Circuit schematic of the proposed LNA

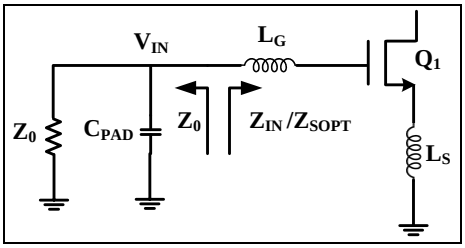

Fig. 2: The equivalent model of Fig. 1 used to calculate Z_{IN}.

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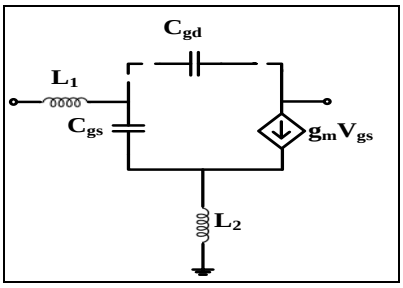

Fig. 3: Small signal circuit for the input transistor (Q_1) (Raffaele, R. S., 2009)

The design of LNA based on transformer feedback technique (Domenico Pepe et al. 2015 and Wen Cheng Lai et al. 2016) has been carried out by the following steps.

1. Select optimum bias current (J_{opt}) for minimum noise figure (NF_{min}) and higher gain.
2. Select the transistor finger widths, there is a trade-off between the maximum available gain and the layout.
3. Select the number of fingers, as there is a trade-off between low P_{DC} and input resistance for noise. This input resistance is close to 50 Ohms.
4. Choose the second stage optimum load inductor and capacitor. These values provide the output complex conjugate impedance matching to a Z_L of 50 Ohms.
5. Choose appropriate values of L_{D1} and C_C of first stage. These values should support interstage matching between two stages.

The optimum values of coupling coefficient (k) and inductor (L_s) have selected by considering the feasibility of the transformer. The widths (W) of all transistors are considered 12 µm. The proposed circuit component sizing is listed in Table 1.

Table 1: Component-Sizing summary

Component	Values
Q_{1-4} (µm)	12
L_{D1} (pH)	205
L_{D2} (pH)	215
L_{M1} (pH)	255
L_{M2} (pH)	215
L_S (pH)	10
L_G (pH)	170
C_{OUT} (fF)	225
C_C (fF)	50
R_G (kΩ)	10
k	0.35

RESULTS DISCUSSION

The proposed LNA is simulated in Advanced Design System (ADS) environment. Predictive Technology Model (PTM) 65 nm is imported into ADS and transistor geometries are identified. The simulation results of the proposed LNA design are presented with a brief description of gain, NF, reverse isolation and input/output reflection coefficients.

The LNA was biased in the condition of V_{DD} = 1.2 V, V_G = 0.65 V. The Fig. 4 shows the simulated S-parameter results of the amplifier. The designed amplifier has a peak gain of 26.15 dB at 54 GHz and next peak gain of 23.16 dB at 60 GHz with a 3 dB bandwidth of (54-64) GHz is 20 dB. The NF is less than 5.5 dB over the frequency range of (50-70) GHz.

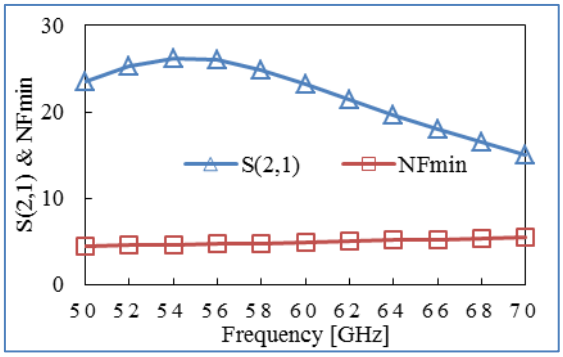

Fig. 4: Gain and NF of the proposed LNA

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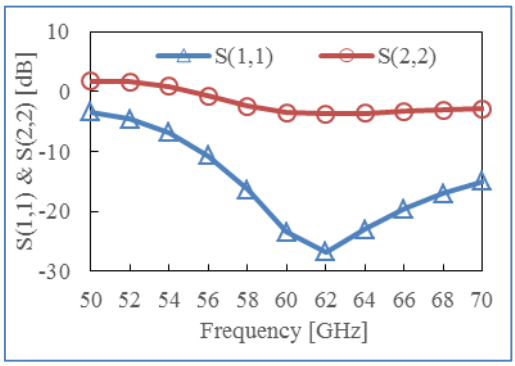

Fig. 5: S_{11} and S_{22} of the proposed LNA

Fig.5 shows the reflection coefficients, S_{11} and S_{22} of the proposed LNA. The LNA achieves minimum S_{11} of -26.79 dB at 62 GHz, and S_{11} less than -15 dB over the frequency range of (57-70) GHz. The output reflection coefficient S_{22} is -3.5 dB at 60 GHz.

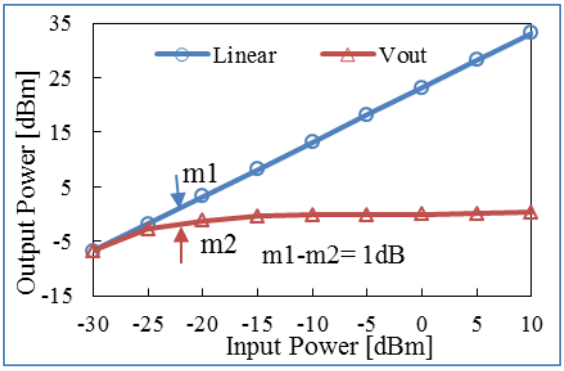

Fig. 6: P1dB of the proposed LNA

The 1-dB compression point of the proposed LNA is as shown in Fig. 6. The linear and output power meet at -22 dB. Further increase of input power, the gain starts to saturate from -22 dB onwards. The 1-dB compression point of the LNA is -22 dB. The Third Order Intercept Point (TOI or IIP3) of the proposed cascode LNA is as shown in Fig. 7. At high frequencies, more number of harmonics are generated and out of these harmonics, the third order is more harmful and close to the fundamental frequency. The third order tone and fundamental tone meet at -15 dBm. IIP3 of the proposed LNA is -15 dB.

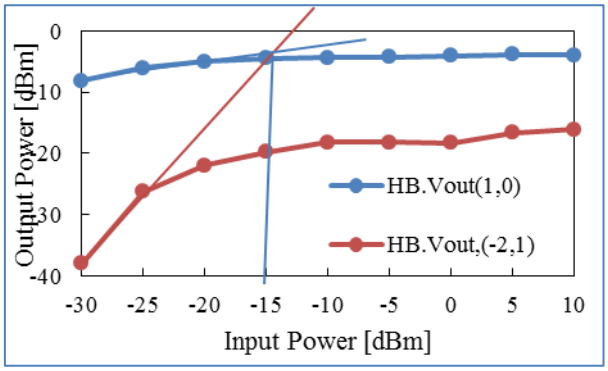

Fig. 7: IIP3 of the proposed LNA

$$K = \frac{1+|\Delta|^2+|S_{11}|^2-|S_{12}|^2}{2|S_{12}||S_{21}|} > 1 \quad (4)$$

From the results presented in Fig. 8 for LNA design, analyzing stability factor K is found to be greater than 1 as defined in equation (4) (Chikkanagouda R., and Cyril Prasanna Raj P. 2019). The designed LNA is unconditionally stable for the frequency range of 57 GHz onwards.

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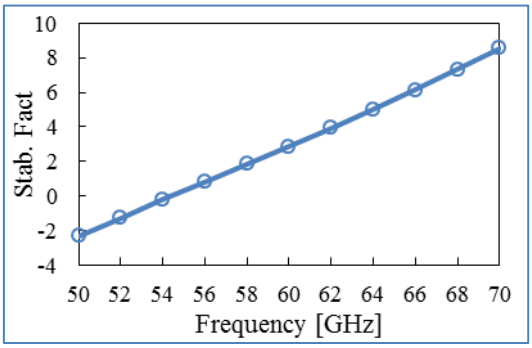

Fig. 8: Stability Factor (K) of the LNA

Table 2: Comparison chart of the various LNA's in 60 GHz band

1	[Doan, C. H]	[Domenico Pepe]	[Raffaele]	**This Work**
Year	2005	2015	2007	**2018**
Tech [nm]	130 nm	65 nm	65 nm	**65 nm**
Topology	2005	Cascode TFB	Cascode TFB	**Cascode TFB**
Gain [dB]	12	13.1	12.5	**23.16**
NF [dB]	8.8	7	7.3	**4.9**
S_{11} [dB]	-15	-16	-17	**-23.5**
S_{22} [dB]	-15	-5	N.A	**-3.5**
P1dB [dBm]	+2.0	-16	N.A	**-23**
IIP3 [dBm]	N.A	N.A	N.A	**-14**
P_{DC} [mW]	54	N.A	34	**18**

Comparison chart is presented in Table 2. It shows mm-wave LNAs with different topologies. The LNA presented in this paper achieves the highest gain for 60 GHz frequency band and minimum noise figure among all previous implementations in technologies. The simulation results indicate that the gain is improved by a factor of 43%, noise figure is improved by a factor of 30% and S_{11} is improved by a factor of 31 % by considering MOSFET's width of 12 µm.

CONCLUSION

In this paper, the design of four stage CS LNA is implemented for wideband mm-wave applications. A multiband LNA has been demonstrated in 65 nm RF-CMOS. The transistor geometry has been arrived for designing circuit schematic captured in ADS software. The simulation results demonstrated that the designed LNA is suitable for mm-wave applications of 60 GHz. The maximum gain of 26.15 dB at 54 GHz and 23.16 dB at 60 GHz with NF_{min} is less than 5.5 dB in frequency range of (57-64) GHz are achieved.

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