AUSTRALIAN JOURNAL OF BASIC AND APPLIED SCIENCES

ISSN:1991-8178 EISSN: 2309-8414
Journal home page: www.ajbasweb.com

Optimization of a Three Phase Cascaded H-Bridge Multilevel Inverters for Harmonic Elimination

[1]RosliOmar, [2]NorSyuhada, [3]Mohammed Rasheed, [4]Marizan Sulaiman, [5]Krismadinata Krismadinata,[6]Afiqah Sabari

[1,2,3,4,6]Faculty of Electrical Engineering, UniversitiTeknikal Malaysia Melaka (UTeM), Melaka,Malaysia,[5]Faculty of Engineering, Department of Electrical,Universitas Negeri Padang Indonesia.

Address For Correspondence:
RosliOmar, Faculty of Electrical Engineering, UniversitiTeknikal Malaysia Melaka (UTeM), Melaka,Malaysia,
E-mail: rosliomar@utem.edu.my

ARTICLE INFO

Article history:
Received 26 July 2016
Accepted 21 September 2016
Published 30 September 2016

Keywords:
Digital Signal processing (DSP) TMS320F2812, Cascaded multilevel, controller, Prototype Optimization, Three Phase

ABSTRACT

Background: This paper presents the analysis and the design of a three-phase cascaded H-Bridge Multilevel inverter (CHB-MLI) based on Newton-Raphson technique controller for optimization techniques in harmonic reduction of the inverter output. **Objective:**The proposed system was comprised of two separated DC sources, three-phase five-level CHB-MLI, and its controller based on Newton-Raphson. The main aim of this paper had been to design, model, construct, and conduct laboratory testing upon CHB-MLI prototype for a three-phase system. The source codes programming based on Newton-Raphson controller was developed, and then stored into the Digital Signal Processing (DSP) TMS320F2812. **Results:** The proposed controller was applied to CHB-MLI. The optimization of this system had managed to reduce the harmonic contents of the inverter output. Besides, the experimental results of the developed prototype are discussed. In addition, the performance of the proposed system was compared between simulation and experimental results for Optimization techniques. **Conclusion:**The Optimization of this system had been capable in reducing the harmonic contents of the inverter output. Thus, optimization of the CHB-MLI system had been successfully demonstrated in this study.

INTRODUCTION

The multilevel inverter concept has been employed to decrease harmonic distortion in the output waveform without decreasing the inverter power output(Omar, Rasheed & Sulaiman 2015). It has several advantages, such as lower switching frequency and switching losses, lower voltage device evaluation, lower harmonic distortion, high power quality waveform, higher efficiency, reduction of electromagnetic interference (EMI), and interfacing renewable energy sources, such as photovoltaic to the electric power grid(Omar *et al*. 2014). Nevertheless, at present, three common topologies of multilevel inverter have been proposed, which are diode-clamped, flying capacitors (FCs), and cascaded H-bridge (CHB)(Omar, Rasheed, Sulaiman, *et al*. 2015)(Rasheed, Omar, Sabari, *et al*. n.d. 2015).

Furthermore, the type of multilevel inverter that uses a single DC source rather than multiple sources is the diode-clamped multilevel inverter. Meanwhile, the FC type is designed by a series connection of capacitor-clamped switching cells. Lastly, the CHB type, which can be series or parallel connected, also consists of a series of H-bridge cells to synthesize the required voltage from several separate DC sources, which are recoverable from batteries, fuel cells, renewable energy or ultra-capacitor. Besides, this CHB topology has the least components for a given number of levels. Thus, CHB is more advantageous among other multilevel inverter topologies. Moreover, an appropriate switching angle has to be generated by using optimizing

ToCite ThisArticle: RosliOmar, NorSyuhada, Mohammed Rasheed, Marizan Sulaiman, Krismadinata Krismadinata, Afiqah Sabari., Optimization of a Three Phase Cascaded H-Bridge Multilevel Inverters for Harmonic Elimination. ***Aust. J. Basic & Appl. Sci.,*** *10(14): 225-240, 2016*

techniques to control the switching frequencies of each semiconductor switches connected(Rasheed, Omar &Sulaiman n.d. 2015). The pure sinusoidal voltage waveform can be obtained by increasing the number of DC sources as well. Thus, insulator gate bipolar transistor (IGBT) is an example of semiconductor switches that are switched on and off in any ways to keep the percentage of total harmonic distortion (THD) to its minimum value. These switches also have low block voltage and high switching frequency(Lai *et al*. 1996).

2.0 Cascaded H-Bridge Multilevel Inverter Topology:

2.1 Cascaded H-Bridge Multilevel Inverter (CHB-MLI):

The smallest number of voltage levels for a multilevel inverter using cascaded- inverter with SDCSs is three. Hence, in order to achieve a three-level waveform, a single full-bridge inverter was employed(Journal & Basic 2016)(Junling *et al*. 2008). Basically, a full-bridge inverter is known as an H-bridge cell, which is illustrated in Figure 1. The inverter circuit consisted of four main switches and four freewheeling diodes(Omar *et al*. n.d. 2015).

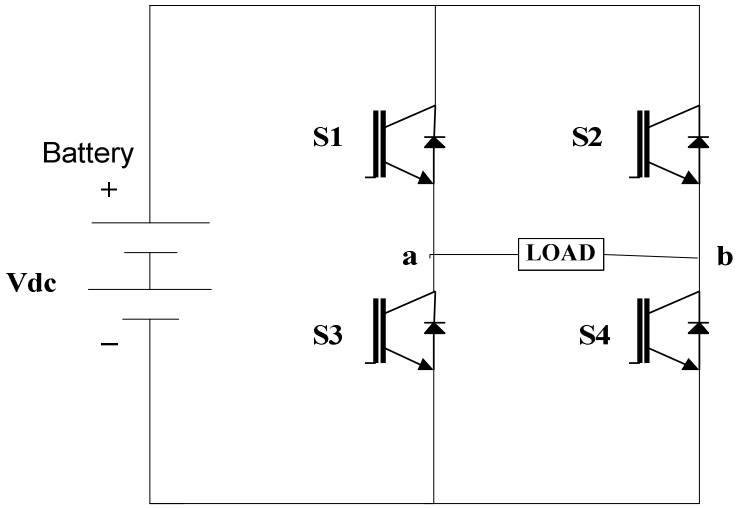

Fig.1: AnH-bridge multilevel inverter

Based on the four-switch combination, three output voltage levels, +V, -V, and 0, can be synthesized for the voltage across A and B(Jones & Satiawan 2013). During the inverter operation shown in Fig. 1, switches S1 and S4 were closed at the same time to provide VAB a positive value and a current path for Io.

Besides, switches S2 and S4 were turned on to provide VAB a negative value with a path for Io. Depending on the load current angle, the current might flow through the main switch or the freewheeling diode(Kaliamoorthy *et al*. 2014).

When all the switches were turned off, the current flowed through the freewheeling diodes. In the case of zero level, there were two possible switching patterns to synthesize zero level; S1 and S2 on, whereas S3 and S4 off. Meanwhile, the other pattern switching was S2 off, while S3 and S4 on. Additionally, a simple gate signal with repeated zero-level patterns is shown in Figure 2. All zero levels were generated by turning on S1 and S2(Gupta & Mahanty 2015).

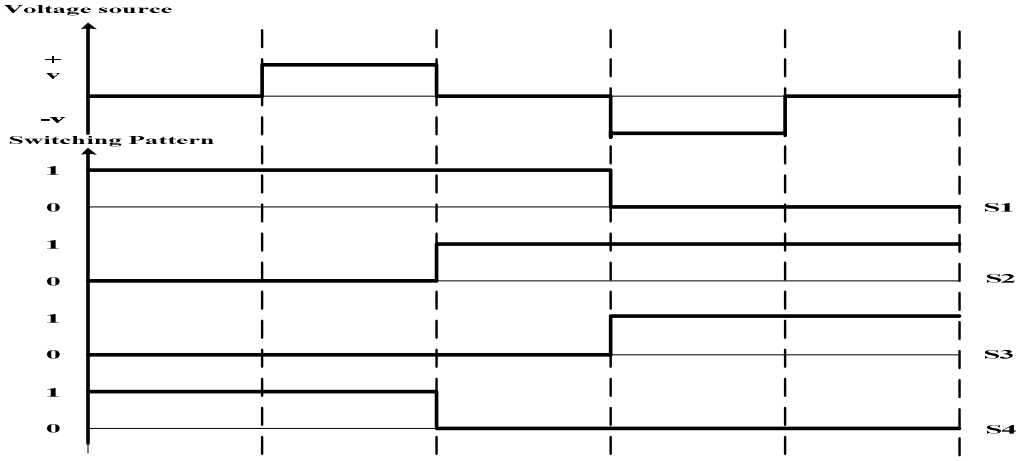

Fig. 2: Repeated zero-level switching pattern.

Note that level 1 represents the state when the gate was turned on, while level0 represents the state when the gate was turned off. Furthermore, in Figure 1, S_1andS_2wereturnedonlonger thanS_3andS_4ineachcyclebecausethesamezerolevelsswitchingpattern was used(Gupta & Khambadkone 2007).As aresult,S_1 andS_2 consumedmorepowerand generated highertempernaturethanthe othertwoswitches. Hence, in order to avoid such issues,adifferentswitchingpatternforzerolevel was applied (Gruson *et al*. 2013).

Inthefirstzerostage,S_1andS_2wereturnedon;then, in the secondzerostage, $S_3$and S_4were turned on, instead of $S_1$and S_2(Fri *et al*. 2013).Byapplyingthismethod, the turn-ontimefor eachswitchturnedouttobeequal,asshowninFigure.3.

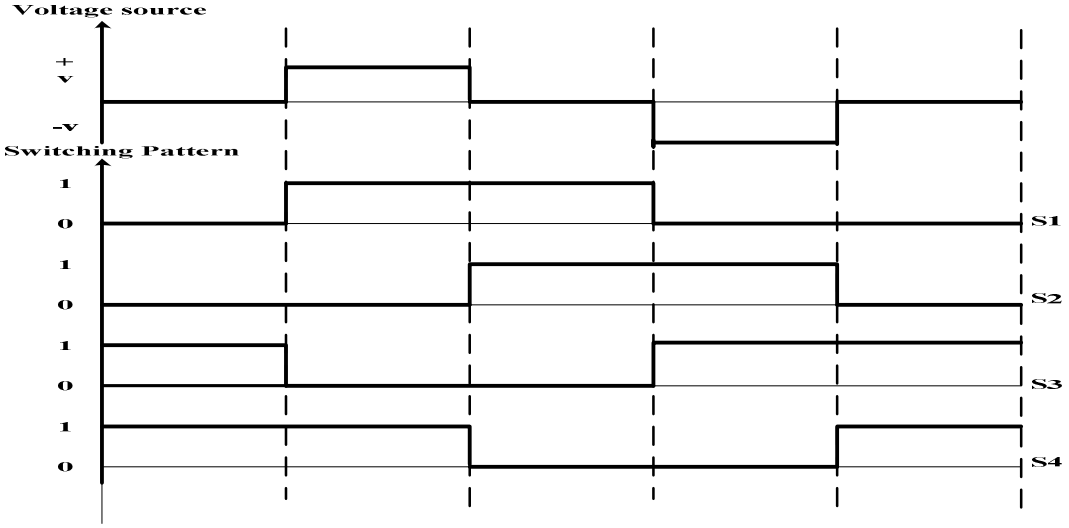

Fig.3: Swapped zero-level switching pattern.

In order tosynthesizeamultilevelwaveform,theACoutputofeachofthedifferentlevel H-bridge cells wasconnectedinseries.Thesynthesizedvoltagewaveform was,therefore,the sum of the inverter outputs. Moreover, the number ofoutputphasevoltagelevelsinacascaded- inverter is defined by

The positive output pulses are marked with P1 and P2, while the negative ones are indicated as P'1 and P'2. The Fourier series expansion of the general multilevel stepped output voltage is shown in Equation (1) and the transform was applied to Figure 4 in Equation (2), where n is the harmonic number of the output voltage of the inverter. The switching angles that are indicated as Θ1 … Θ5 and Equation (2) was chosen to obtain minimum voltage harmonics. Other than that, several fundamental frequency-switching techniques were evaluated, such as selective harmonic elimination PWM or active harmonic elimination PWM(Omer 2015).

$$V(wt) = \sum_{n=1,3,5,..}^{\infty} \frac{4Vdc}{\pi}(\cos(n.\theta_1) + \cos(n.\theta_2) + \cdots + \cos(n.\theta_5)). \quad (\frac{\sin(n\,wt)}{n}) \tag{1}$$

$$V(wt) = \sum_{n=1,3,5,..}^{\infty} \frac{4Vdc}{\pi}(\cos(n.\theta_1) + \cos(n.\theta_2)). \quad (\frac{\sin(nwt)}{n}) \tag{2}$$

An example of the switching angle calculation is given in Equation (3) to eliminate 5th, 7th, 11th, and 13th order harmonics.

$\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)+\cos(\theta_5)=5\cdot m_i$

$\cos(5\cdot\theta_1)+\cos(5\cdot\theta_2)+\ldots+\cos(5\cdot\theta_5)=0$

$\cos(7\cdot\theta_1)+\cos(7\cdot\theta_2)+\ldots+\cos(7\cdot\theta_5)=0$

$\cos(11\cdot\theta_1)+\cos(11\cdot\theta_2)+\ldots+\cos(11\cdot\theta_5)=0$

$\cos(13\cdot\theta_1)+\cos(13\cdot\theta_2)+\ldots+\cos(13\cdot\theta_5)=0$ (3)

Meanwhile, the modulation index is defined as mi and can be calculated as in Equation (4).

$$m_i = \frac{\pi V_1}{4V_{dc}} \tag{4}$$

Since the values of Equation (4) are non-linear, the calculations were obtained by using Newton–Raphson Iteration. The fundamental and high-frequency control methods are reviewed in the next section of the paper.

CHB-MLIs have been previously designed for static VAR compensators and motor drives, but the topology has been prepared with an interface with renewable energy sources due to the use of separate DC sources.

Furthermore, numerous studies have been carried out on CHB-MLIs for connecting renewable energy sources with AC grid and power factor correction

$$m = 2U+1 \quad (6)$$

Where,
m = number of output phase voltage levels
U= the number of dc sources.

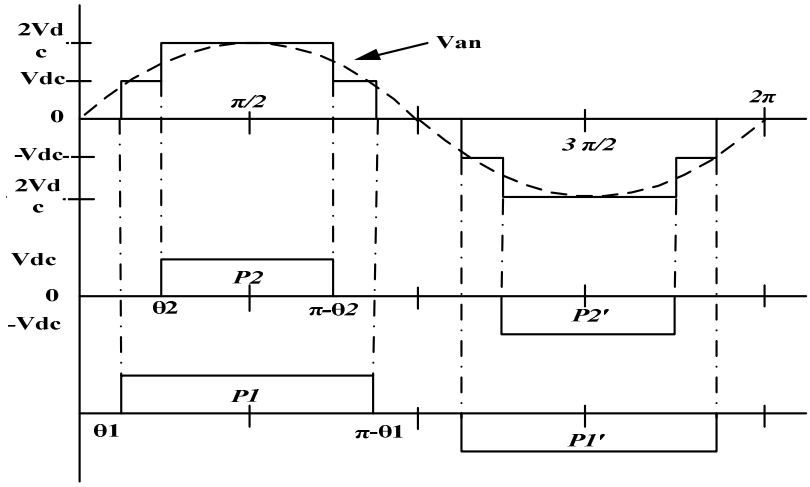

Fig.4: Phase output voltage waveforms of a five-level topology CHB-MLI with two Separate DC sources.

2.2 Construction of the Proposed CHB-MLI Scheme:

Figure 5 shows that the proposed alternative multilevel inverter topology required fewer power devices compared to the previously mentioned topologies known as CHB-MLI and the topology had been based on the series connection of H-bridges with separate DC sources.

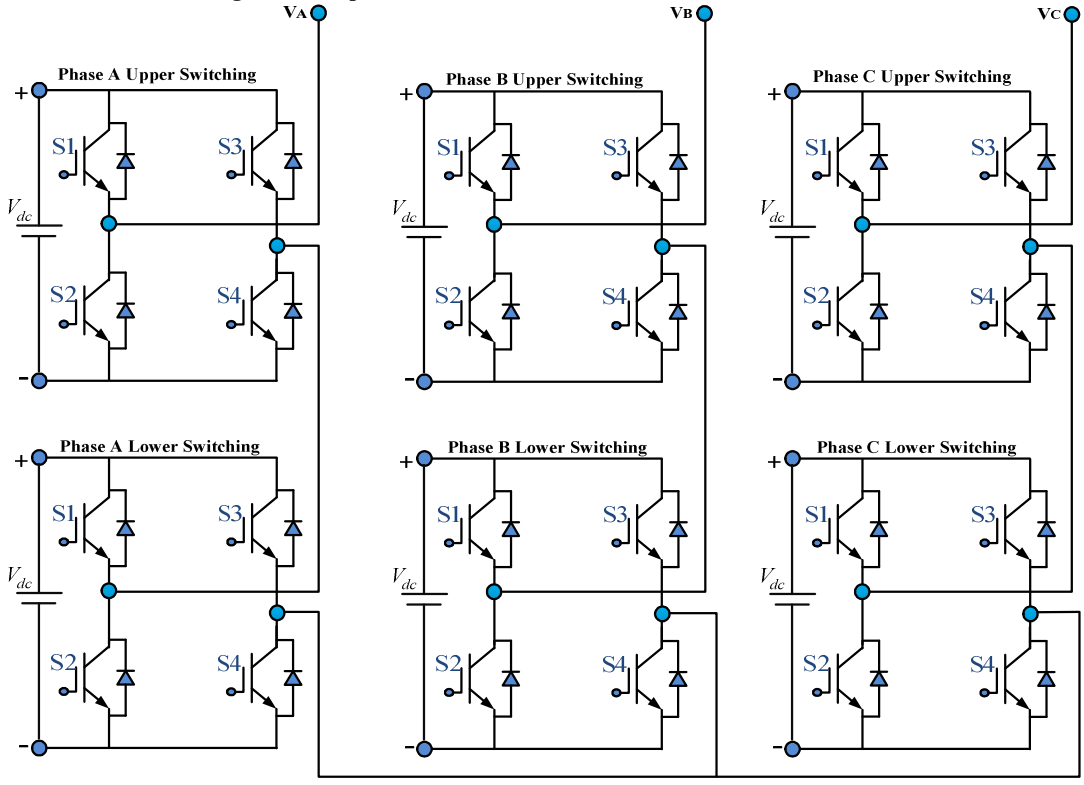

Fig.5: The Proposed Topology of a Three-Phase CHB-MLI.

Since the output terminals of the H-bridges were connected in series, the DC sources must be isolated from each other. Owing to this property, CHB-MLIs have also been proposed to be used with fuel cells or photovoltaic arrays in order to achieve higher levels. The resulting AC output voltage was synthesized by the addition of the voltages generated by different H-bridge cells. Each single phase H-bridge generated three voltage levels as +Vdc, 0, and -Vdc by connecting the DC source to the AC output by different combinations of four switches, S1, S2, S3, and S4, as depicted in the first cell of Figure 3.2. Meanwhile, the CHB-MLI that is shown in Figure 3.2 utilised two separate DC sources per phase and generated an output voltage with five levels. Therefore, in order to obtain +Vdc, S1, and S2; switches were turned on, whereas the Vdc level was obtained by turning on both S2 and S1. The output voltage was 0 by turning on S1 and S2 switches. Moreover, n was assumed as the number of modules connected in series.

2.3 Simulation Model of the Three-Phase CHB-MLI based on MATLAB/SIMULINK:

The proposed topology of CHB-MLI, as shown in Figure 3.2, was modelled via MATLAB/SIMULINK. Matlab is a software package that can be used to perform analysis, as well as solve mathematical and engineering problems. It has the characteristics of excellent programming and graphics capabilities. Meanwhile, Simulink is used to model, analyse, and stimulate dynamic system block diagram, which is fully integrated with MATLAB, easy and quick to learn, as well as flexible. It has a comprehensive library of blocks that can be used to simulate systems of linear, non-linear or discrete elements.The first step in testing the proposed three-phase five-level CHB-MLI was simulating it on software, i.e., MATLAB/SIMULINK. The system's operation was simulated at the low switching frequency. The SIMULINK model consist of DC source of 150V, pulse generator block, three unit of single phase CHB-MLI and R and L as a loads. The values of R = 100km and L= 2.07mH. The system block diagram is shown in Figure 6 and Figure 7.

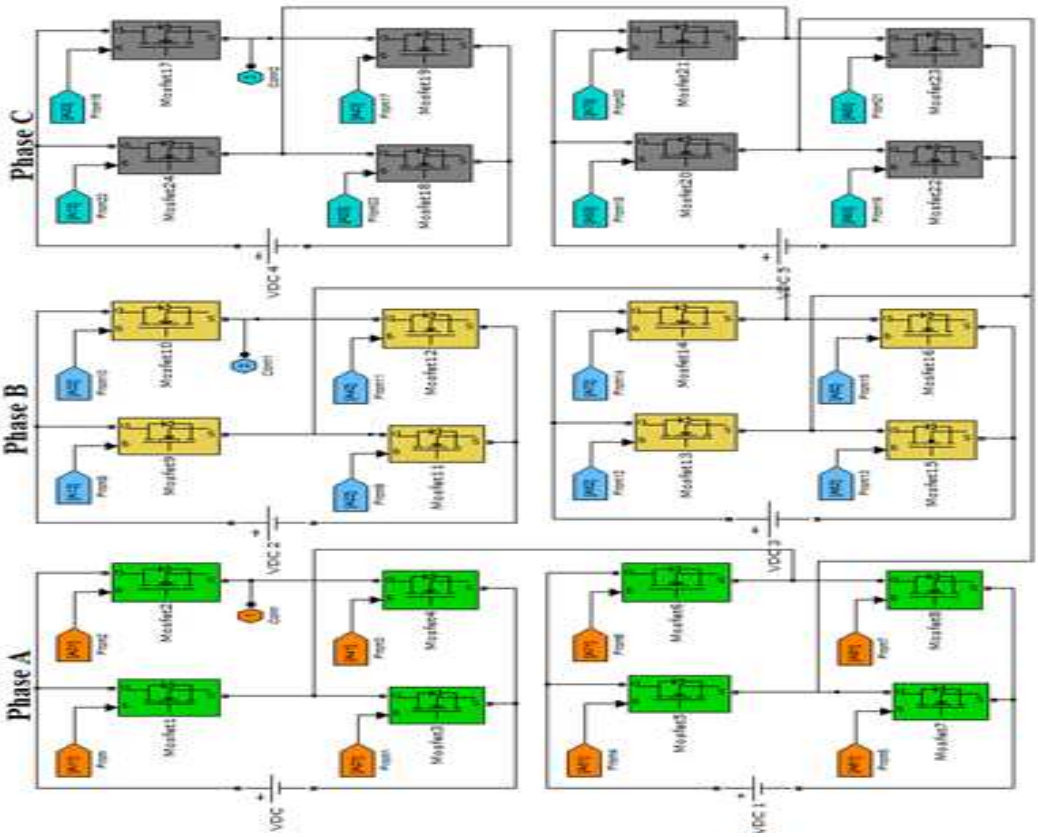

Fig.6: Five-Level CHB- MLI Model

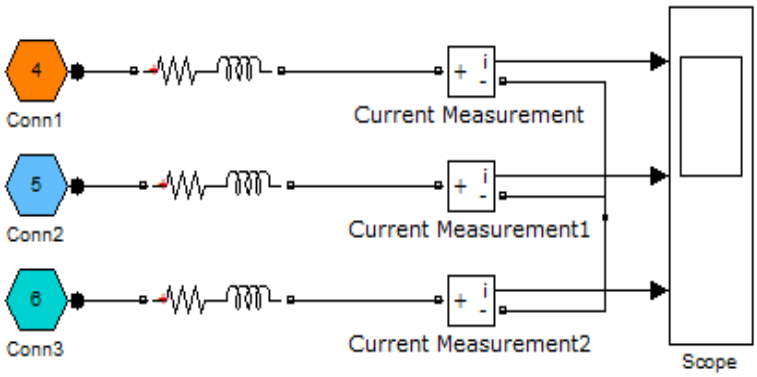

Fig.7: Current Measurement Five-Level CHB- MLI Model.

2.3.1 Simulation Results for Optimization of a Three-Phase Five-Level CHB-MLI model with MI= 0.84:

In the case of one cycle, the duration of time was equal to 0.02s for optimization of a three-phase five-level CHB-MLI and the MI used was 0.84. Besides, the proposed CHB-MLI was simulated with switching angles θ1=17.06˚ and θ2= 43.53˚ at the upper and lower switches of CHB-MLI. Figures 4.1 to 4.6 illustrate the timing diagram of phases A, B, and C. Each phase comprised of switches S1, S2, S3, S4, S5, S6, S7, and S8 for both the upper and lower switches. From Figures 8 to 13, it was observed that the upper and the lower switches had equal switching period.

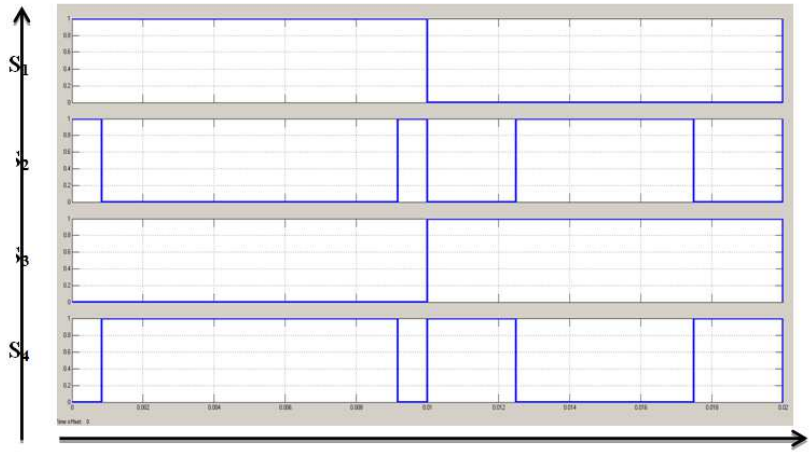

Fig. 8: Upper Switches Timing Diagram for S1, S2, S3, and S4 at phase A with MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0.

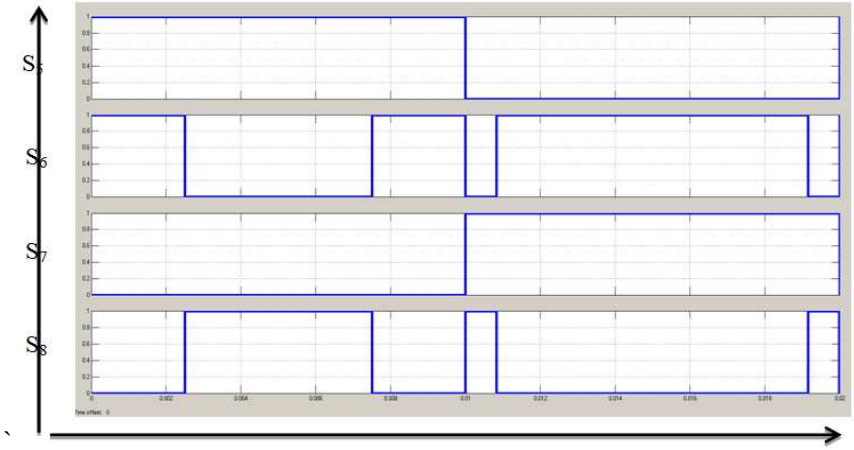

Fig. 9: Lower Switches Timing Diagram for S5, S6, S7, and S8 at phase A with MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0

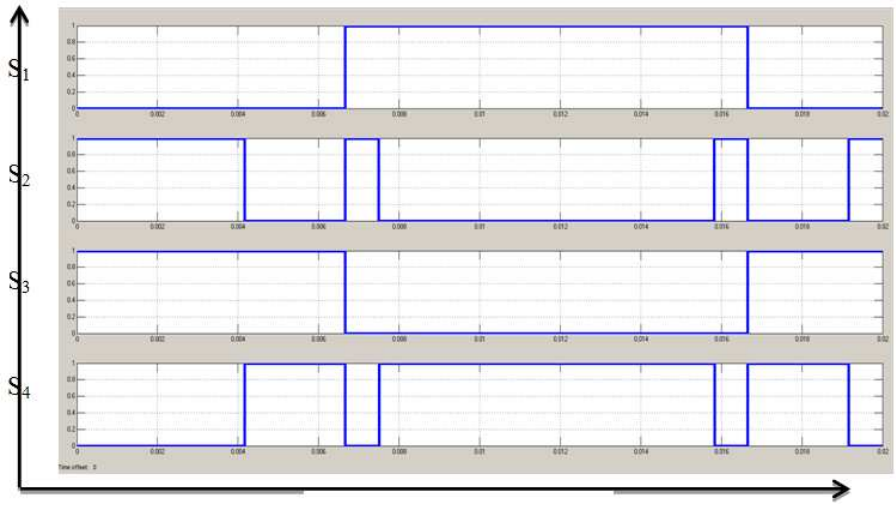

Fig. 10: Upper Switches Timing Diagram for S1, S2, S3, and S4 at phaseB with MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0.

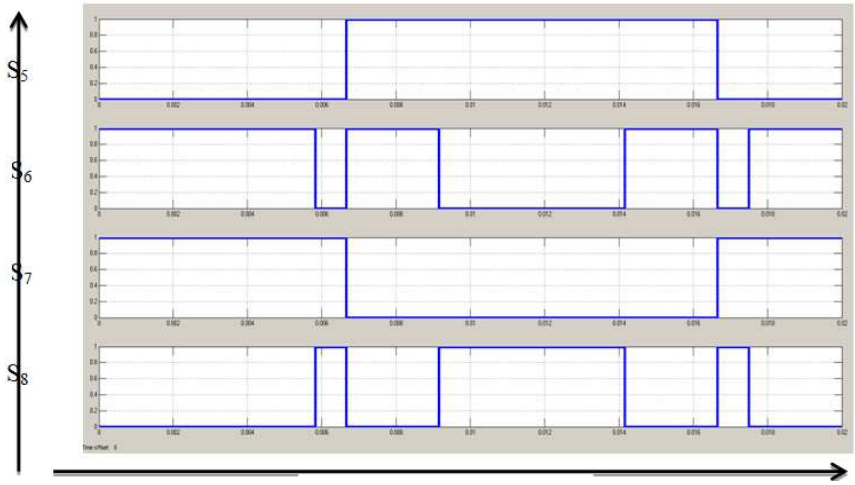

Fig. 11: Lower Switches Timing Diagram for S5, S6, S7, and S8 at phase B MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0.

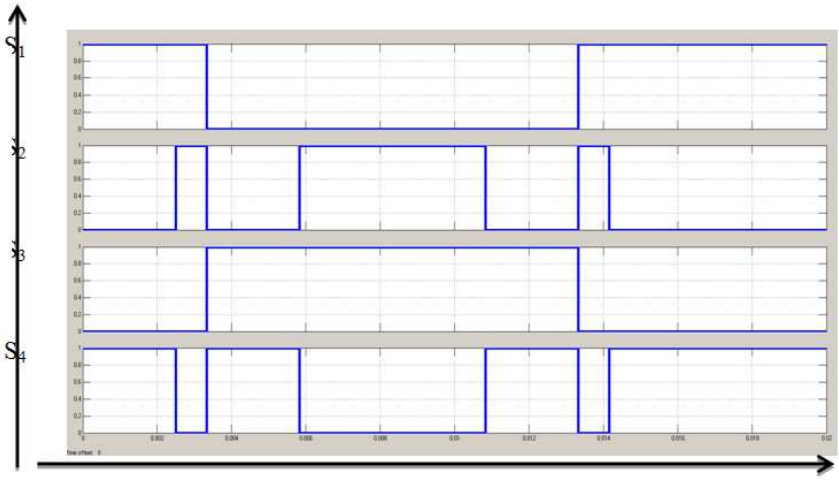

Fig. 12: Upper Switches Timing Diagram for S1, S2, S3, and S4 at phase C MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0.

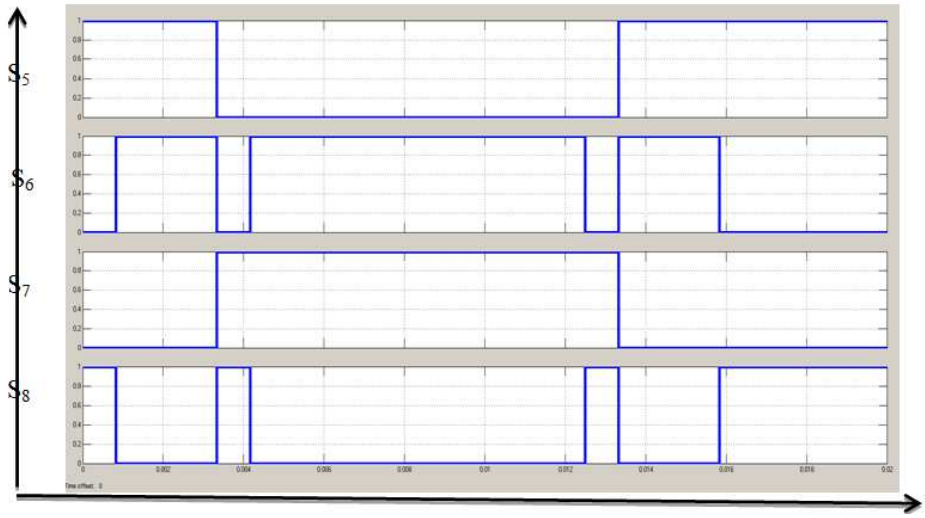

Fig. 13: Lower Switches Timing Diagram for S5, S6, S7, and S8 at phase C with MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0.

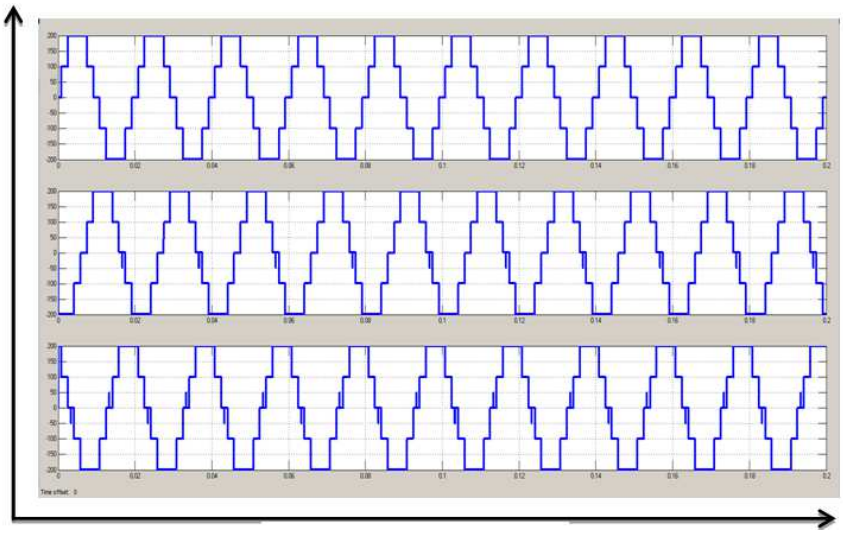

Fig. 14: Output Optimization Phase Voltage 5-level inverter based on Modulation Index MI=0.84.

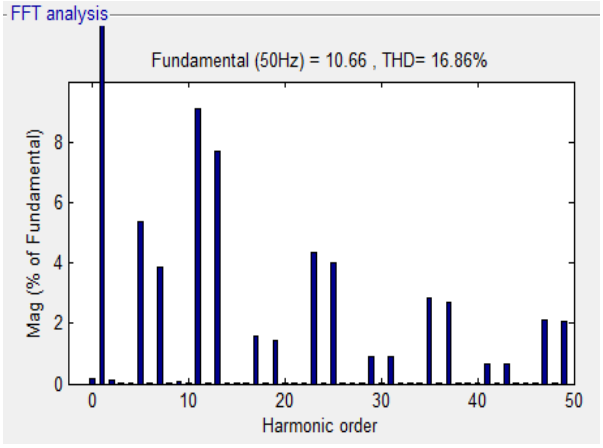

Fig. 15: Optimization Harmonic spectrum for voltage waveform output Of 5-level CHB-MLI with MI=0.84.

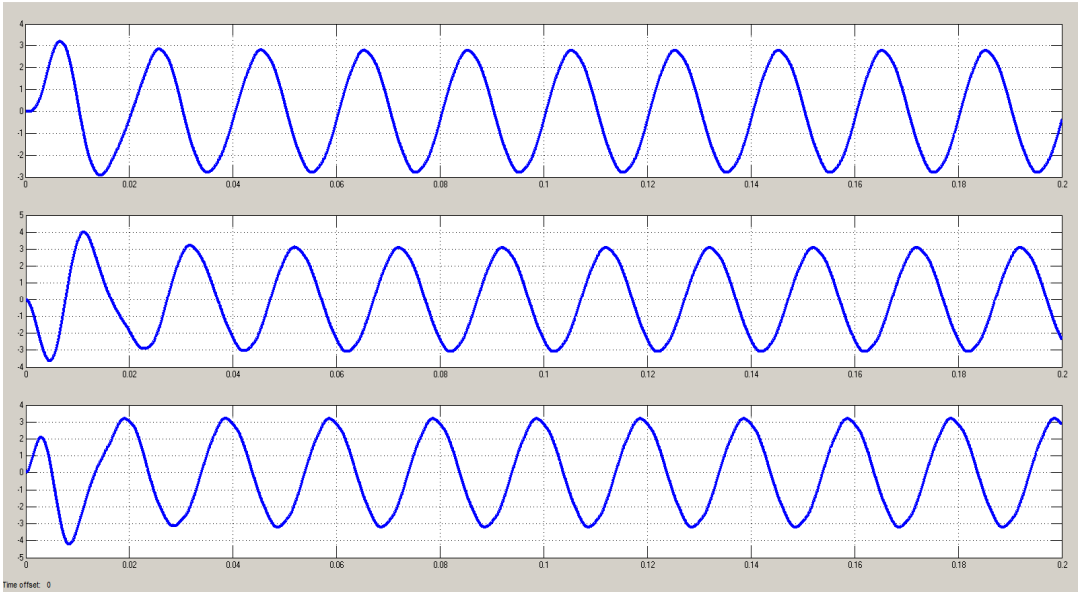

Fig. 16: Optimization Current Waveform Output of 5-level CHB-MLI withMI=0.84.

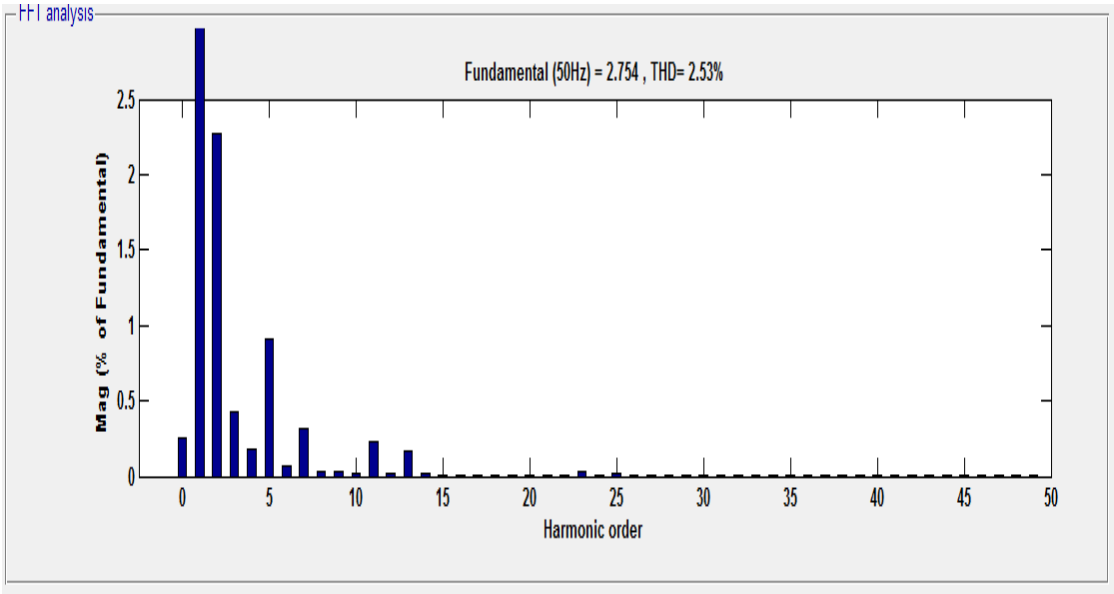

Fig. 17: Optimization harmonic spectrum for current waveform output of 5-level of CHB-MLI with MI=0.84.

Figure 16 shows the optimization for the current output waveform of 5-level CHB-MLI for Phases A, B, and C respectively. The optimization output current waveforms for each phase of CHB-MLI had been very smooth due to accurate calculation of the switching angles. Figure 17 shows the harmonic spectrum of optimization for the current output waveform of CHB-MLI with THD values equivalent to 2.53%. The THD value, in fact, met the IEC standard.

2.4Prototype development of Three-Phase Experiment Circuits:

With regard to the hardware connection of the system, a prototype model of the CHB-MLI system was constructed and tested to verify the proposed systems operations shown in the experimental setup. The full system is shown in Figure 18. The system consisted of DC power supply, three-phase five-level CHB-MLI with DSP-based control circuit connected RL loads, and a personal computer (PC).

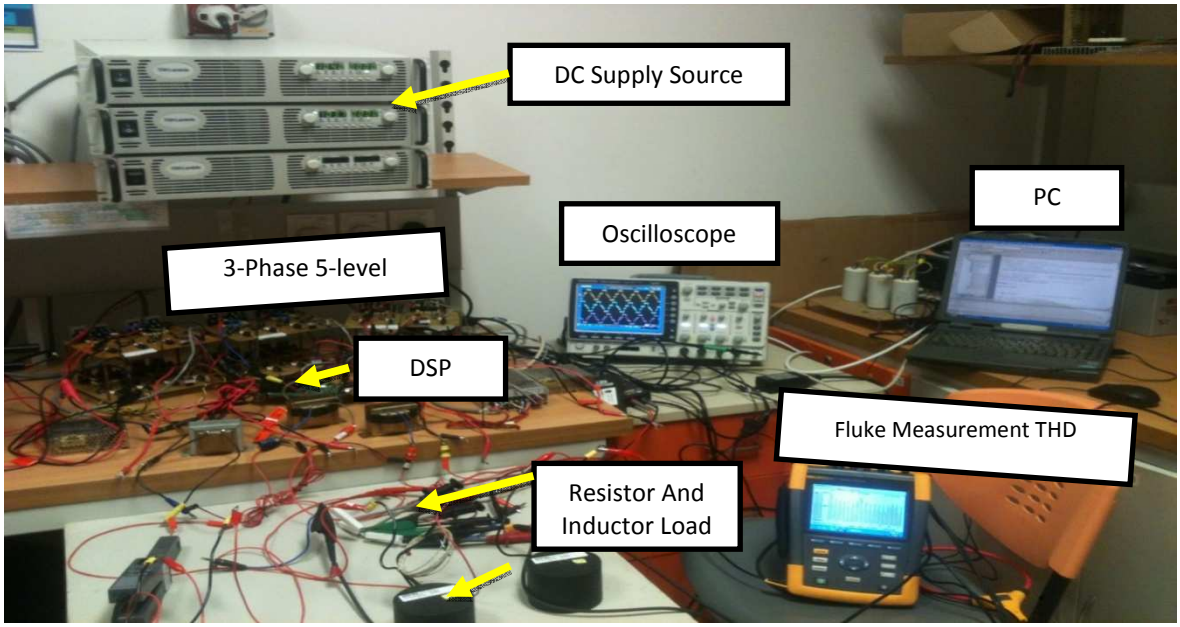

Fig.18: The Overall Experimental set-up for the Prototype of Five-Level CHB MLI Inverters.

2.4.1Optimization Experimental Results of A Three-Phase 5-level CHB-MLI (MI=0.84):

In order to determine if the simulation results are in good agreement with the experimental results, a source code based on Newton-Raphson controller for optimization of a three-phase five-level CHB-MLI had been developed. The developed source codes programming, as shown in Appendix C (I), were then stored into DSPTMS320F2812. The DSPTMS320F2812 card was then interfaced with the proposed prototype of CHB-MLI. In the source code programming, one cycle for the duration of time was equal to 0.02s with MI=0.84. Meanwhile, the values of the switching angles were θ_1= 17.06° and θ_2= 43.53°at the upper and lower switches of CHB-MLI. Moreover, Figures 4.41 to Figure 4.49 show the timing diagram of phases A, B, and C. Each phase comprised of switches S_1, S_2, S_3, andS_4, as well as S_5, S_6, S_7, andS_8 for upper and lower switches respectively. Besides, from Figures 19 until 24, it had been noted that the upper and lower switches for each phase had equal switching period.

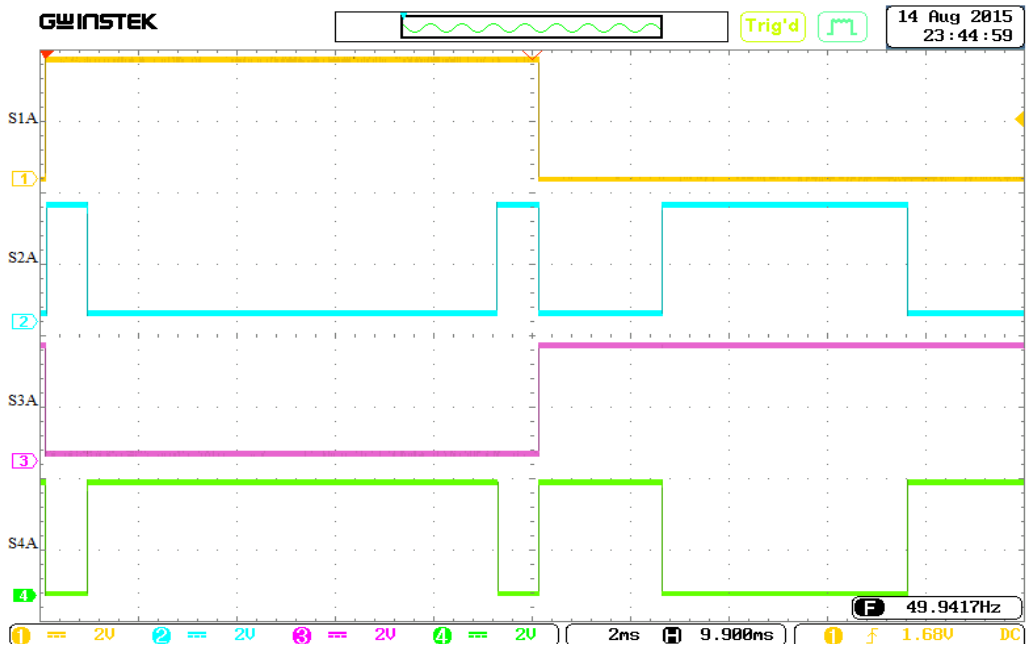

Fig.19: Upper Switches Timing Diagram for S1, S2, S3, and S4 at PhaseA with MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0.

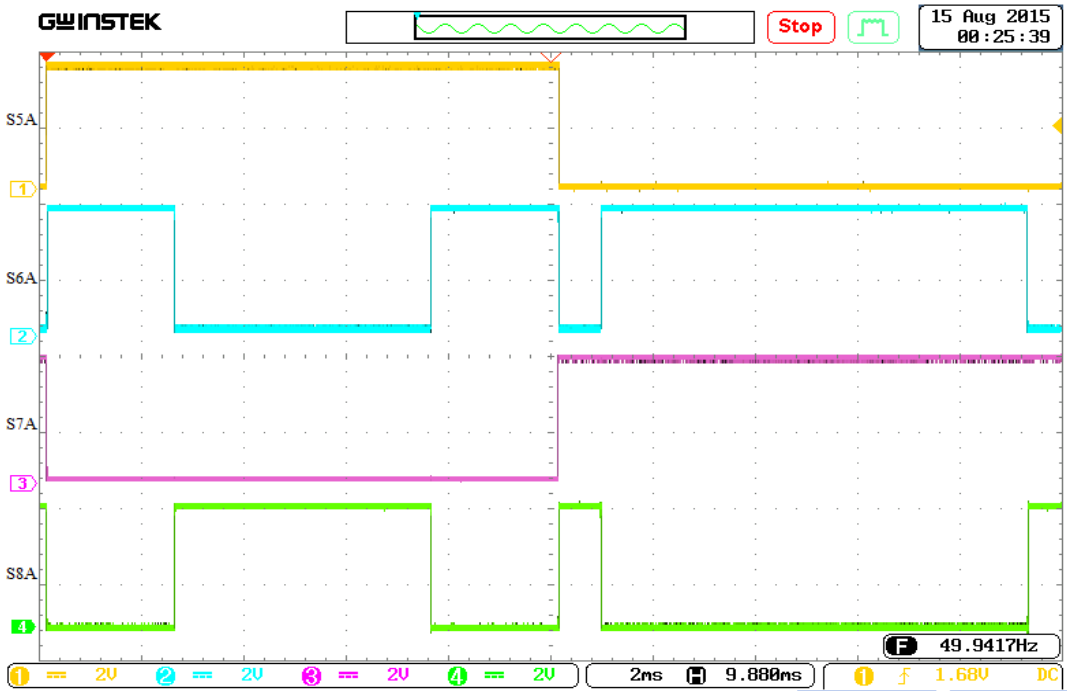

Fig.20: Lower Switches Timing Diagram for S5, S6, S7, and S8 at phaseA with MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0.

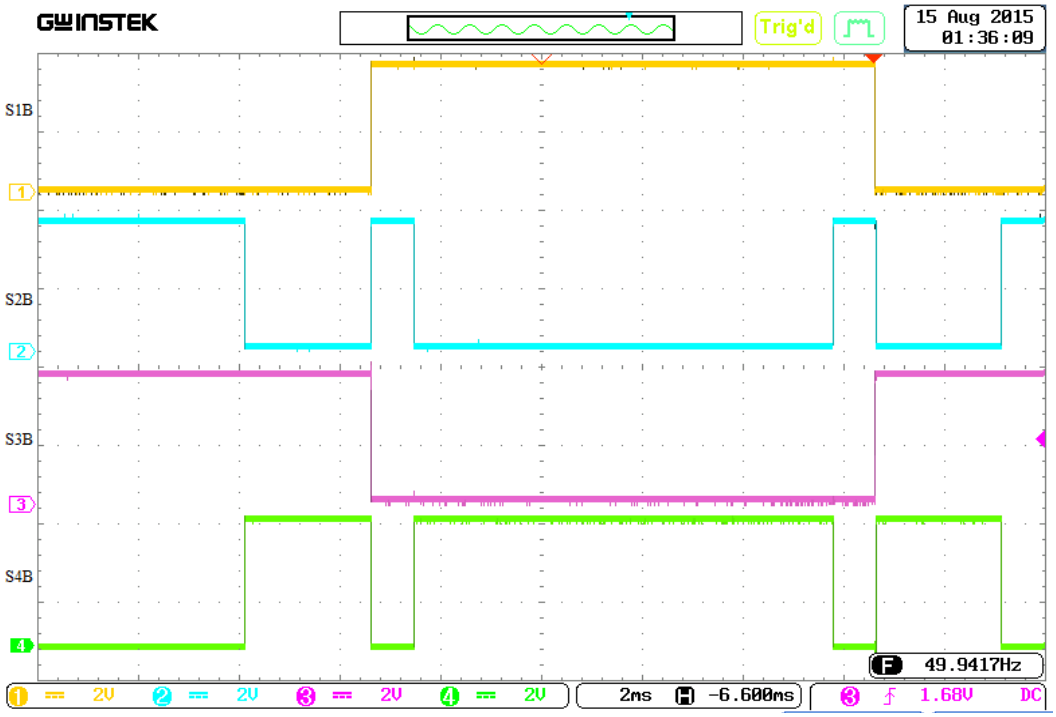

Fig.21: Upper Switches Timing Diagram for S1, S2, S3, and S4 with MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0.

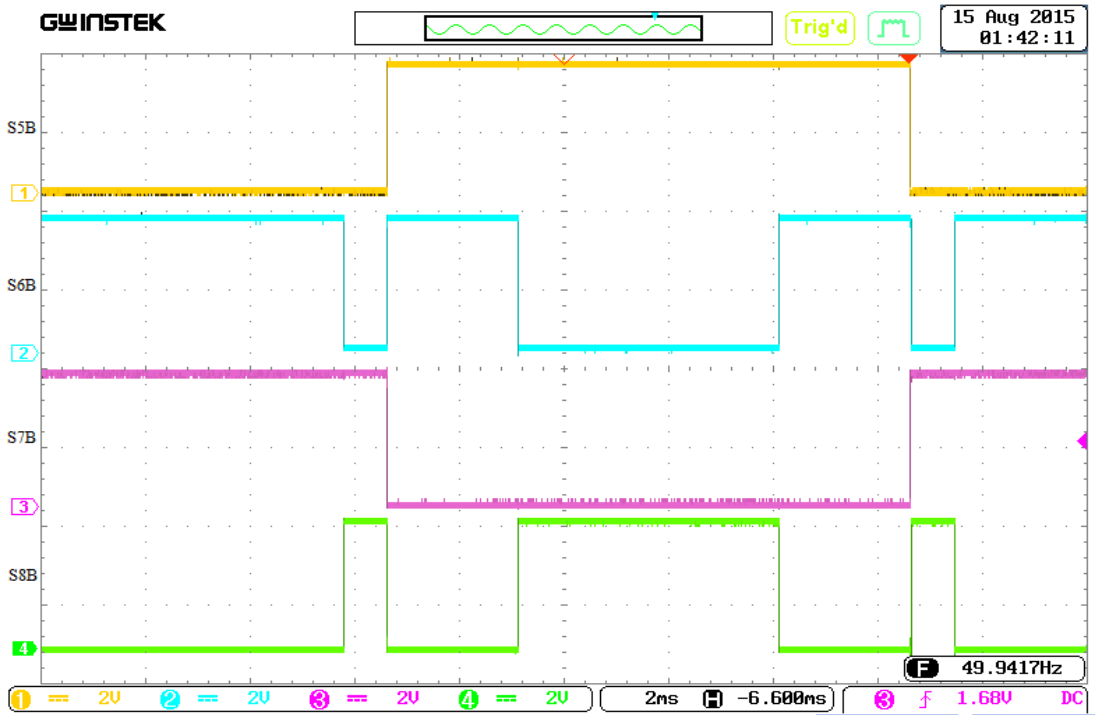

Fig.22: Lower Switches Timing Diagram for S5, S6, S7, and S8 for Phase B with MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0.

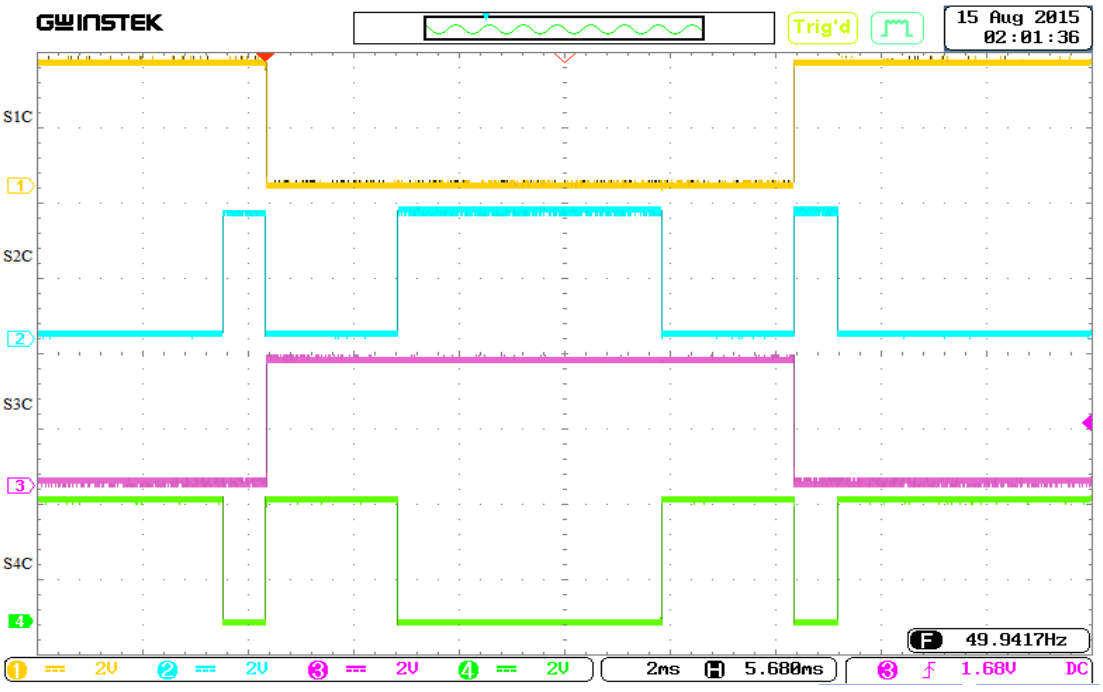

Fig.23: Upper Switches Timing Diagram for S1, S2, S3, and S4 for Phase Cwith MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0.

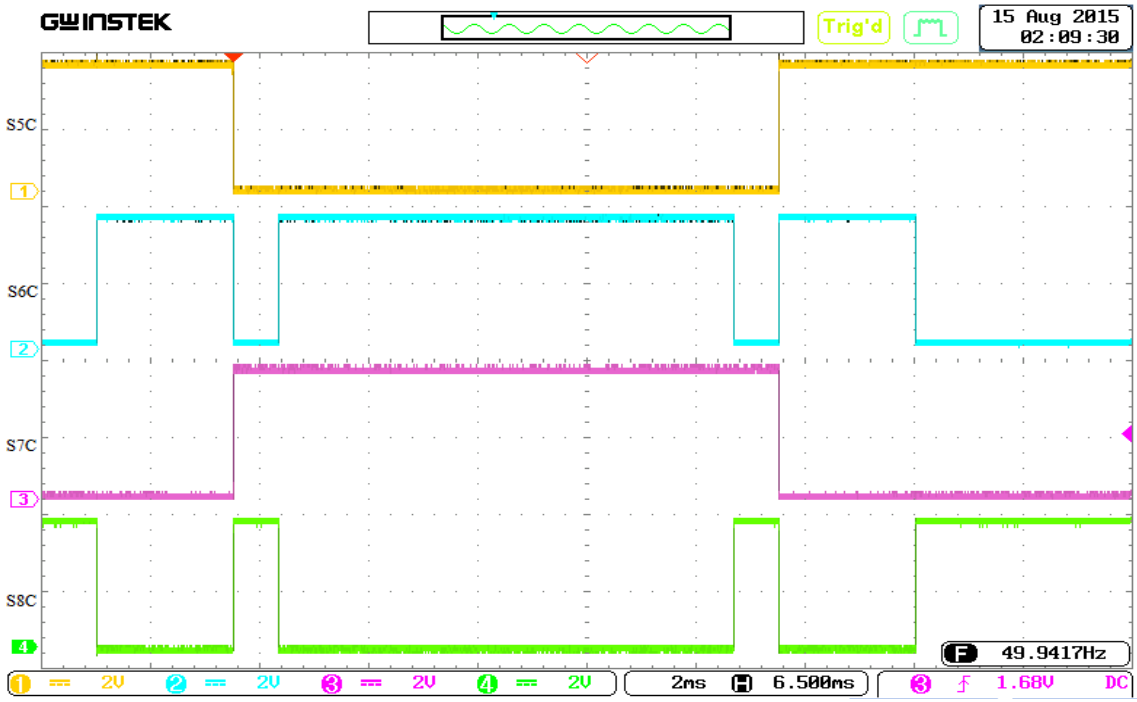

Fig.24: Lower Switches Timing Diagram for S5, S6, S7, and S8 for Phase CWith MI=0.84 for θ_1 =17.06^0 and θ_2 =43.53^0.

Figure 25 shows the optimization voltage output waveform of 5-level CHB-MLI for Phases A, B, and C respectively. The optimization of voltage output waveforms for each phase of CHB-MLI had been very smooth due to accurate calculation of the switching angles. Figure 26 shows the harmonic spectrum of the optimization of voltage output waveform for CHB-MLI with THD values equivalent to 15.6%.

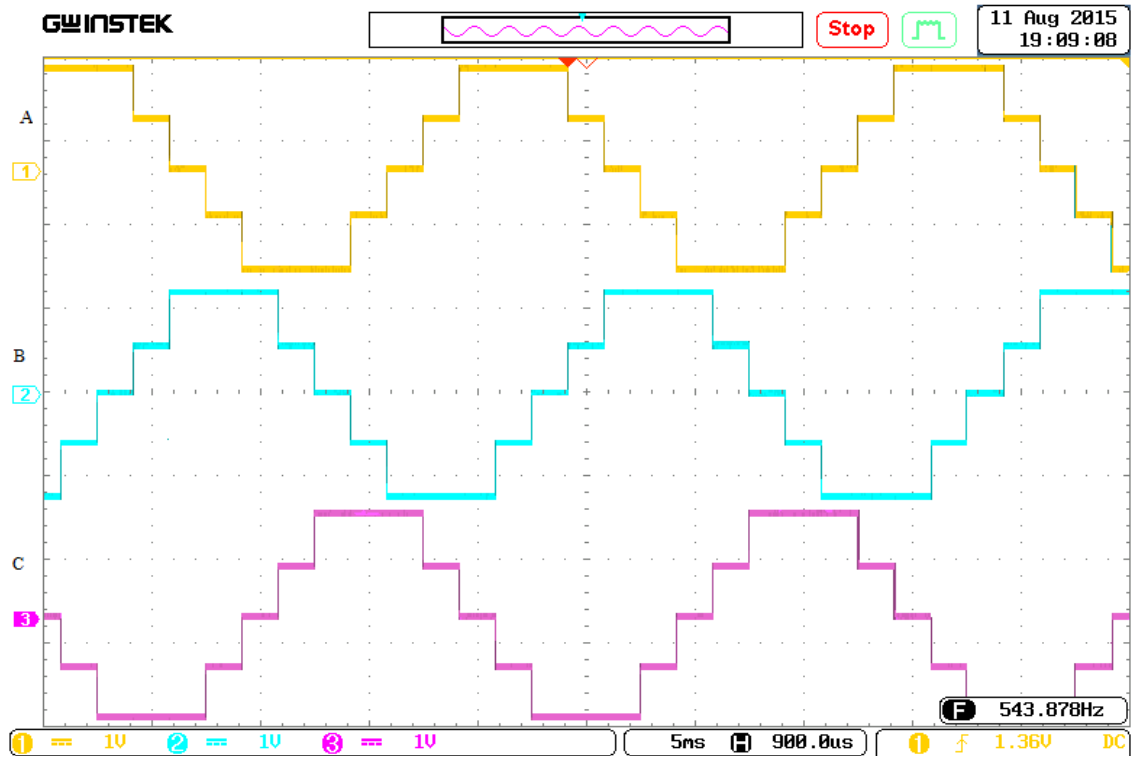

Fig.25: Optimization of Voltage Output Waveform of 5-Level CHB-MLIwith MI=0.84.

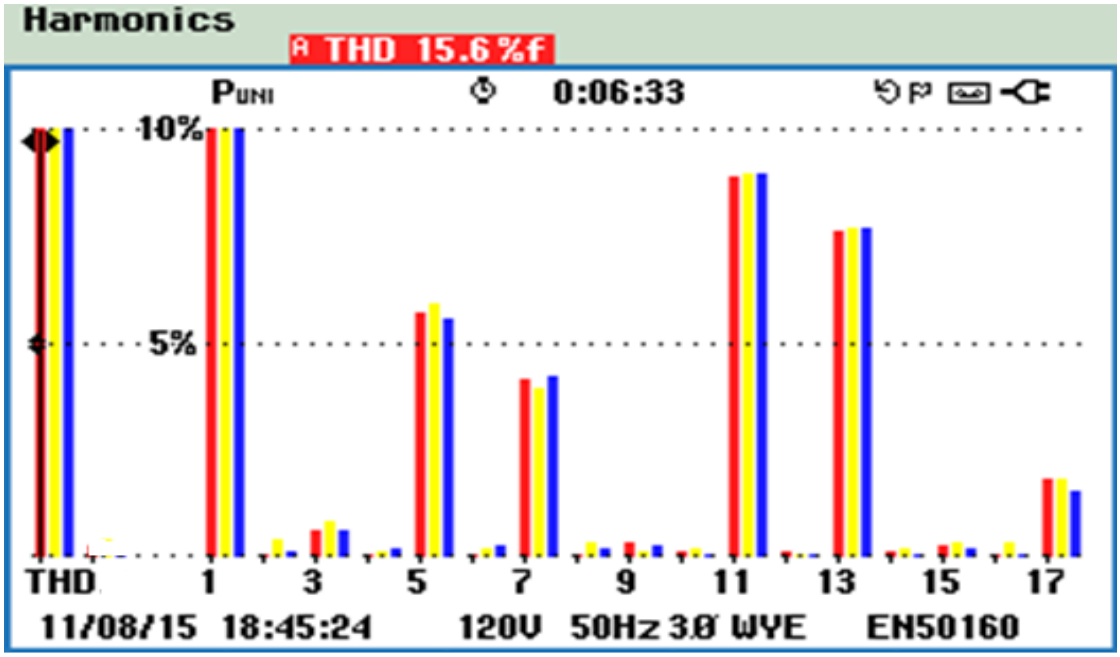

Fig.26: Optimization Harmonic Spectrum of Voltage Output Waveform ofCHB-MLI with MI=0.84.

Figure 27 shows the optimization of voltage and the current output waveform of 5-level CHB-MLI for Phases A, B, and C respectively. The optimization of current output waveforms for each phase of CHB-MLI had been very smooth due to accurate calculation of the switching angles. Figure 28 shows the harmonic spectrum of the optimization of current output waveform of CHB-MLI with THD values equivalent to 3.9%. The THD obtained met the International Electrical Code (IEC) standard.

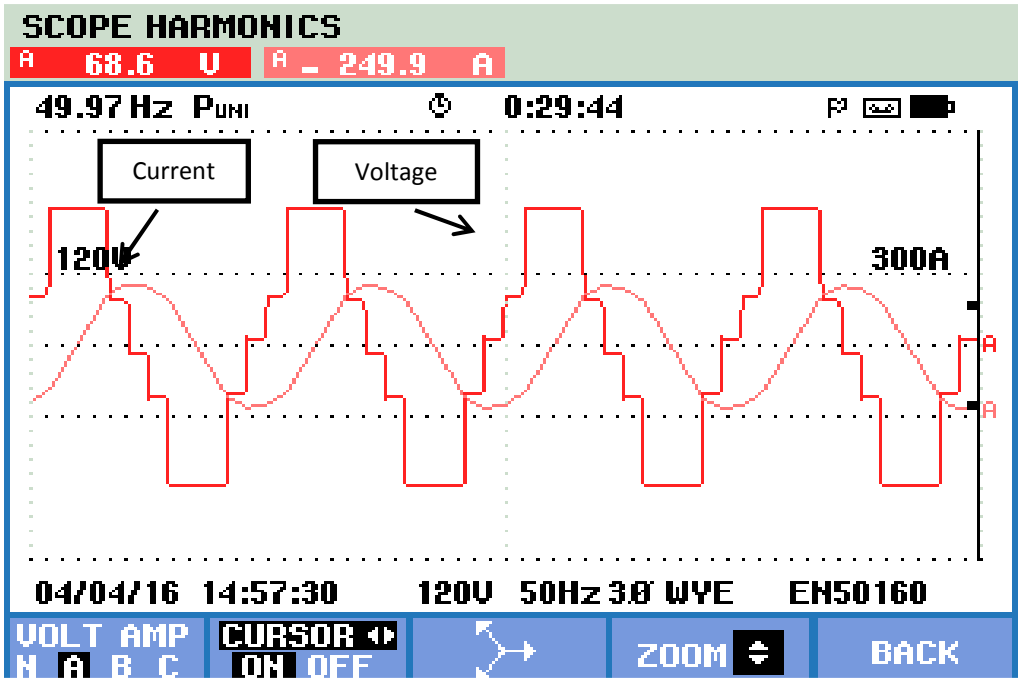

Fig.27: Optimization Voltage and Current Output Waveform of 5-Level CHB-MLIWith MI=0.84.

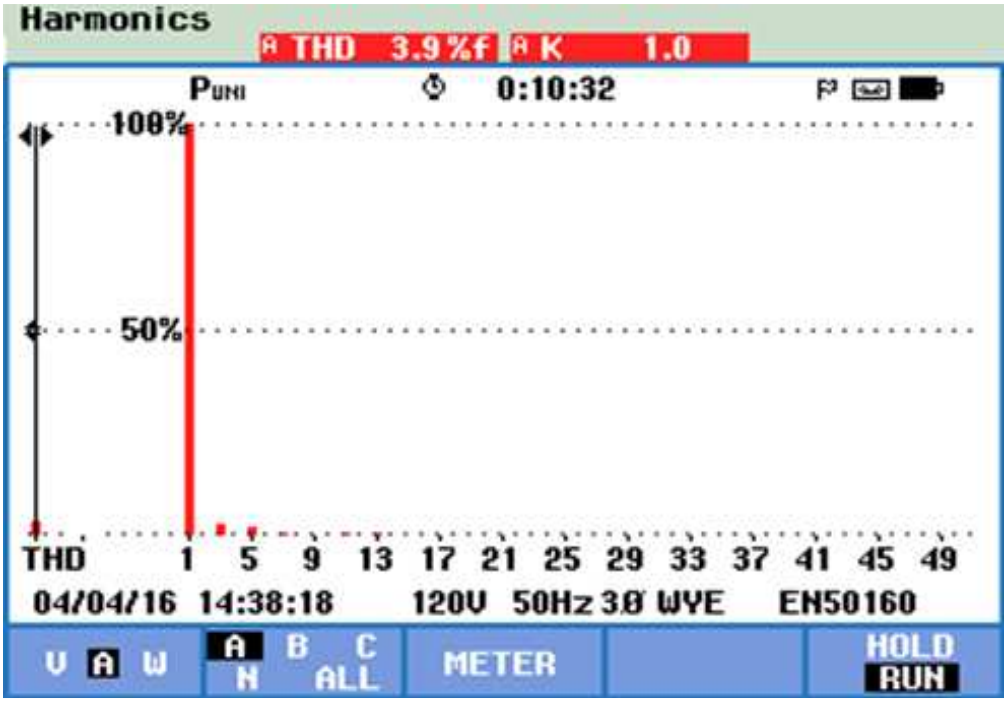

Fig.28: Optimization Harmonic Spectrum of Current Output WaveformOf CHB-MLI with MI=0.84.

Conclusion:

Simulations and experimental work had been carried out successfully. The simulation studies showed the best results on the designed CHB-MLI based on a three-phase system. Each step of the simulation studies had been conducted properly and displayed the good possibility to implement the control technique in hardware. After the simulation studies were accomplished, the study was continued with the experiments. The simulation results for Optimization is in good agreement with the experimental results, which further exhibited the effectiveness of the proposed developed prototype and its controller.

ACKNOWLEDGMENT

The authors wish to thank UniversitiTeknikal Malaysia Melaka (UTeM) for supporting this research under the grant FRGS/1/2016/TK04/UTeM/02/8.

REFERENCES

Fri, A., R.Bachtiri, El &A.Ghzizal, El, 2013. A Comparative Study of Three Topologies of Three-phase (5L) Inverter for a PV System. *Energy Procedia*, 42: 436-445. Available at: http://linkinghub.elsevier.com/retrieve/pii/S1876610213017463 [Accessed November 5, 2014].

Gruson, F. *et al*., 2013. A Simple Carrier-Based Modulation for the SVM of the Matrix Converter. *IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS*, 9(2): 947–956.

Gupta, A.K. andA.M.Khambadkone, 2007. A Simple Space Vector PWM Scheme to Operate a Three-Level NPC Inverter at High Modulation Index Including Overmodulation Region, With Neutral Point Balancing. *IEEE Transactions on Industry Applications*, 43(3): 751-760. Available at: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4215003.

Gupta, V.K. andR.Mahanty, 2015. Optimized switching scheme of cascaded H-bridge multilevel inverter using PSO. *International Journal of Electrical Power & Energy Systems*, 64: 699-707. Available at: http://linkinghub.elsevier.com/retrieve/pii/S014206151400516X [Accessed November 5, 2014].

Jones, M. andI.N.W.Satiawan, 2013. A simple multi-level space vector modulation algorithm for five-phase open-end winding drives. *Mathematics and Computers in Simulation*, 90: 74-85. Available at: http://www.sciencedirect.com/science/article/pii/S0378475412001152 [Accessed September 17, 2014].

Journal, A. andO.F.Basic, 2016. AUSTRALIAN JOURNAL OF BASIC AND Transformerless High Boost Interleaved Boost Dc-Dc Converter for Fuel Cell Application., 10: 105-109.

Junling, C. *et al*., 2008. A closed-loop selective harmonic compensation with capacitor voltage balancing control of cascaded multilevel inverter for high-power active power filters. *2008 IEEE Power Electronics Specialists Conference*, pp.569-573. Available at:

http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4591990.

Kaliamoorthy, M., V.Rajasekaran and I.Gerald Christopher Raj, 2014. Single-phase fifteen-level grid-connected inverter for photovoltaic system with evolutionary programming based MPPT algorithm. *Solar Energy*, 105, pp.314–329. Available at: http://www.sciencedirect.com/science/article/pii/S0038092X14001650 [Accessed September 17, 2014].

Lai, J., S.Member andF.Z.Peng, 1996. Multilevel Converters-A New Breed of Power Converters. *IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS*, 32(3): 509-517.

Omar, R. *et al*., 2014. Australian Journal of Basic and Applied Sciences Harmonic Reduction for Diode Clamped and Cascaded H-Bright , Five to Nine Levels of Multilevel Inverters Application., 8: 211-227.

Omar, R., M.Rasheed, M.Sulaiman, *et al*., 2015. Comparative Study of a Three Phase Cascaded H-Bridge Multilevel Inverter for Harmonic Reduction. *TELKOMNIKA Indonesian Journal of Electrical Engineering*, 14(3): 481-492. Available at: http://www.iaesjournal.com/online/index.php/TELKOMNIKA/article/view/7949 [Accessed November 11, 2015].

Omar, R. *et al*., MODELING AND SIMULATION OF A THREE PHASE MULTILEVEL INVERTER FOR HARMONIC REDUCTION BASED ON MODIFIED SPACE VECTOR PULSE WIDTH MODULATION (SVPWM).

Omar, R., M.Rasheed andM.Sulaiman, 2015. A Survey of Multilevel Inverter based on Cascaded H-Bridge Topology and Control Schemes., 3(2): 1097-1108.

Omer, R., 2015. Harmonic Reduction of Cascaded H-Bridge Multilevel Inverter Based on Newton-Raphson., 10(3): 6569-6580.

Rasheed, M., R.Omar, A.Sabari, *et al*., 2016. Validation of a Three-Phase Cascaded Multilevel Inverter based on Newton Raphson (N . R .)., 9: 1-13.

Rasheed, M., R.Omar andM.Sulaiman, Design and Development Multilevel Inverterwith Different Modulation Index (MI) Based on Super Capacitor (SC) for Harmonic Reduction., 34(6): 760-769.