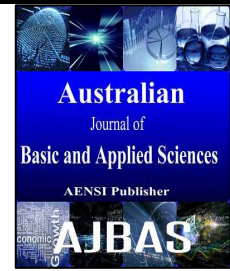




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Design of Power Efficient DET D-Flip Flop for Portable Applications

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ABSTRACT

Owing to larger increase in the demand of portable devices, low power device design technique has acquired a significant place. To backup this demand we propose a new Double Edge Triggered Flip Flop in order to ease the portability. The existing DET D Flip Flop design is subjected to different substrate bias voltages in sub threshold region to achieve better design. This modified design has been compared with previous design Technique to show the design superiority. Due to better choice of portability, the power of DET D FF has considerably diminished which has been proved through the simulation results.

INTRODUCTION

The latest advances in mobile battery-powered devices such as the Personal Digital Assistants (PDA) and mobile phones have set new goals in digital VLSI design. The mobile devices require high speed and low power consumption and thus power-delay product plays important role in the designing of VLSI circuits. The operation of low frequency circuits in the sub-threshold region stands out as the optimal method of power reduction (Wang, A., 2005). Sub-threshold current of a MOSFET transistor occurs when the gate-to-source voltage (VGS) of a transistor is lower than its threshold voltage (VTH). When VGS is larger than VTH, majority carriers are repelled from the gate area of the transistor and a minority carrier channel is created. This is known as strong-inversion, as more minority carriers are present in the channel than majority carriers. When VGS is lower than VTH, there are less minority carriers in the channel, but their presence comprises a current and the state is known as weak-inversion. In standard CMOS design, this current is a sub-threshold parasitic leakage, but if the supply voltage (VDD) is lowered below VTH, the circuit can be operated using the sub-threshold current with ultra-low power consumption. Sub-threshold circuit operation is driven by currents much weaker than standard strong-inversion circuits, and so is characterized by longer propagation delays and limited to lower frequencies. One of the most complex, power consuming and indispensable components is the Flip-Flop (FF) among the various building blocks in digital designs about 30%-70% of the total power in the system is dissipated due to clocking network, and the flip-flops (Vladimir Stojanovic 1999). The logic gate delays in a clock period is reducing by 25% per generation in high-performance microprocessors, and is approaching value of 10% or below beyond 0.13 μ m technology (Tschanz, J., 2001). As a result, latency of the flip-flops or latches is becoming larger portion of the cycle time. Several FF designs have been proposed for power reduction. Although many of these methods have been shown to considerably reduce the power consumption, they are not necessarily suitable for operation in the sub-threshold region. In addition, some of these designs require a large number of transistors for implementation, resulting in a large area, not necessarily suitable for small, low-priced systems.

Two type of flip flops are found in literature – single edge triggered (SET) and double edge triggered (DET). The single edge-triggered flip flop samples the data on only one clock edge (either on rising or falling clock edge). The SET flip-flops are usually configured as Master- Slave configuration.

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In a single edge-triggered (SET) flip-flop, data move from input to output in synchrony with one edge of the clock. In a DET flip-flop, both rising and falling edges of the clock signal are used to transfer data from input to output. In this way, for a given throughput, the clock frequency can be halved with respect to a system using SET flip-flops, with a reduction of power consumption.

Threshold voltage of the transistor plays significant role in controlling the leakage current. Threshold voltage of the transistor depends on the biasing of the transistor. Considerable work has been done to control the leakage current by substrate biasing technique and in turn to reduce the power dissipation (Tripti Sharma, K.G., 2010; Narendra, S., 2004). The Double edge triggered DET D-FF design [1] is modified by using substrate biasing technique (Sharma Tripti, K.G., 2011). Here the STGB, LVSB and NBB designs are compared.

Existing Det D-Flip Flop:

Several DET D-Flip flop designs (Gary, K., Yeap, 1998; Chung, W.M., 2002; Yu Chien-Cheng, 2007) were proposed. The earliest proposed DET flip-flop (Yu Chien-Cheng, 2008) is illustrated in Figure 1. This design can be thought of as a parallel connection of two latches, one transparent when the clock is high and the other transparent when the clock is low, with a multiplexor selecting the output of the latch that is in hold state. In the upper data path, transistor MP2 provides feedback to pull up storage node X substantially to VDD when signal node XB is low. Pull-up transistor MP2 ensures that, although a clock signal applied to the gate of MN1 does not reach the voltage VDD , the storage node X can still reach VDD . In the lower data path, transistor MN2 provides feedback to pull down node Y to a lower voltage when the signal node YB is high. The inclusion of pull-down transistor MN2 ensures that, although the clock signal applied to the gate of MP1 does not reach the voltage GND , the storage node Y can still reach GND .

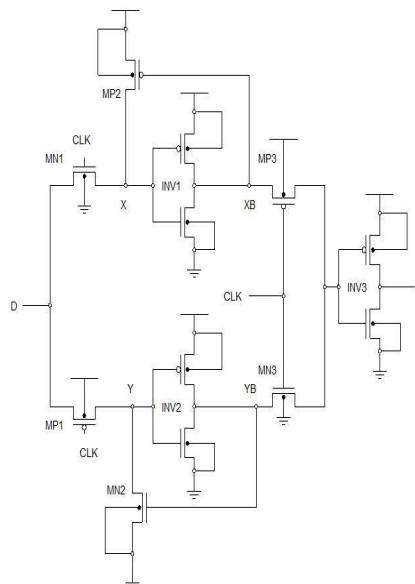


Fig. 1: Earlier proposed 12-Transistor DET D-FF.

When the clock is in the "high" state, for the upper data path, the input signal D is quickly conducted into the node XB . If the input signal D is "high", node X goes to the logic high with help from the pull-up transistor $MP2$. Node X remains high as long as input signal D is at the high level. Meanwhile, for the lower data path, the previously hold data is quickly pass to the output node Q with help from the transistor $MN3$. On the contrary, when input signal D falls while the clock is in the "low" state, for the lower data path, the input signal D is quickly conducted into the node YB and node Y goes to the logic low with help from the pull-down transistor $MN2$. Node Y remains low as long as input signal D is at the low level. Meanwhile, for the upper data path, the previously hold data is quickly pass to the output node Q with help from the transistor $MP3$.

Proposed Designs:

In this paper the existing 12-transistor design is modified to reduce the power consumption so that the design can be applicable for portable applications. The low power 12-transistor DET Flip flop design is achieved by changing the substrate connections.

Fig.2 shows Low Voltage Swapped Body (LVSB) bias 12-transistor design. In this design, substrate of all PMOS transistor are connected to ground and substrate of all NMOS transistors are connected to the supply

voltage (V_{dd}). In this type of substrate connection, bulk voltage is less than the source voltage ($V_B < V_S$). As a result, all devices receive an amount of forward body bias equal to V_{dd}.

Fig.3 shows Sub Threshold Grounded Body (STGB) bias 12-transistor design . In this design, substrate of all NMOS and PMOS transistors are connected to ground. This type of substrate connection reduces the complexity of the design. All the NMOS transistors are at no body bias condition and all PMOS are at forward body bias condition. STGB design is less sensitive towards supply and ground noise than LVSB design. The substrate of the MOSFET is connected to the source and thus the VSB of the MOS transistor is always at zero voltage and thus it is known as No Body Bias (NBB) condition.

In NBB connection, threshold voltage of the MOSFET transistor is always constant. Fig.4 shows No Body Bias (NBB) 12 – transistor double edge triggered (DET) D flip-flop.

Simulation and analysis:

The 12-transistor DET D flip-flop designs are tested in 45nm technology using tanner tools v13.0. The proposed designs are technology independent.

Table I gives the comparison result of the conventional and proposed designs. From the table it is clear that the power and delay and thus the power-delay product of the 12-transistor designs with various substrate biasing techniques are better than the conventional 12-transistor design.

The No-Body bias design shows less power consumption than the contending LVSB and STGB designs.

Fig.5 shows waveform obtained from the simulation of all proposed DET D- Flip flops such as LVSB, STGB and NBB designs.

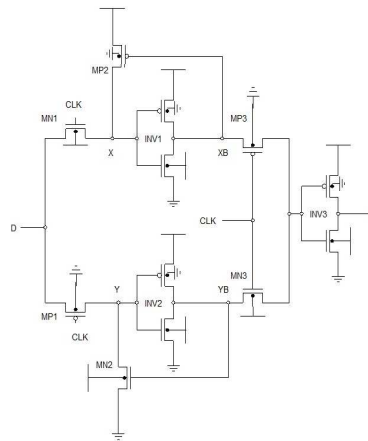


Fig. 2: LVSB 12-Transistor DET D-FF.

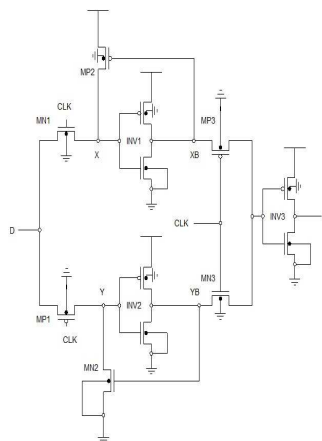


Fig. 3: STGB 12-Transistor DET D-FF.

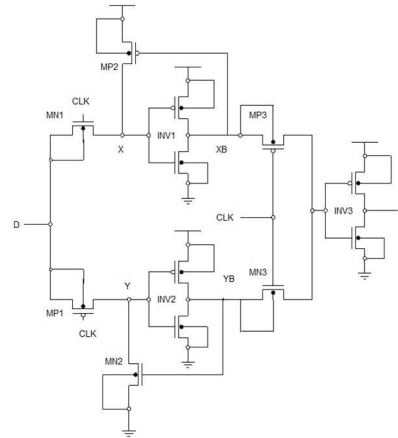


Fig. 4: NBB 12-Transistor DET D-FF.

Table I: Comparison of existing and proposed DET D-FFs.

| Design | Power (uW) | Delay (ps) | PDP (fJ) |
|---------------------|------------|------------|----------|
| Earliest Design [1] | 769.79 | 202 | 155.49 |
| LVSB | 695.13 | 186 | 129.29 |
| STGB | 662.79 | 174 | 115.32 |
| NBB | 653.33 | 162 | 105.83 |

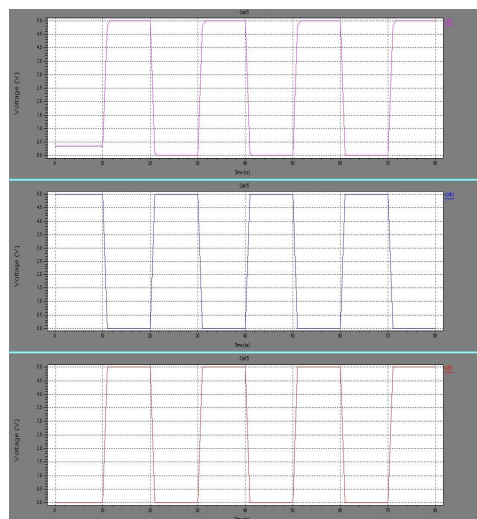


Fig. 5: Simulation Results of Proposed DET D-FFs.

Conclusion:

In low power applications delay and power consumption of the device are the main technological aspects to prefer a design over the other contending designs. The NBB design of DET D flip-flop shows better performance in terms of power dissipation and delay among designs discussed in this paper. Hence NBB design of Double edge triggered DET DFF design is suitable for portable application, as it is more speed and power efficient.

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