ISSN:1991-8178

Australian Journal of Basic and Applied Sciences

Journal home page: www.ajbasweb.com

Simulation Analysis of Nine Level MLI with Six Switches for THD Reduction

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ARTICLE INFO

Article history:
Received 12 January 2015
Accepted 1 May 2015
Available online 8 May 2015

Keywords:
MATLAB/SIMULINK, nine level inverter, POD, PWM, THD.

ABSTRACT

The various topology of cascaded multilevel inverter with considerable reduction in the number of switches and DC voltage sources have been analyzed in the literature. Due to more number of semiconductor switches, both the size and price of the multilevel inverter are increased. Hence a multilevel inverter topology with reduced number of switches has been proposed in this paper. The proposed topology is based on symmetrical multilevel inverter which produces 9 levels of output with the use of six switches, one diode and four DC voltage sources. In this work, the performance of the proposed nine level inverter with six switches using Phase Opposition Disposition Pulse Width Modulation(POD-PWM) technique is compared with that of conventional nine level inverter using Sinusoidal PWM technique to validate the effectiveness of the proposed topology. The digital simulation results obtained through MATLAB/SIMULINK software are compared in terms of Total Harmonic Distortion (THD) values for the above cases.

To Cite This Article: K. Srilatha and D. Murali., Simulation Analysis of Nine Level MLI with Six Switches for THD Reduction. ***Aust. J. Basic & Appl. Sci.,*** *9(21): 202-208, 2015*

INTRODUCTION

The consumption of power is projected to double by 2020 and an enormous amount of electricity is consumed by data centers every year. The world electricity generation is primarily dependant on fossil fuels such as coal, oil, natural gas, etc. One of the most promising sources of renewable energy for data centers is the sun's energy as it is clean and widely available. Sun's energy can be harnessed using solar photovoltaic (PV) modules which convert the solar radiation into direct current (DC) electricity. It is common that the DC electricity is converted into alternating current (AC) form so that it is compatible with existing power grid systems and most of the standard electrical appliances. Various types of inverters have been proposed in the past to provide the DC-to-AC conversion and multilevel inverter is one of them.

In modern times, the multilevel inverters (MLI) have become quite popular in the high power and medium voltage applications. In high power range, switching devices of a two level inverter cannot withstand the total DC link voltage. Multilevel inverters are able to overcome this problem by using more number of devices and sharing the DC link voltage among them. Not only does it help with voltage stress sharing but it also facilitates high quality power output due to more number of levels in the inverter output (Bayat, Z., E. Babaei, 2012). This, however, comes at the cost of increased number of components (switches, diodes, capacitors etc). This leads to an increase in system size, cost and control complexity (Babaei, E. and S.H. Hosseini, 2009).

In the year 1975, the concept of multilevel inverters was introduced. The unique structure of multilevel voltage source inverter provides a path to reach high voltages with low harmonics by using series connected synchronized switching devices or transformers. There are many existing topologies for the generation of multilevel output voltage. The main topologies used are cascaded H-bridge type, diode clamped type, flying capacitor type for the generation of less distorted output and each topology has a different mechanism for producing desired output (Rashid, M.H., 2004). Diode clamped type uses series capacitors in order to clamp output voltage. Whereas in flying capacitor model, the floating capacitors are used in order to produce output voltage. Whereas the cascaded type neither uses clamping diode nor flying capacitor. The multilevel inverters became very popular in medium and high power applications such as Adjustable Speed Drive's and static power compensators (Rodriguez, J., 2002).

The conventional cascaded H-bridge inverter has 16 switches (Babaei, E., 2014) to generate desired 9-

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level output voltage waveform and the proposed topology is aiming at the reduction of switches to a maximum extent a new topology is introduced with 6 switches for 9 level and this would be the least possible reduction (Booma, N., Nagisetty Sridhar, 2011). The new multi-level inverter is made out 6 switches, 1 diode and 4 D.C sources. Higher the output voltage level will lower the amount of Total Harmonic Distortion (Kang, D.W., D.S. Hyun, 2005). The effectiveness can be measured by simulating the circuit with POD PWM techniques using MATLAB/SIMULINK software.

II. Topologies:

(A) Conventional Topology:

This conventional topology is designed by using 4 dc sources and 4H-Bridge unit while each H Bridge consists of 4 switches, hence 16 switches is used to form nine level output voltage. The single H-bridge can produces an output of 3 levels as $+V_{dc}$, 0 and $-V_{dc}$. The output voltage expression for m level = (n+2)/2, where n is the number of switches in configuration. By cascading these H bridges in such a fashion to produce stepped 9 level staircase waveforms. Figure (1) represents the Conventional Cascaded H bridge inverter.

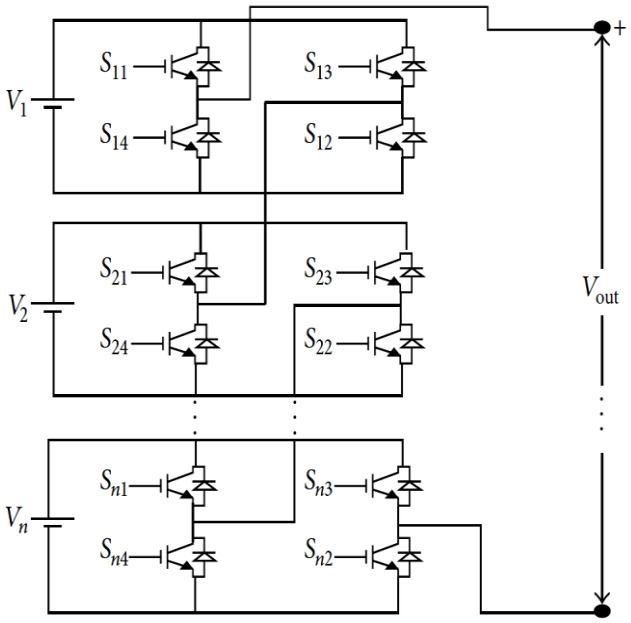

Fig. 1: Conventional Cascaded H-bridge Inverter.

When levels are increased, it requires more number of semiconductor switches and this is the main drawback in this topology. As a result, some alternations are to be made in the inbuilt structure in order to reduce the size and switch of the inverter.

(B) Existing Topology:

The general structure of the Modified cascaded multilevel inverter using 8 switches is shown in Figure 2.

This inverter consists of an H Bridge which consists of four switches and multi conversion cell which consists of four separate voltage sources (Vdc1, Vdc2, Vdc3 and V dc4), four switches and four diodes. To make output voltage in positive polarity with several levels, each source connected in cascade with other sources through a circuit consists of one active switch and one diode. To acquire both positive and negative polarity, only one H-bridge is connected with multi conversion cell. By turning on controlled switches S1 (S2, S3 and S4 turn off) the output voltage +1Vdc (first level) is produced across the load. Similarly turning on of switches S1, S2 (S3 & S4 turn off) +2Vdc (second level) output is produced across the load. Similarly +3Vdc levels can be achieved by turning on S1, S2, S3 switches (S4 turn off) and +4Vdc levels can be achieved by turning on S1, S2, S3 & S4 as shown in below Table 1.

Table 1: Switching scheme for nine level with 8 switches.

S.NO	S_A	S_B	S_C	S_D	S_1,S_2	S_3,S_4	Output Voltage
1.	ON	ON	ON	ON	ON	OFF	$+4V_{DC}$
2.	ON	ON	ON	OFF	ON	OFF	$+3V_{DC}$
3.	ON	ON	OFF	OFF	ON	OFF	$+2V_{DC}$
4.	ON	OFF	OFF	OFF	ON	OFF	$+V_{DC}$
5.	OFF	OFF	OFF	OFF	ON	OFF	0
6.	ON	OFF	OFF	OFF	OFF	ON	$-V_{DC}$
7.	ON	ON	OFF	OFF	OFF	ON	$-2V_{DC}$
8.	ON	ON	ON	OFF	OFF	ON	$-3V_{DC}$
9.	ON	ON	ON	ON	OFF	ON	$-4V_{DC}$

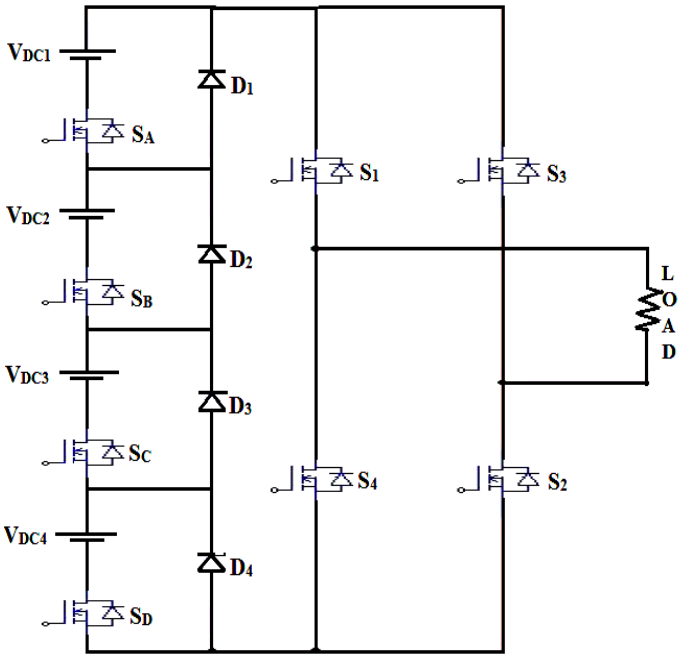

Fig. 2: Nine level inverter using 8 switches.

From the above table, it is observed that for each voltage level, among the paralleled switches only one switch is switched ON. The input DC voltage is converted into a stepped DC voltage, by the multi conversion cell, which is further processed by the H Bridge and outputted as a stepped or approximately sinusoidal AC waveform.

(C) Proposed Topology:

9-Level, 6 Switches Topology:

The Existing topology is modified further to design a proposed 9 level MLI inverter using only 6 switches. By using 6 switches and 4 dc sources with added one diode attaining 9 level, 6 switch configuration. The circuit thus obtained is simplest design compared to conventional and all other existing topologies. When comparing existing topology and conventional topology with this proposed topology, the arrangements of switches differ entirely. To obtain the unique pulse pattern switches should be triggered at the proper instant. This nine level inverter topology gives a higher quality output voltage waveform when it is compared with the existing topology. Thus a less distorted waveform is produced in its output voltage waveform of this proposed topology. For the positive half cycle, only two switches conducts at an instant. For negative half cycle, one switch and a diode conducts at an instant. The proposed nine level 6 switch topology is shown in figure (3).

Amount of THD produced is very much less when compared to the previous topologies and 4 dc sources are used for generation of 9 level results in less utilization of sources.

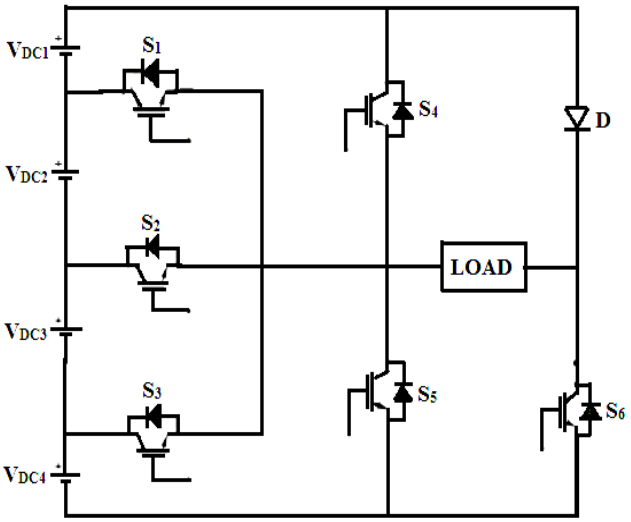

Fig. 3: Proposed nine level topology using 6 switches.

Table 2: Switching scheme for 9 level, 6 switches topology.

S.No.	S_1	S_2	S_3	S_4	S_5	S_6	D	Output Voltage
1.	OFF	OFF	OFF	ON	OFF	ON	OFF	+ $4V_{DC}$
2.	ON	OFF	OFF	OFF	OFF	ON	OFF	+ $3V_{DC}$
3.	OFF	ON	OFF	OFF	OFF	ON	OFF	+ $2V_{DC}$
4.	OFF	OFF	ON	OFF	OFF	ON	OFF	+ V_{DC}
5.	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
6.	ON	OFF	OFF	OFF	OFF	OFF	ON	- V_{DC}
7.	OFF	ON	OFF	OFF	OFF	OFF	ON	- $2V_{DC}$
8.	OFF	OFF	ON	OFF	OFF	OFF	ON	- $3V_{DC}$
9.	OFF	OFF	OFF	OFF	ON	OFF	ON	- $4V_{DC}$

III. Simulation Circuit and Its Specifications:

In the proposed 9-level MLI, the circuit is built of 6 MOSFET bi-directional switches and a diode. The load is resistive with a value of 10 ohms. Four 50-volt symmetric DC input voltages are used Figure (4) represent the simulation circuit of the proposed topology.

Note that in order to obtain the shaped 9-level output without distortion, MOSFET block parameters in MATLAB should vary according to the load used. Table (3) shows the simulation circuit parameters.

Table 3: Circuit Parameters.

S.No.	Parameters	Values
1.	Input Voltage	50V
2.	FET resistance	0.01ohms
3.	Internal diode resistance	10 kilo ohms
4.	Internal diode inductance	0 henry
5.	Load resistance	10 ohms

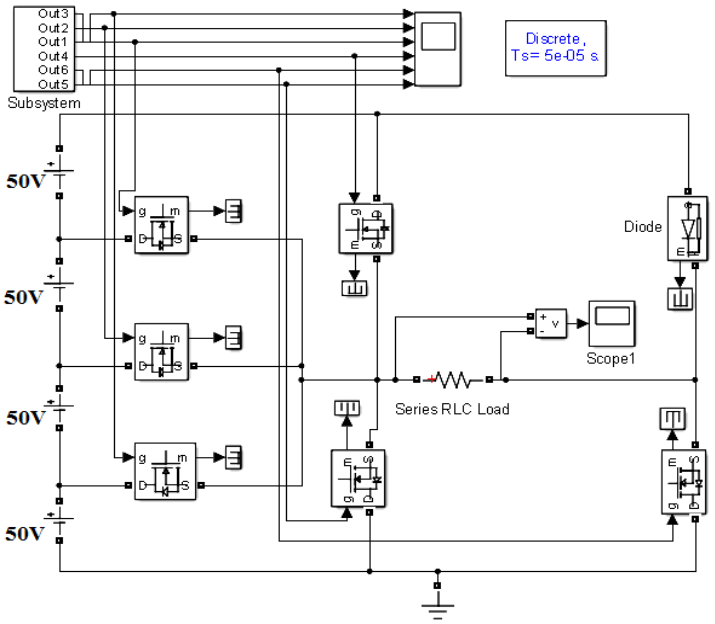

Fig. 4: Simulation circuit of proposed topology.

IV.PWM Generation:

To trigger the switches with appropriate pulse pattern to produce the desired 9-level output, the pulse generation circuit drive is very important. The level shifting Carrier Based PWM technique provides less harmonics when compared with phase shifting carrier based PWM, hence in this proposed circuit the level shifting carrier based PWM is preferred over it. Specifically, the new circuit design is analyzed with level shifting carrier based PWM, that is POD PWM as shown in Figure (5). . In POD or Phase Opposition Disposition for 7-level, 6 carriers are aligned as symmetric mirror images above and below the Zero reference axis.

The PWM generation circuit is the heart of the circuitry. One reference sine wave of amplitude 0.8 and frequency 50 Hertz is compared with C1 to C8 triangular carriers of frequency 1 KHz. If *m*-level needs to be synthesized, $(m-1)$ carriers are required. Whenever the reference sinusoid exceeds the carrier, instant pulses are generated to trigger the switch to ON state. Higher triangular carrier amplitude is taken as one.

V. Simulation Results and Discussions:

The conventional cascaded H-bridge inverter using 4 dc sources with 16 switches has the output waveform and FFT analysis is shown in figure (6) and (7). For the proposed topology using 4 dc sources with 6 switches, the simulation results are obtained for POD PWM technique as shown in Figure (9). The pulse generation for POD PWM technique is shown in Figures (8). The harmonic content have been found by taking the FFT analysis of the output waveform using POD PWM technique as shown in figures (10).

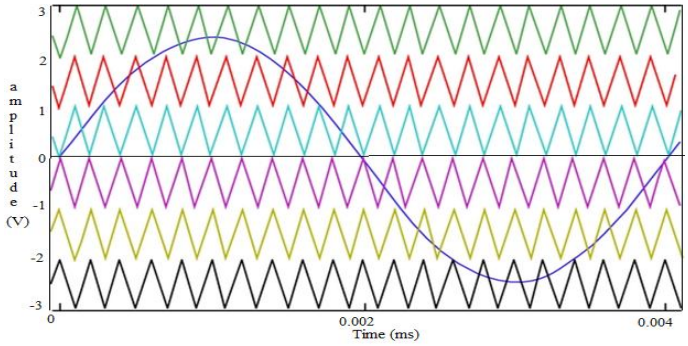

Fig. 5: POD PWM Technique.

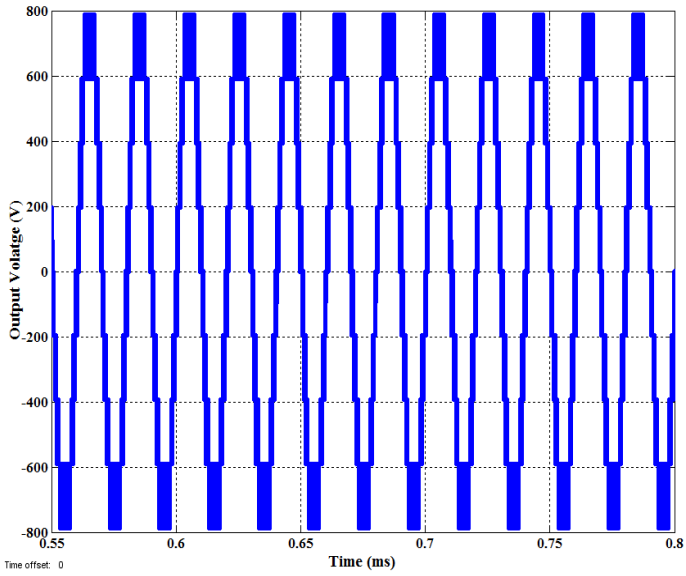

Fig. 6: Output Waveform for Conventional Cascaded H-bridge Inverter.

The POD PWM pulse signal generation has introduced by comparing the reference sine wave of amplitude 0.8 and frequency 50Hertz with triangular carrier waves C1 to C8 (each phase shifted by 45º) having the frequency of 1KHz.

The THD value comparison for conventional using SPWM and proposed topology using POD PWM techniques is tabulated as shown in table (3).

Table 3: Comparison of THD value.

MLI System	PWM Techniques	THD (%)
Conventional Cascaded H-bridge Inverter	Sinusoidal PWM	40.99
Proposed 9-level Inverter	POD	31.44

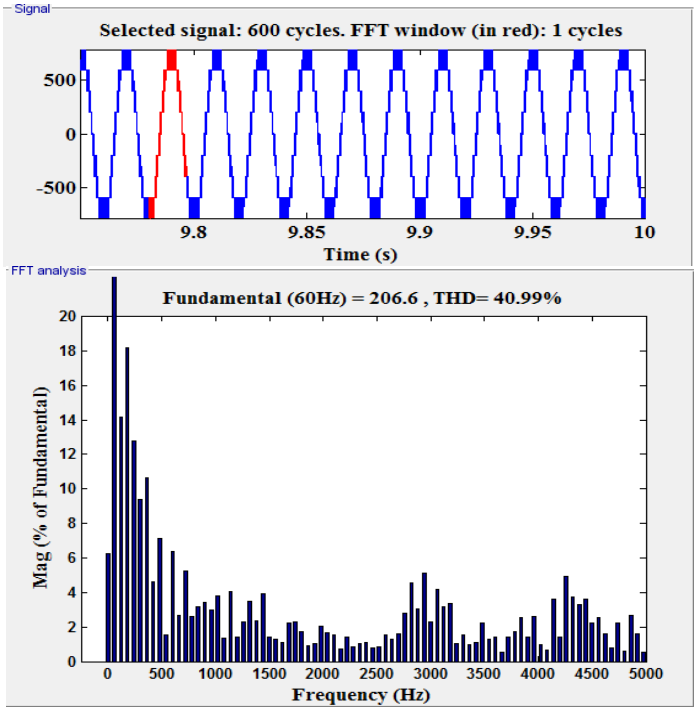

Fig. 7: FFT analysis for Conventional Cascaded H-bridge Inverter.

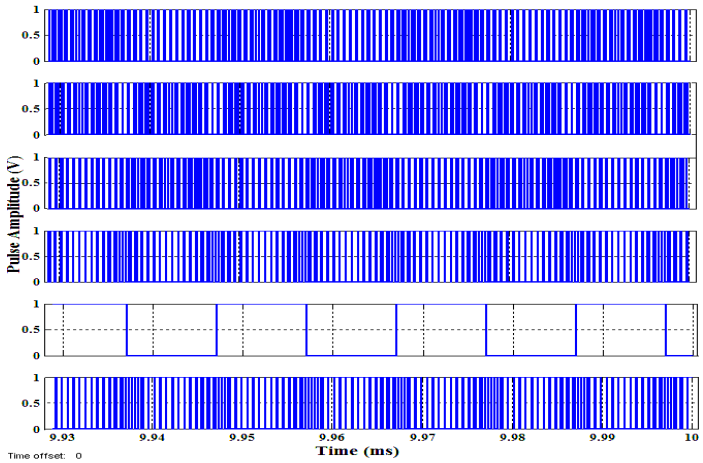

Fig. 8: Pulse Generation for 9 Level MLI using POD Technique.

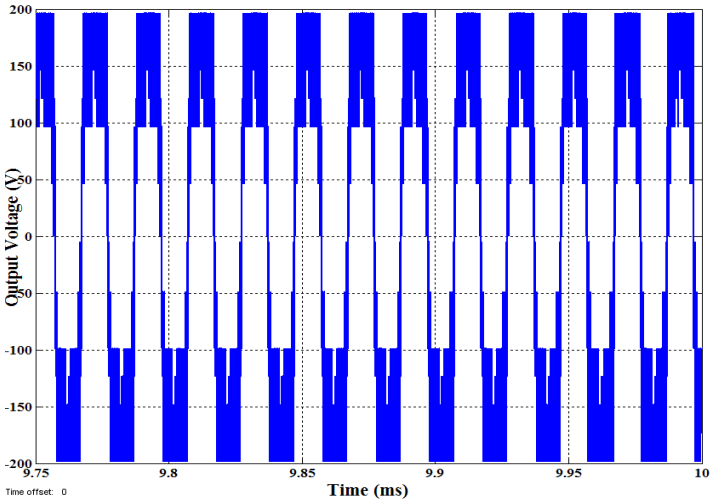

Fig. 9: Output Waveform for 9 Level MLI using POD Technique.

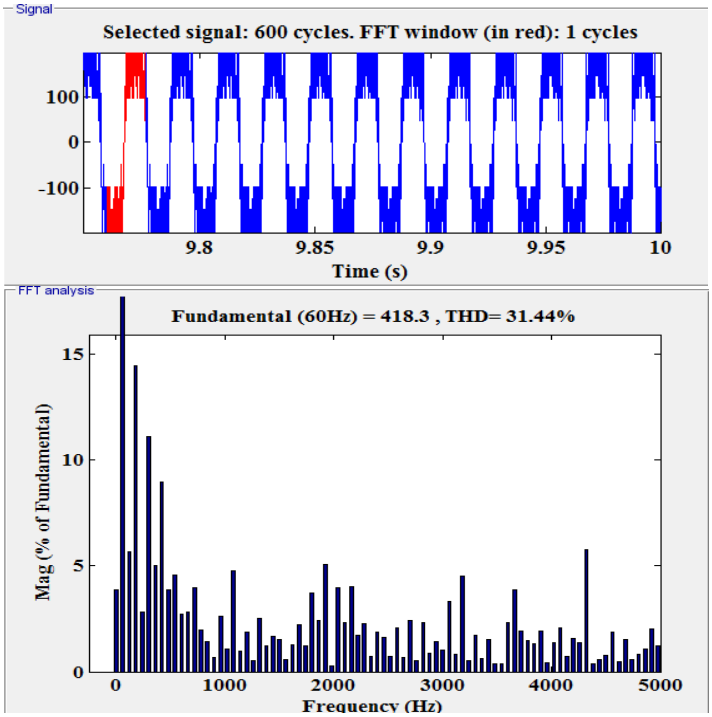

Fig. 10: FFT Analysis for Proposed Topology using POD PWM.

VI. Conclusion:

The proposed 9-level multilevel inverter topology is much superior than the conventional 9-level cascaded H-bridge topology in terms of using less number of switches, low switching loss, reduced total harmonic distortion (THD) and reduced cost. The MATLAB/SIMULINK software is used for modeling the circuit and the simulation of the proposed Nine level multilevel inverter is successfully done by using the POD PWM technique and the sinusoidal PWM technique for conventional Cascaded H-Bridge inverter. The total harmonic distortion produced by the proposed inverter is 31.44% only which is low when compared to the conventional H-bridge inverter having the THD value of 40.99%. Thus the proposed 9-level MLI has showed the best performance in terms of lower THD values as compared to conventional MLI topologies.

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