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Non-Isolated Interleaved DC-DC Converter With High Step-Down Conversion Ratio

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ABSTRACT

In this paper, high efficiency transformerless interleaved step-down conversion ratio dc-dc converter is proposed. Without using extremely short duty cycle, it is possible to achieve higher step-down ratio. This is obtained by allowing series charging and parallel discharging in the capacitors. The parallel discharge is brought about by a two-phase interleaved buck converter. The voltage divider circuit allows for storing energy in capacitors, enhancing the conversion ratio of active switches. Switching and conduction losses can be reduced as only lower voltage rated MOSFETs are used. This in turn improves the efficiency, which further increases when operation is carried out in a closed loop. Working principles of the proposed circuit are given and output of the circuit is obtained by using PSIM simulation software.

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INTRODUCTION

PWM boost DC-DC converters have been gathering much attention in a variety of power conditioning systems as renewable energy and distributed power generation. But most of the dc-dc converters include magnetic components which occupy high volume and weight in the converter, and also produce non-negligible losses. Thus, the PWM boost dc-dc converters require a substantial reduction of switching losses.

Buck type dc-dc converters are widely employed in the power electronics industry. Buck converters are perhaps most widely used dc-dc converters in the world because no other topology is as simple. Their applications range from low-power regulators to very high power step-down converters, which are characterized by a low number of components, low control complexity, and no insulation (Lu, D.D.C. and V.G. Angelides, 2009; Sun, K., 2010).

In the conventional buck topology, which uses a single active switch, the maximum voltage applied across the terminals of the semiconductors equals the input voltage, and hard switching is observed. These converters are often used in high-power and high-input-to-output voltage-ratio applications; however, the conventional buck-type topologies have low efficiencies because of high conduction losses due to high-voltage-rated devices and high switching losses. Furthermore, for high input voltages, the choice of

switches is limited, which leads to difficulty in selecting transistors or finding low-cost devices. The main parameters that impose limits on a buck converter with high-frequency pulswidth modulation (PWM) operation are the junction capacitances of the semiconductors, parasitic inductances, and the reverse recovery of the diodes. To minimize these effects, many soft-switching techniques are used.

The Buck converter is widely adopted for step-down dc-dc conversion when there is no isolation requirement. For output levels with high currents and low voltages, a synchronous MOSFET can replace the freewheeling diode in order to reduce the conduction loss.

The conventional IBC shown in Fig.1(a) because active switch devices suffer from the input voltage, high-voltage rated devices rated at the voltage of entry should be applied. High-voltage-rated devices are with poor characteristics such as high cost, large ON-resistance, large voltage drop, severe reverse recovery, etc. These limit the switching frequency of the converter and impact the power density improvement.

For high input and low-output voltage regulation applications, pursuing higher density and better dynamics. It is required operating at higher switching frequencies that will increase both switching and conduction losses. Consequently, the efficiency is further deteriorated. Also, it experiences an extremely

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short duty cycle in the case of high-input and low-output voltage applications.

To eliminate the drawbacks of the conventional IBC, many step-down converters have been proposed [7,13]. A quadratic buck converter is synthesized by cascading two dc-dc buck converters which have the voltage conversion ratios of two cascaded converters but with fewer switches. It can

operate with wider ranges of step-down conversion ratio than those of conventional single-switch converters without an extremely short duty ratio. By using the aforementioned converter, low-voltage MOSFETs have higher efficiency and better performance compared with the conventional buck converter.

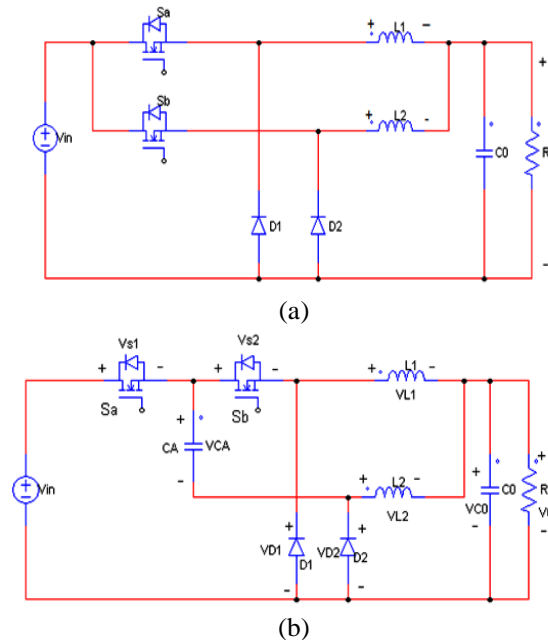


Fig. 1: configuration of (a)conventional IBC and (b)two-phase extended duty ratio IBC.

However, so many components are required for the use of IBC. In (Tsai, C.T. and C.L. Shen, 2009), an IBC with a single-capacitor turn-off snubber is introduced. Its advantages are that the switching loss associated with turn-off transition can be reduced, and a single coupled inductor implements the converter as two output inductors. However, it operates in discontinuous conduction mode (DCM), and all elements suffer from high-current stress, resulting in high conduction and core losses. In addition, the voltages across all semiconductor devices are still the input voltage. To reduce switching losses, an active clamp IBC is proposed in (Yao, K., 2005). In the converter, all active switches are turned on with zero-voltage switching (ZVS). Moreover, a high step-down conversion ratio can be obtained.

However, it requires additional passive elements and active switches, which increases the cost at low or middle levels of power applications. An IBC with two winding coupled inductors is introduced in (Yao, K., 2005; Lee, I.O., 2012). It can be operated in discontinuous conduction mode (DCM). The voltages across all semiconductor devices can be reduced by adjusting the turn ratio of the coupled inductors, and the switching losses can be reduced. Additionally, a high step-down conversion ratio can also be obtained. However, the leakage energy needs

to recycle. To deal with a small duty cycle of the IBC in high-input and low-output voltage regulation applications, a new extended duty ratio multiphase (Extended-D) topology has been proposed. The two-phase and four-phase versions of the topology have been discussed in (Lee, I.O., 2012). The two-phase extended duty ratio IBC is shown in Fig. 1(b). Extended duty ratio (ExtD) mechanisms are very efficient input voltage dividers which reduce the switching voltage and associated losses. However, the voltage stress of the input switch devices remains rather high.

Working Principle Of Proposed System:

The proposed non-isolated IBC is shown in Fig. 2. From Fig. 2, the proposed converter consists of two inductors, four active power switches, two diodes, and four capacitors. The main objectives of the four capacitors are twofold. First, they are used to store energy as usual. Second, based on the capacitive voltage division principle, they are used to increase the step-down conversion ratio. The operating principle of the proposed converter can be classified into four operation modes.

As the main objective is to obtain a high step-down conversion ratio and as such characteristic can only be achieved when the duty cycle is less than 0.5 and in DCM, hence the steady-state analysis is made

only for this case. However, in DCM, as there is not enough energy transfer from the blocking capacitors to the inductors, output capacitors, and load side, and as, consequently, it is not possible to get the charge

balance of the blocking capacitor, then the nice automatic uniform current sharing property will be lost, and additional current-sharing control between phases should be included under this condition.

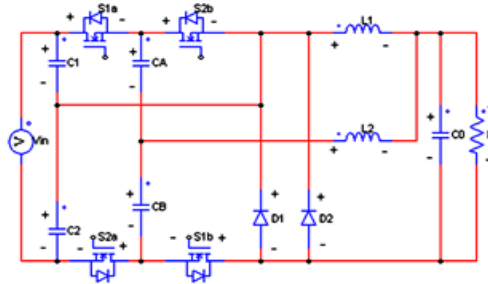


Fig. 2: Configuration of the proposed converter.

Mode 1 [$t_0 < t \leq t_1$]: During this mode, S_{1a} , S_{1b} , and D_1 are turned on while S_{2a} , S_{2b} , and D_2 are turned off. The corresponding equivalent circuit is shown in Fig. 3(a). From Fig. 3(a), one can see that, during this mode, current i_{L1} freewheels through D_1 , and L_1 is releasing energy to the output load. However, current i_{L2} provides two separate current paths through CA and CB . The first path starts from C_1 , through S_{1a} , CA , L_2 , CO and R , and then back to C_1 again. Hence, the stored energy of C_1 is discharged to CA , L_2 , and output load. The second path starts from CB , through L_2 , CO and R , and S_{1b} and then back to CB again.

In other words, the stored energy of CB is discharged to L_2 and output load. Therefore, during this mode, i_{L2} is increasing, and i_{L1} is decreasing. Also, from Fig. 3(a), one can see that V_{C1} is equal to V_{CA} plus V_{CB} due to conduction of S_{1a} , S_{1b} , and D_1 .

Mode 2 [$t_1 < t \leq t_2$]: During this mode, S_{1a} , S_{1b} , S_{2a} , and S_{2b} are turned off. The corresponding equivalent circuit is shown in Fig. 3(b). From Fig. 3(b), one can see that both i_{L1} and i_{L2} are freewheeling through D_1 and D_2 , respectively. Both V_{L1} and V_{L2} are equal to $-V_{CO}$, and hence, i_{L1} and i_{L2} decrease linearly. During this mode, the voltage across S_{1a} , namely, V_{S1a} , is equal to the difference of V_{C1} and V_{CA} , and V_{S1b} is clamped at V_{CB} . Similarly, the voltage across S_{2a} , namely, V_{S2a} , is equal to the difference of V_{C2} and V_{CB} , and V_{S2b} is clamped at V_{CA} .

Mode 3 [$t_2 < t \leq t_3$]: During this mode, S_{2a} , S_{2b} , and D_2 are turned on while S_{1a} , S_{1b} , and D_1 are turned off. The corresponding equivalent circuit is shown in Fig. 3(c). From Fig. 3(c), one can see that, during this mode, current i_{L2} is freewheeling through D_2 , and L_2 is releasing energy to the output load. However, current i_{L1} provides two separate current paths through CA and CB . The first path starts from C_2 , through L_1 , CO and R , D_2 , CB , and S_{2a} and then back to C_2 again. Hence, the stored energy of C_2 is discharged to CB , L_1 , and output load.

The second path starts from CA , through S_{2b} , L_1 , CO and R , and D_2 and then back to CA again. In other words, the stored energy of CA is discharged to L_1 and output load. Therefore, during this mode, i_{L1} is increasing, and i_{L2} is decreasing.

Mode 4 [$t_3 < t \leq t_4$]: For this operation mode, its operation is the same as that of mode 2. During this mode, S_{1a} , S_{1b} , S_{2a} , and S_{2b} are turned off. The corresponding equivalent circuit is shown in Fig. 3(b). From Fig. 3(b), one can see that both i_{L1} and i_{L2} are freewheeling through D_1 and D_2 , respectively. Both V_{L1} and V_{L2} are equal to $-V_{CO}$, and hence, i_{L1} and i_{L2} decrease linearly.

During this mode, the voltage across S_{1a} , namely, V_{S1a} , is equal to the difference of V_{C1} and V_{CA} , and V_{S1b} is clamped at V_{CB} . Similarly, the voltage across S_{2a} , namely, V_{S2a} , is equal to the difference of V_{C2} and V_{CB} , and V_{S2b} is clamped at V_{CA} .

Steady State Analysis of proposed system:

In order to simplify the circuit analysis of the proposed converter, some assumptions are made as follows.

- All components are ideal components.
- The capacitors are sufficiently large such that the voltage across them can be considered constant. Also, assume that $C_1 = C_2$ and $CA = CB$.
- The system is under steady state and is operating in CCM with the duty ratio being lower than 0.5 for high step-down conversion ratio purposes.

Conversion Ratio:

Referring to Fig. 3(a) and (c), from the volt-second relationship of inductor L_1 (or L_2), one can obtain the following relations:

$$(V_{CB} - V_O)D = V_O(1 - D) \quad (1)$$

$$(V_{CA} - V_O)D = V_O(1 - D) \quad (2)$$

Also, from the equivalent circuits in Fig. 3(a) and (c), voltages V_{C1} , V_{C2} , V_{CA} , and V_{CB} can be derived as follows:

$$V_{CA} = V_{CB} = \frac{V_{in}}{4} \tag{3}$$

$$V_{C1} = V_{C2} = \frac{V_{in}}{2} \tag{4}$$

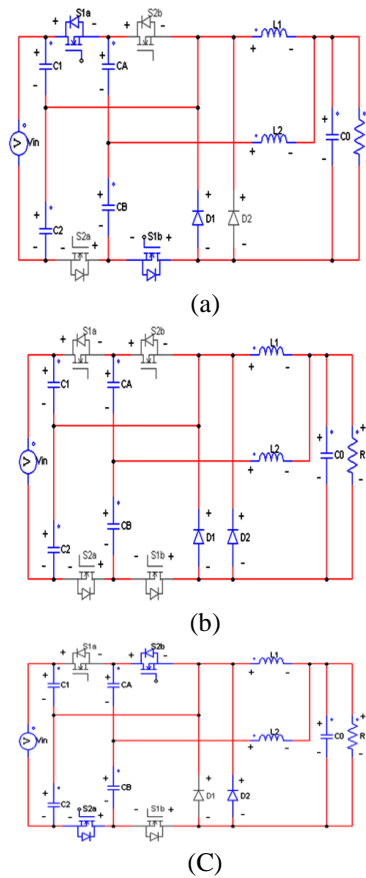


Fig. 3: Equivalent circuit of the proposed converter(a) Mode 1. (b) Modes 2and 4. (c) Mode 3.

The output voltage can be obtained by substituting (4) into (1) or (2) as follows:

$$V_o = \frac{D}{4} V_{in} \tag{5}$$

Thus, the conversion ratio *M* of the proposed converter can be obtained as follows:

$$M = \frac{V_o}{V_{in}} = \frac{D}{4} \tag{6}$$

By using Eq. 5, the output voltage of the proposed converter for respective duty cycle can be determined. Similarly, step-down conversion ratio of proposed converter can be determined using Eq. 6.

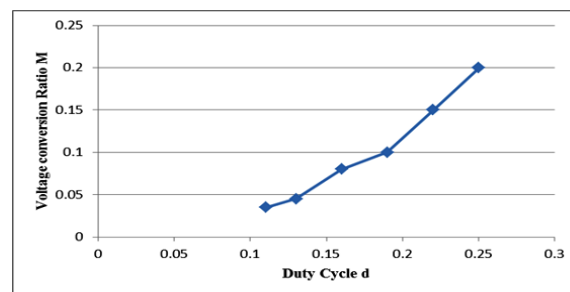


Fig. 4: Graphical representation of Conversion ratio with respect to duty cycle.

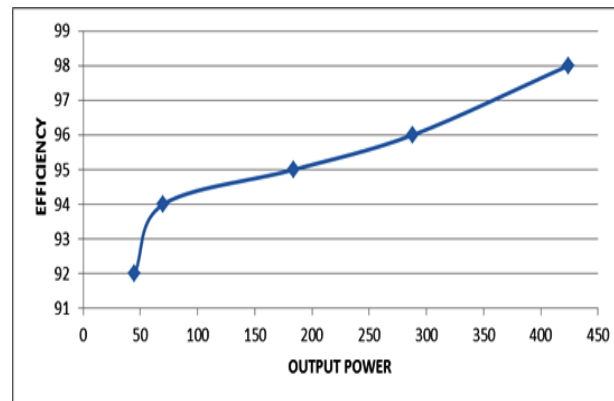


Fig. 5: Graphical representation of Efficiency Vs Output power.

Fig. 4 shows the graphical representation of the proposed converter can achieve a higher step-down conversion ratio than the other system. Here, as duty cycle increases, the conversion ratio also increases and also the output voltage is increases. It is

calculated by (6). Fig. 5 shows the graphical representation of efficiency Vs input voltages. As the input voltage increases the input power and also the output power increases. Due to this the efficiency of the converter is increased.

Table I: Conversion ratio for various duty cycle.

S.No	Duty cycle(D)	Input voltage(v_{in})	Output Voltage(V_o)	Conversion ratio (M)
1	0.11	400	14	0.035
2	0.13	400	18	0.045
3	0.16	400	22	0.08
4	0.19	400	23	0.1
5	0.22	400	24	0.15
6	0.25	400	25	0.2

Table I shows the conversion ratio for various duty cycle. This table gives the graphical representation of conversion ratio with respect to duty cycle which is shown in Fig. 4.

Table II Measured efficiency for various input voltage

Table II: shows the measured efficiency for various input voltage. This gives the graphical representation of Efficiency Vs Output power which is shown in Fig. 5.

Input voltage(v_i)	Input current(I_{in})	Input power (P_{in})	Output voltage (V_o)	Output current (I_o)	Pout	η
200	0.12	48	25	1.8	45	92%
250	0.13	65	32	2.2	70	94%
300	0.21	168	51	3.6	183	95%
350	0.278	278	64	4.5	288	96%
400	0.36	432	77	5.5	423	98%

B. Component Parameters Of The Proposed System:

The following components are used to implement the simulation of proposed converter.

Components	Specification
Input voltage	400 VDC
Output voltage	25 VDC
Power rating	400 W
Switching frequency	40 kHz
Inductors (L_1, L_2)	250 μ H
Blocking Capacitors (C_A, C_B)	10 μ F
Input Capacitors (C_1, C_2)	250 μ F
Output Capacitors (C_0)	250 μ F

IV. Simulation Results and discussion:

Simulation' in general terms can be defined as the representation of a system in its realistic form. Before implementing a new project, by simulation, one can see the effect of various parameters or components on the output

accordingly change them to get a desired output. PSIM denotes Power Simulation. PSIM is simulation software specifically designed for the analysis and design of power electronics and control circuits. It provides a powerful simulation and design environment for power supplies,

analog/digital control and electric motor drives. Simulink is the waveform display and post-processing program for PSIM. It provides a

powerful environment to display and analyze simulation results.

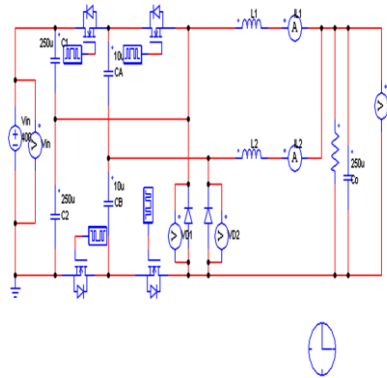


Fig. 6: Simulation diagram of proposed converter under open loop.

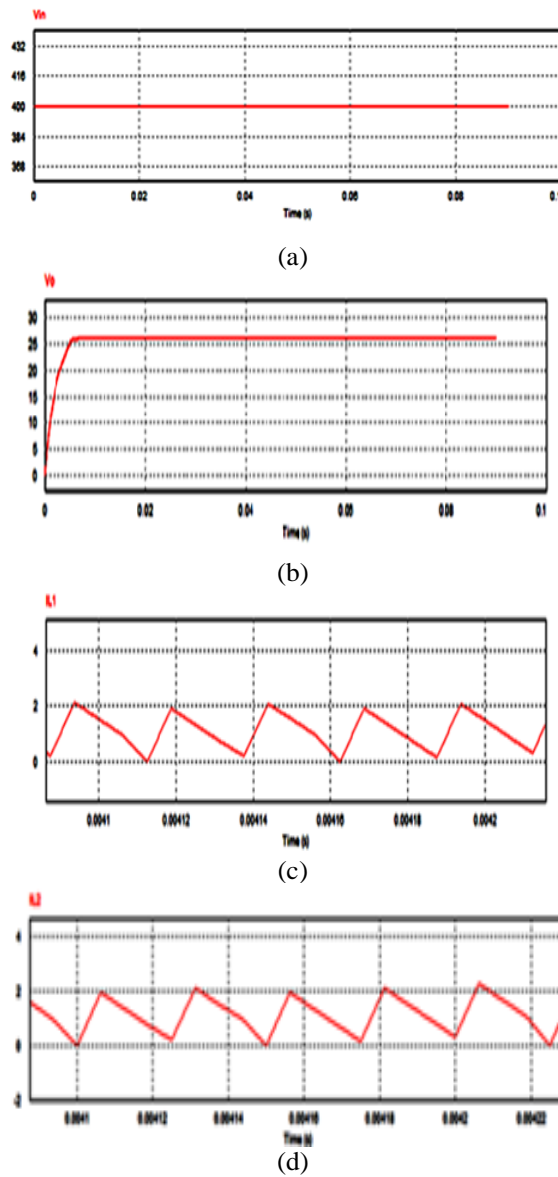


Fig 7: Simulated waveforms of proposed converter under open loop system (a) Input voltage waveform (b) Output voltage waveform (c) Waveform of inductor current I_{L1} (d) Waveform of output current I_{L2} .

Simulation waveforms of proposed converter under open loop system is shown in Fig. 7. Step down output voltage $V_0 = 25$ V for input voltage V_{in}

$= 400$ V is shown in Fig. 7(a) and Fig. 7(b) respectively. Also, the inductor current of L_1 and L_2 is illustrated in Fig. 7(c) and Fig. 7(d).

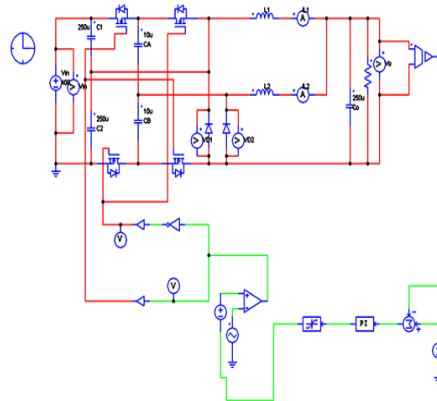


Fig. 8: Simulation diagram of proposed converter under closed loop.

Fig.8 shows the simulation diagram of proposed converter under closed loop system. Since this

operation is carried out in closed loop, it increases the efficiency.

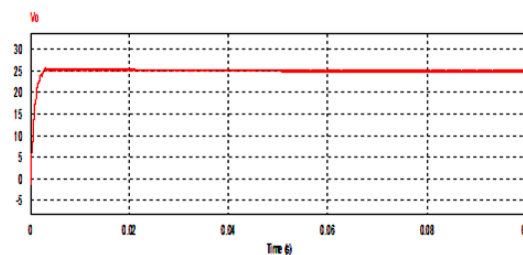


Fig. 9: output voltage waveform of proposed converter under closed loop system.

The above fig.9.shows the output voltage($V_0=25$ V) waveform of proposed converter under closed loop system for input voltage 400V.Thus, high efficiency is achieved by both open loops and closed loop system. Also, due to interleaved operation the conversion ratio of proposed converter increases when compared to the conventional configuration.Furthermore, the losses are reduced due to transformerless operation.

closed loop get the output voltage very quickly.Hence, the closed loop system is more efficient than the open loop system.The operation principles and simulation results of the proposed converter are presented in this paper. The proposed converter is very suitable for applications requiring high step-down conversion ratio.

Conclusion:

In this paper, High efficiency transformerless interleaved step-down conversion ratio dc-dc converter is proposed.Increase in step-down conversion ratio is one of the main objectives that has been achieved in this paper with the use of new voltage divider circuit that has blocking capacitor which acts as energy storage device. The reduced switching and conduction loss due to use of low voltage rated MOSFETs further enhances the efficiency, which has been proved through simulation results.In open loop system the output voltage 25 VDC is achieved at the setting time $t_s=0.0087$.In closed loop system the output voltage 25 VDC is achieved at settling time $t_s=0.0037$.So,when compare to open loop system the

REFERENCES

- Lu, D.D.C. and V.G. Angelides, 2009. "Photovoltaic-battery-powered dc bus system for common portable electronic devices," IEEE Trans. PowerElectron., 24(3): 849–855.
- Sun, K., L. Zhang, Y. Xing and J.M. Guerrero, 2010. "A distributed control strategy based on dc bus signaling for modular photovoltaic generations systems with battery energy storage," IEEE Trans. Ind. Electron., 26(10): 3032–3045.
- Larico, H.R.E. and I. Barbi, 2012. "Three-phase push-pull dc-dc converter: Analysis, design, experimentation," IEEE Trans. Ind. Electron., 59(12): 4629–4636.
- Lin, R.L., C.C. Hsu and S.K. Changchien, 2009. "Interleaved four-phase buck-based current source with isolated energy-recovery scheme for

electrical discharge machine,” IEEE Trans. Power Electron., 24(7): 2249–2258.

Garcia, C., P. Zumel, A.D. Castro and J.A. Cobos, 2006. “Automotive dc-dc bidirectional converter made with many interleaved buck stages,” IEEE Trans. Power Electron., 21(3): 578–586.

Rodrigues, J.P., S.A. Mussa, M.L. Heldwein and A.J. Perin, 2009. “Three level ZVS active clamping PWM for the dc-dc buck converter,” IEEE Trans. Power Electron., 24(10): 2249–2258.

Chen, Y.M., S.Y. Teseng, C.T. Tsai and T.F. Wu, 2004. “Interleaved buck converters with a single-capacitor turn-off snubber,” IEEE Trans. Aerosp. Electron. Syst., 40(3): 954–967.

Tsai, C.T. and C.L. Shen, 2009. “Interleaved soft-switching coupled-buck converter with active-clamp circuits,” in Proc. IEEE Int. Conf. Power Electron. Drive Syst., 1113–1118.

Yao, K., Y. Qiu, M. Xu and F.C. Lee, 2005. “A novel winding-coupled buck converter for high-frequency, high-step-down dc-dc conversion,” IEEE Trans. Power Electron., 20(5): 1017–1023.

Yao, K., M. Ye, M. Xu and F.C. Lee, 2005. “Tapped-inductor buck converter for high-step-down dc-dc conversion,” IEEE Trans. Power Electron., 20(4): 775–780.

Lee, I.O., S.Y. Cho and G.W. Moon, 2012. “Interleaved buck converter having low switching losses and improved step-down conversion ratio,” IEEE Trans. Power Electron., 27(8): 3664–3675.

Sung-Sae, L., 2014. “Step-down converter with efficient ZVS operation with load variation,” IEEE Trans. Ind. Electron., 61(1): 591–597.