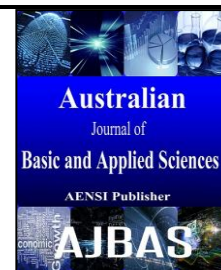




ISSN:1991-8178

Australian Journal of Basic and Applied Sciences

Journal home page: www.ajbasweb.com



A Zero-Voltage Switching Full Bridge Dc–Dc Converter For Hybrid Electric Vehicle

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ARTICLE INFO

Article history:

Article Received : 12 January 2015

Revised: 1 May 2015

Accepted: 8 May 2015

Keywords:

Battery charger, capacitive filter, dc–dc converter, full-bridge, plug-in hybrid electric vehicle (PHEV), resonant converters, zero-voltage switching (ZVS).

ABSTRACT

In this project, a novel zero-voltage switching full-bridge converter with trailing edge pulse width modulation and capacitive output filter is presented. The target application for this study is the second stage dc–dc converter in a two stage 1.65 Kw on-board charger for a plug-in hybrid electric vehicle. For this application, the design objective is to achieve high efficiency and low cost in order to minimize the charger size, charging time, and the amount and the cost of electricity drawn from the utility. A detailed converter operation analysis is presented along with simulation and experimental results. In comparison to a benchmark full-bridge with an LC output filter, the proposed converter reduces the reverse recovery losses in the secondary rectifier diodes.

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To Cite This Article: K. Kannan and Dr. I.Gnanambal., Intelligent Classification Techniques for Effective. *Aust. J. Basic & Appl. Sci.*, 9(21): 127-133, 2015

INTRODUCTION

PLUG-IN hybrid electric vehicle (PHEV) is a hybrid electric vehicle with rechargeable batteries that can be restored to full charge by connecting the vehicle plug to an external electric power source. In recent years, PHEV motor drive and energy storage technology have developed at a rapid rate in response

To expected market demand for PHEV's. Battery chargers are other key components required for the emergence and acceptance of PHEV's. For PHEV applications, most commonly on-board chargers are used. The most common charger power architecture includes an ac–dc converter with power factor correction (PFC) followed by an isolated dc–dc converter. Galvanic isolation is required in onboard battery chargers in order to meet the double fault protection for the PHEV user safety. Many high-efficiency full-bridge dc–dc converter solutions have been proposed that are potential candidates for the isolated dc–dc converter in a PHEV charger. The phase-shifted zero voltage switching (ZVS) pulse width modulated (PWM) dc-to-dc full-bridge converter was presented. ZVS for the switches is realized by using the leakage inductance of the transformer in addition to an external inductor and the output capacitance of the switch. Although various improvements have been suggested for this converter, these solutions increase the component count and suffer from one or more disadvantages

including, a limited ZVS range, high voltage ringing on the secondary side rectifier diodes, or duty cycle loss. A new complementary gating scheme for the full-bridge dc-to-dc PWM converter is presented. This gating scheme requires an additional zero-voltage transition circuit to achieve ZVS for all the switches for a wide variation in the load current. Current fed topologies with capacitive output filter inherently minimize diode rectifier ringing since the transformer leakage inductance is effectively placed in series with the supply side inductor. In addition, high efficiency can be achieved with ZVS, in particular, the trailing edge PWM full-bridge gating scheme proposed in is an attractive solution to achieve ZVS. In this paper, a novel PWM ZVS full-bridge dc–dc converter with the trailing edge pulse width modulation and capacitive output filter is presented. The paper is organized as follows: section II presents the converter operating modes. Results in Section III. The conclusions are presented in Section IV.

Operating Principles:

The proposed ZVS full-bridge converter topology is illustrated in Fig. 1. The converter primary side circuit consists of a traditional full-bridge inverter. However, rather than driving the diagonal bridge switches simultaneously, the lower switches (Q3 and Q4) are driven at a fixed 50% duty cycle and the upper

Switches (Q1 and Q2) are PWM on the trailing edge. Although the proposed converter can operate in either discontinuous conduction mode (DCM), Boundary Conduction Mode (BCM), or

continuous conduction mode (CCM), only the DCM and BCM modes are circuit operation in all three modes is given next. The detailed circuit operation in all three modes is given next.

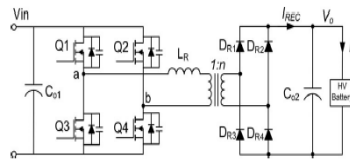


Fig. 1: PWM ZVS full-bridge converter topology with a capacitive output filter.

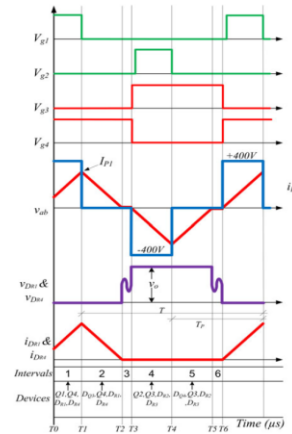


Fig. 2: Typical operating waveforms to illustrate the operation of the ZVS full-bridge converter in a DCM mode.

This converter has six operating intervals for DCM, BCM, or CCM. The operating intervals are determined by the ON/OFF states of the four primary switches. Detailed operating waveforms are provided for DCM in Fig. 2, for BCM in Fig. 3 and for CCM in Fig. 4. In the analysis that follows, the power semiconductor switches have been modeled with

parallel diodes and parasitic capacitances. All parasitic capacitances in the circuit including winding and heat sink capacitance have been lumped together with the switch output capacitance. The output rectifiers are considered ideal, and the external resonant inductor also includes the transformer leakage inductance.

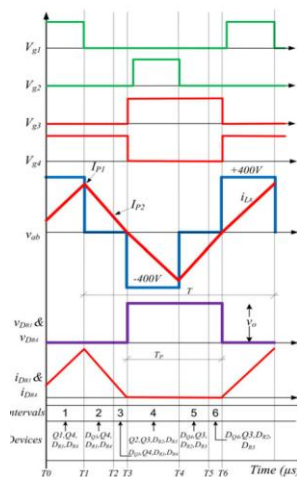


Fig. 3: Typical operating waveforms to illustrate the operation of the ZVS full-bridge converter in a BCM mode.

A. Interval 1 (T0–T1):

Referring to Fig 2.2, during Interval 1 (T0–T1), switches Q1 and Q4 are ON and Q2 and Q3 are OFF.

This is a power transfer interval, and the primary current flows through Q1, the resonant inductor LR, transformer primary and Q4, as illustrated in Fig.2.2.

The rate of rise of the current (di/dt) through LR is proportional to the difference between the input voltage V_{in} and the output voltage V_o . During this mode, power flows to the output through rectifier diodes DR1 and DR4 and also energy is stored in LR. The resonant inductor current $I_{LR}(t)$ using initial condition $I_{LR}(0) = 0$.

B. Interval 2 ($T1-T2$):

1) Case (a): Operating in DCM: Referring to Fig 2.3, interval 2 begins after switch Q1 turns OFF, as determined by the PWM duty cycle. Since the current flowing in the primary side cannot be interrupted instantaneously, it finds an alternate path and flows through the parasitic switch capacitances of Q3 and Q1 which discharges the

node “a” to 0 V and then forward biases the body diode D3.

Energy stored in the resonant inductor LR assists in transferring energy from the lower to the upper bridge MOSFET capacitances. Therefore switches Q3 and Q4 always achieve ZVS with the help of the energy stored in the resonant inductor LR for nearly the entire load current I_o range. During this interval the energy stored in LR is transferred to the output. The primary resonant inductor LR maintains the current, which circulates around the path of D3, resonant inductor LR, transformer primary and Q4, as illustrated in Fig2.6. The rate of the downslope of the current through LR is proportional to the output voltage V_o .

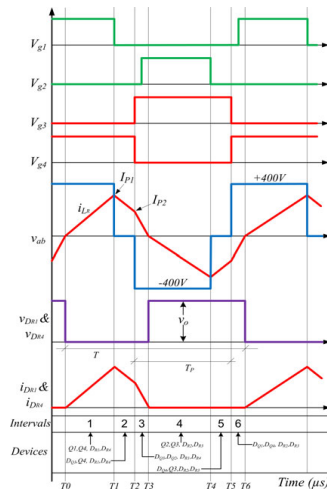


Fig. 4: Typical operating waveforms to illustrate the operation of the ZVS full-bridge converter in a CCM mode.

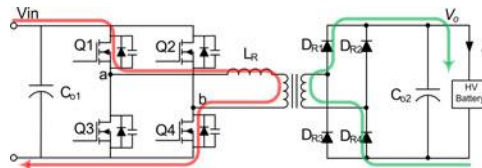


Fig. 5: Equivalent circuit for Interval 1 ($T0-T1$) for DCM, BCM and CCM.

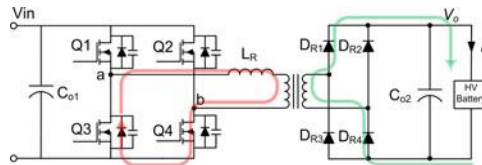


Fig. 6: Equivalent circuit for Interval 2 ($T1-T2$) for DCM, BCM, and CCM and Interval 3 ($T2-T3$) for BCM.

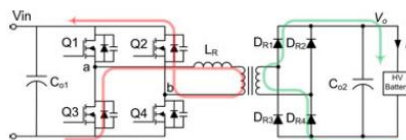


Fig. 7: Equivalent circuit for Interval 3 ($T2-T3$) for CCM.

At T_2 , the energy stored in LR is transferred to the output and the current becomes zero and the rectifier diodes DR1 and DR4 turn OFF. The resonant inductor current $i_{LR}(t)$ using initial condition $i_{LR}(0) = IP_1$.

2) Case (b): Operating in BCM and CCM: Referring to Fig 2.7. The only difference in BCM or CCM as compared to DCM during Interval 2 is that the current through the resonant inductor does not reach zero at T_2 and the rectifier diodes DR1 and DR4 are ON. At the end of this interval, $i_{LR}(t) = IP_2$. Fig. 2.6 illustrates the equivalent circuit for this interval.

C. Interval 3 (T_2-T_3):

1) Case (a): Operating in DCM: Referring to Fig. 2.7, during this interval no power is transferred to the secondary. Accordingly, this interval is a

passive interval. In this interval, the parasitic capacitances of the rectifier diodes resonate with LR. This resonance appears across the rectifier diodes DR1 and DR4 as illustrated in Fig.2.7 For this interval, current in the resonant inductor remains zero ($i_{LR} = 0$).

2) Case (b): Operating in BCM: During this interval the resonant inductor current continues to circulate around the path of D3, resonant inductor LR, transformer primary and Q4, as illustrated in Figs.2.3 and 2.6. The rate of the downslope of the current through LR is proportional to the output voltage V_o . At T_3 the entire energy stored in LR is transferred to the output and the current becomes zero and the rectifier diodes DR1 and DR4 turn OFF. The resonant inductor current $i_{LR}(t)$ using initial condition $i_{LR}(0) = IP_2$.

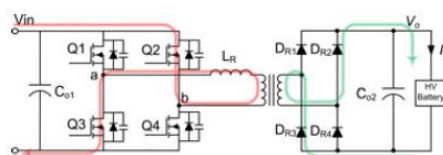


Fig. 8: Equivalent circuit for Interval 4 (T_3-T_4) for DCM, BCM, and CCM.

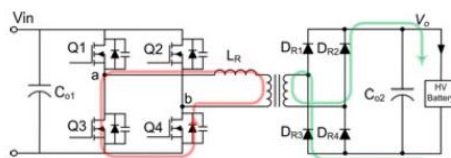


Fig. 9: Equivalent circuit for Interval 5 (T_4-T_5) for DCM, BCM and CCM and Interval 6 (T_5-T_6) for BCM.

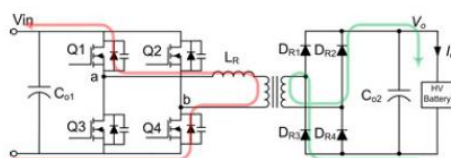


Fig. 10: Equivalent circuit for Interval 6 (T_5-T_6) for CCM.

D. Interval 4 (T_3-T_4) through Interval 6 (T_5-T_6):

Intervals 4 to 6 are the negative equivalent of Intervals 1 to 3 as shown in Figs. 8-10.

RESULT AND DISCUSSION

A. System Parameters:

The system parameters are used given in the following Tabulation I. The performance of the converter designed was evaluated using PSIM. Simulations were run varying the output voltage and output load conditions. Circuit parameters, including component stresses, obtained from theoretical analysis and simulation are listed in Table II at $V_{in} = 400$ V and $I_o = 5.5$ A and 0.7 A. As can be

observed, there is a close match between the theoretical prediction and simulation results.

B. Voltage and Current Waveforms:

Fig11 provide the experimental waveforms for DCM and BCM, respectively. It is noted that the MOSFET Q3 turns ON with ZVS and turns OFF with ZCS and the current through the resonant inductor also has a very low di/dt .

Fig 12 provide the voltage across and current through rectifier diode DR3 in DCM and BCM, respectively. The voltage across the diode is clamped to the output voltage, at $V_o = 300$ V, and the di/dt through the diode is low enough to minimize the

losses due to reverse recovery issues inherent with ultrafast diodes.

Table I: system parameters.

S.no	Parameters	Value
1	Input DC Voltage	400 V
2	Efficiency	96 %
3	Output DC Voltage Range	150-450 v
4	Maximum output DC current	5.5 A
5	Maximum output power	1.65 KW
6	DC-DC switching frequency	100KHz

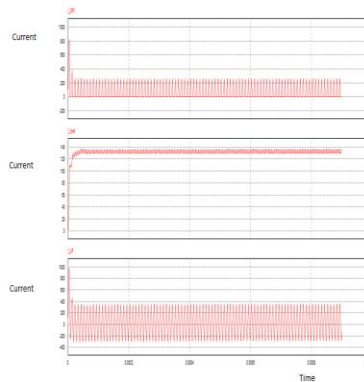


Fig. 11: DCM output current waveforms.

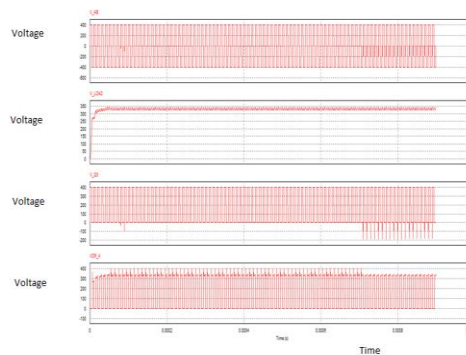


Fig. 12: DCM output Voltage waveforms.

Waveforms of the ripple free output voltage and current are provided in Fig 11 at $V_o = 300\text{ V}$ and $I_o = 5.5\text{ A}$. Figs.13 and 14 provide the experimental waveforms for DCM and BCM, respectively. It is

noted that the MOSFET Q3 turns ON with ZVS and turns OFF with ZCS and the current through the resonant inductor also has a very low di/dt.

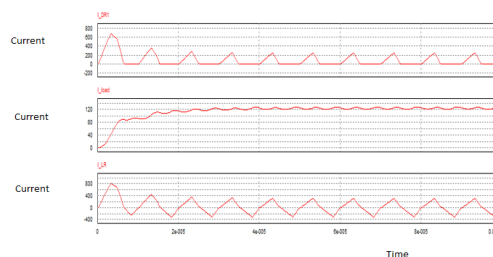


Fig. 13: BCM output Current waveforms.

Fig4.3 provide the voltage across and current through rectifier diode DR3 in DCM and BCM, respectively. The voltage across the diode is clamped

to the output voltage, at $V_o = 300\text{ V}$, and the di/dt through the diode is low enough to minimize the losses due to reverse recovery issues inherent with

ultrafast diodes. Waveforms of the ripple free output voltage and current are provided in Fig.4.3 at $V_o = 300$ V and $I_o = 5.5$ A. and $P_o = 1.2$ kW. High efficiency

over the entire load range is achieved with this solution.

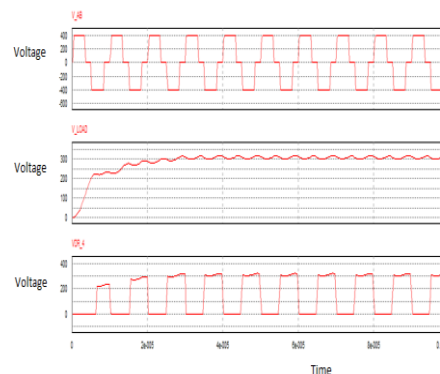


Fig. 14: BCM output Voltage waveforms.

Conclusion:

A novel ZVS full-bridge dc-dc converter with capacitive output filter has been presented for application in PHEV battery charging. The detailed operating intervals in DCM, BCM, and CCM were presented in addition to a step by step design procedure, simulation results and experimental waveforms. The proposed topology achieves soft switching for the full-bridge primary switches, naturally clamps the voltage across the output rectifier to the output voltage and the current through the rectifier diodes has a low di/dt , which helps to minimize reverse recovery losses. It has been shown that the converter achieves an overall peak efficiency of 95.7% at $V_o = 400$ V with inexpensive hyper fast diodes. Finally, the converter performance in terms efficiency is superior to its inductive output filter counterpart.

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