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New Improved High Speed Low-Power Tail To Tail Comparator Design

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ABSTRACT

Modern communication and signal processing is dependent on the high speed, area efficient and ultra low power consumption of the Analog-to-Digital converters (ADC) to a very large extent. In today's world everything is digitized but signals are analog in nature. So there is a need to convert the analog signal into digital signal. Nowadays devices like high-speed ADCs, operational amplifiers play a major role in technology and they are widely used for high speed and less delay applications and a majority core is provided for low power aspects. The power consumed in these devices can be minimized by provoking against the smaller aspect size processes. Despite, as we provoke against the smaller aspect size the non-idealizes and the variations of the process can extremely change the overall device performance. Hence there is a need of efficient comparators in order to improve the delay and speed efficiency. A new design of double tail comparator was intended based on the circuit of the conventional dynamic double tail comparator and the circuit is customized in terms of speed, delay, low power and high frequency even for inadequate supply voltages. Beyond aggravating the circuit but by enumerating some transistors. The positive feedback mechanism during the latch regeneration process is been enhanced to reduce delay time and is compared with the new regenerative tail to tail comparator design in terms of area on chip power utilization, delay consideration and speed. For a higher frequency the power consumption is less for the proposed double tail comparator design which keeps on getting better with every rising frequency. The maximum frequency of operation is also increased along with lesser delay which is significant considering the need of high speed devices.

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INTRODUCTION

Dynamic comparators are the most widely used essential block in the ADC converters because these dynamic comparators provide full swing digital output at a briefer time extent, less delay and lesser static power consumption. But these comparators results in drastic power dissipation and produces a huge input-referred offset voltage. Adjacent inverters provide a positive feedback system in these dynamic comparators which provides a smaller differential digital output voltage in full scale. The latch offset voltages arise due to the device mismatches which occur as result of the threshold voltage, node and load capacitance. These mismatches restraints the efficiency of these dynamic comparators. Due to this fact, the latch offset value is the most decisive circuit specifications of the latched comparator. A lesser mismatch can be attained by using larger devices during the latching stage. Improvement in mismatch provides increased delay due to the slow regeneration process and power dissipation. The latch offset voltage can be further reduced practically by implementing pre-amplifier in the circuit which leads to regenerative latching stage.

Analog-to-digital converter depends upon lower delay, lesser power dissipation, prominent slew rate, improved speed, less power consumption and offset. The performance specifying blocks in an analog to digital converter are generally the comparators and the center-stage amplifiers. Among this the comparators are the most essential block with ultimate importance. Hence the different design concern related to Delay, speed, Power consumption, gain, resolutions and offset are of foremost importance.

Comparator is the most essential block in almost all the analog-to-digital converters (ADCs). Great speed analog to digital converters such as Successive Approximation ADCs, flash ADCs desires ultimately efficient speed CMOS

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technologies. These sub-micrometer technologies endure from inadequate supply voltages specifically when the threshold voltages are not scaled for the devices to satisfy the criteria as similar as the power supply of the advanced CMOS technology. Thus the design of the high speed and less delay comparators is ultimately complex when the smaller voltage is given as the input. In another words in the modern CMOS process the speed is attained by using larger sized transistors. These large transistors are needed in order to satisfy the supply voltage minimization and it also ensures that adequate die spacing and power supply is required. Apart from this the operation of lower supply voltage brings about finite common-mode input range. It is the most extensive parameter in frequent Analog to Digital Converters architectures, such as Successive Approximation ADCs. Numerous methods such as supply boosting techniques proffered by Ay (2012) which consist of the body-driven transistors based on 10 bit supply boosting Successive Approximation ADC to satisfy the need of supply voltages. Amin *et al*. (2007) introduced a dual oxide processes to overcome latch comparator offset mismatch which occurs due to load mismatches. Babayan *et al*. (2014) designed a double tail comparator to meet the design challenges of the low power technology by handling higher power supplies effectively.

Blalock (2010) proffered a Body-driven mechanism in order to eliminate the threshold voltage condition. In this technique the driven MOSFET behave as the depleted transistor. In contempt of the advantages this technique suffers from the serious disadvantages that it has lower transconductance. To overcome this issues a deep n-well fabrication process is required in order to make the transistors work in the transistor driven mode. Goll *et al*. (2009) designed a 65nm CMOS technology comparator by modifying the latch circuit in order to attain a frequency of about 700 MHz at 0.6V. The two techniques termed as boosting and bootstrapping was proffered By Mesgarani *et al*. (2010) to augment the clock or the supply reference voltage in order to locate the switching and the input range problems. These are the efficient techniques but there occurs issues in terms of reliability specifically in CMOS sub micrometer technologies. Pedro *et al*. (2008) proffered a regeneration technique to reduce kickback noise that occurs during the regeneration process.

Many new design structures have been developed as the base for the technological improvement. These design techniques avoids circuit complexity and stacking of transistors.

Regenerative Comparator:

Comparators are apparently the second most extensively used electronic device after the amplifier abstraction in this world. In most of the analog to digital convertors, comparator acts as an essential block. The Regenerative comparator is composed of three stages such as the preamplifier stage, decision making or the positive feedback stage and finally the differential amplifier or the output buffer stage.

The preamplifier stage in the comparator is used to amplify the input signal in order to enhance the comparator input to create a larger differential voltage, which helps the comparator to decide and isolates the input and prevents the comparator from the kick back noise effect. The decision making stage is used to determine the larger differential input stage. The output buffer amplifies and it converts the analog information into the digital form.

Previous Work Circuit:

Double tail Comparator is derived from the conventional dynamic comparators to satisfy the need of the low voltage applications. The main purpose of the double tail comparator is to speed up the latch regeneration mechanism for improving the power, speed and to lower the delay.

A. Operation of Conventional Double Tail Comparator:

The operation of the Conventional double tail comparator occurs in two phase i) Reset Phase ii) Comparison Phase. Initially the clock is set to 0, tail current 1 and tail current 2 are in off state, m3 and m4 transistor are in on state which pulls both the nodes fn and fp to vdd. When clk=1, both mtail1 and mtail2 are in on state and both m3 and m4 are in off state, fn and fp are pre-charged to vdd. Input voltage is given fn and fp starts to discharge depending on the input voltage. In decision making phase there are two cases. i) Vinp > Vinn and ii) Vinn > Vinp.

When vinp > vinn, fn start to discharge faster since m2 provides more current and this causes mc1 transistor to turn on.mc1 transistor remains on till fn is completely discharged and this mc1 pulls fp node to vdd. When fn starts to charge to vdd and fp is discharging. Differential voltage is calculated if there occurs large differential voltage then latch regeneration occurs. In vinn > vinp, the vice versa process occurs. n this m1 provides more current and the mc2 transistor turns on and the latch regeneration process occurs.

The advantages of the conventional double tail comparator are high input impedance, improved speed and delay and in this comparator switches are additionally added in order to prevent the comparator from the static current leakage. The comparator delay, speed and the power consumption can be further decreased by enumerating two transistors in parallel to increase

the load during regeneration and this causes increase in differential voltage which provides the digital output faster with less delay and improved speed.

B. Delay Analysis:

Delay analysis is made by calculating the Discharge Delay (to) which occurs during the discharge phase of the nodes fn and fp and the Latching Delay (tlatch) which occurs during latch regeneration condition. This latch regeneration is responsible for delay improvement.

$$t_0 = \frac{C_L|V_{thp}|}{I_2} = \frac{2C_L|V_{thp}|}{I_{tail}}$$

$$t_{latch} = \frac{C_L}{g_{m,eff}} . ln\left(\frac{\Delta V_{out}}{\Delta V_o}\right) = \frac{C_L}{g_{m,eff}} . ln(\frac{\frac{V_{DD}}{2}}{\Delta V_o})$$

By using this discharge and latching delay the total delay is analyzed for the double tail comparator.

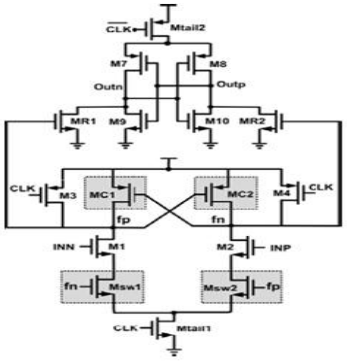

Fig. 1: Schematic Diagram of double tail comparator.

Proposed Circuit:

The New Regenerative dynamic tail to tail comparator operation is similar to the operation of the new double tail comparator. This is the new contingent idea the structure is similar to the new double tail comparator but additionally two transistors are enumerated in parallel beyond aggravating the design. New Tail to Tail comparator is designed in order to improve speed and delay.

A. Operation of Proposed Tail to Tail Comparator:

The operation of the Tail to Tail comparator occurs in two phase i) Reset Phase ii) Comparison Phase. Initially the clock is set to 0, tail current 1 and tail current 2 are in off state, m3 and m4 transistors are in on state which pulls both the nodes fn and fp to vdd. When clk=1, tail current1 and tail current 2 are in on state, m3 and m4 transistors are in off state fn and fp are pre-charged to vdd. Input voltage is given fn and fp starts to discharge depending on the input voltage.

In decision making phase there are two cases. i) Vinp > Vinn and ii) Vinn > Vinp. When vinp > vinn, fn start to discharge faster since m2 provides more current and this causes mc1 transistor to turn on.mc1 transistor remains on till fn is completely discharged and this mc1 pulls fp node to vdd. When fn starts to charge to vdd and fp is discharging. Differential voltage is calculated if there occurs large differential voltage then latch regeneration occurs. In vinn > vinp, the vice versa process occurs in this m1 provides more current and the mc2 transistor turns on and the latch regeneration process occurs.

In this additionally two transistors are connected in parallel to increase the load for latch regeneration. Adding transistors in parallel to the tail to tail comparator the Offset will be low and the delay will be reduced. Parallel connected dynamic latch is used as the load to the first stage to increase the voltage difference. Delay will be more in cascade connection when compared to parallel connection. Hence delay is very much reduced and the speed is increased.

B. Delay Analysis:

Delay analysis for tail to tail comparator is computed by calculating the Discharge Delay (to) which occurs during the discharge phase of the nodes fn and fp and the Latching Delay (tlatch) which occurs during latch regeneration condition. This latch regeneration is responsible for delay improvement.

$$t_0 = \frac{C_L|V_{thp}|}{I_2} = \frac{2C_L|V_{thp}|}{I_{tail}}$$

$$t_{latch} = \frac{C_L}{g_{m,eff+mR1,R2}} . ln\left(\frac{\Delta V_{out}}{\Delta V_o}\right) = \frac{C_L}{g_{m,eff+mR1,R2}} . ln(\frac{\frac{V_{DD}}{2}}{\Delta V_o})$$

By using this discharge and latching delay the total delay is analyzed for the tail to tail comparator.

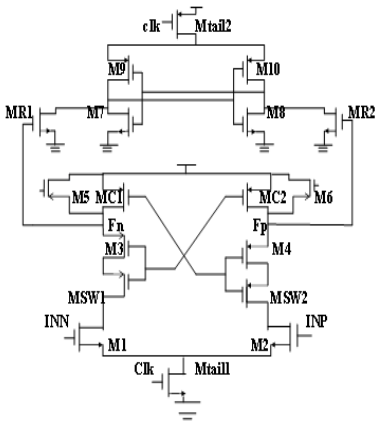

Fig. 2: Schematic Diagram of Tail to Tail Comparator.

Application Enhancement:

In Application enhancement the designed comparator circuit is implemented. Since the comparator is the most essential block of the Analog to Digital converter and Phase Generator. The designed Tail to Tail comparator is implemented in ADC and Phase generator and the Delay, speed and yield range for the different application is attained. Finally circuit enhancement is obtained.

A. ***Successive Approximation ADC:***

Successive Approximation ADC is one of the types of analog to digital converter. It converts the analog information to digital form. In this approximation technique time of conversion is constantly maintained throughout the process and it depends on the total number of bits in the digital representation. The primary aim of the analog to digital converter is to approximate the unknown input analog value against the digital n-bit value, each bit at a time, starting from the most significant bit. Thus the ADC works by dividing the voltage value successively by half.

(i) Initially the MSB = 1, followed by three 0 bits. This digital representation is compared with the analog input value.

(ii) If the given input value is greater than the digital form then the MSB value remains 1 and the second most significant bit becomes 1, if the input is lesser, then the MSB bit will be equal to 0 and the second bit will become 1.

(iii) Analysis is done to decide whether to reset the second MSB bit or to retain. Now the third bit becomes 1 and the same operation is followed for LSB and finally the converted digital representation is attained.

This method provides an effective binary search method which gives an N-bit digital output in N clock periods. Hence for 8 bit approximation, the converter requires only 8 bits for conversion process. This shows that the converter provides the required digital value by approximating each bit at a time. The output from the digital to analog converter is given as the input to the non inverting terminal of the comparator and the unknown input analog signal is the other input of the comparator. The output of the comparator activates the successive approximation analog to digital converter.

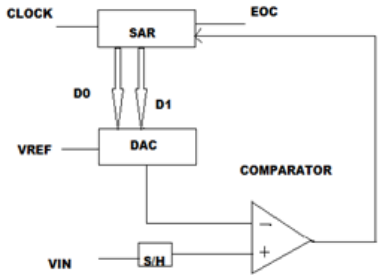

Fig. 3: Successive Approximation ADC.

When the START command is applied, the SAR sets the MSB of the digital signal, while the other bits are made zero, so that the trial code becomes 1 followed by zeros. For example, for an 8-bit A/D converter the trial code is 10000000. The output of the SAR is converted into analog equivalent Vr and gets compared with the input voltage Vi. If Vi is greater than that of the D/A converter output, then the trial code 10000000 is less than the correct digital value. The MSB is retained as 1 and the lower significant bit is made as 1 and the testing is repeated. If the analog input Vi is now less than the

D/A converter output, then the value 11000000 is greater than the exact digital equivalent. Therefore, the comparator resets the second MSB to zero and proceeds to the next most significant bit. This process is repeated for all the remaining lower bits in sequence until all the bits positions tested. The EOC signal is sent out when all the bits are scanned and the value of D/A converter output just crosses Vi.

B. Phase Generator:

The designed Tail to Tail comparator is implemented in Phase Generator. The Comparator is the fundamental building block of phase generator it is used to generate various frequencies and compares the analog signal and provides the digital output. The circuit enhancement is achieved and maximum improvement in speed and delay is obtained.

RESULTS AND DISCUSSION

The performance of the proposed Tail to Tail comparator is compared with the conventional comparators for the analysis of the speed, Delay and power. The speed and delay is very much improved when compared to the conventional circuits.

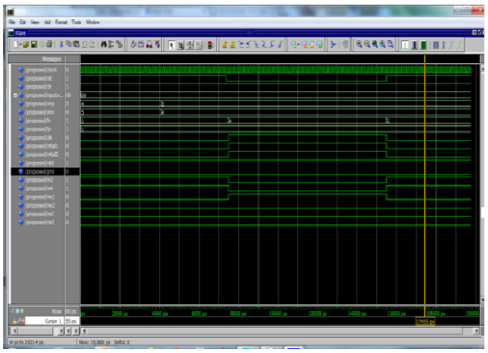

Fig. 4: Simulation Output for Comparator.

Conclusion:

The comparator circuits for high-speed ADCs have been investigated. The designs are mainly optimized for the low propagation time, minimal input resolution and minimal circuit area. The delay analysis for the dynamic comparators were analyzed and two similar structures of the conventional dynamic and the conventional double-tail dynamic comparators were compared to design a new improved high speed Tail to Tail comparator based on delay analysis. This analysis provides the comparator with the improved voltage, power and delay capability. Thus the performance of the device is readily improved. Modern CMOS technology proved that the speed, delay and power consumed is decreased to a larger extent when compared to the conventional ones. Simulation results show that both comparator give low offset voltage. Auto zeroing technique was used in proposed comparator which reduces the offset voltage further. In this comparator the delay, power and the speed is analyzed which is very much reduced when compared to the conventional comparators. MOSFET switch are added in series and additionally two transistors are enumerated in parallel beyond aggravating the design. This parallel connected latch acts as load of first stage and this increases the differential voltage which very much reduces the delay and increases the speed of the circuit and the preamplifier current source had significantly reduced the static power dissipation of the preamplifier. In this the delay is very much reduced but it can be further reduced by increasing the load for further improvement.

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