Australian Journal of Basic and Applied Sciences, 9(11) May 2015, Pages: 741-748

ISSN:1991-8178

Australian Journal of Basic and Applied Sciences

Journal home page: www.ajbasweb.com

Power Analysis In Nbti And Oxide Degradation Sensor

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ARTICLE INFO

Article history:
Received 12 March 2015
Accepted 28 April 2015
Available online 1 June 2015

Keywords:
Negative Bias Temperature Instability, Gate Oxide Degradation, Power consumption, Area Efficiency, Reliability.

ABSTRACT

Energy efficiency is the supreme design concern in many low power application. Sensors enable high volume data collection and monitoring of degradation mechanism to guide dynamic control schemes and warn of impending device failure. Scaling, temperature and area are the important factor in the IC manufacturing. The degradation mechanism have effect on the above mentioned factors. In the presence of these degradation mechanisms, it is difficult to ensure the reliability of ICs over their lifetimes. Lifetime evaluation is difficult to improve the effectiveness of this structure which makes it easier to collect and process it with less number of devices. To solve this critical reliability issue, compact low power sensor was provided without sacrificing the reliability of CMOS. Existing sensors provide the reliability upto particular level of temperature and large power consumption. Thus the proposed sensor will overcome the drawbacks of exiting sensors. By providing control and monitoring over the CMOS without sacrificing the reliability.

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To Cite This Article: Dr.M.Ramkumar Prabhu, K.Venkateswara Rao, Dr.A.Rajalingam and U.T.Sasikala., Power Analysis In Nbti And Oxide Degradation Sensor. ***Aust. J. Basic & Appl. Sci.,*** *9(11): 741-748, 2015*

INTRODUCTION

MOSFETs have been the major force behind the tremendous development in the microelectronics industry, yielding unprecedented scientific and technological advancements. This fundamental impact of MOSFETs has been facilitated by the phenomenal properties of both Si and its oxide, SiO2. The ability to integrate various circuit components on the same substrate and the scalability of the dimensions of the MOSFETs have allowed increasing density of transistors with higher speed and computational capability along with lower power consumption and cost per MOSFET. The progress in MOSFET based microelectronics has not been without its problems. The operating requirements of ICs put stress on the devices, leading to performance and reliability problems.

MOSFETs and particularly the oxide degrade during the device operation and cannot retain its original specifications. One general degradation type is defect generation in the oxide bulk or at the Si-SiO_2 interface over time. The defects can increase leakage current through the gate dielectric, change transistor metrics such as the threshold voltage or result in the device failure due to oxide breakdown. The trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area.

Technology scaling improves the performance of the transistor but at the same time compromises its reliability. Since scaling mainly targets high performance applications, to further boost the performance the supply voltage is not reduced in the same proportion as the critical dimensions. As a result electric field increases across the transistor gate-oxide, channel, and interconnects which exacerbates transistor degradation mechanism such as gate-oxide wear-out, Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), and Electro migration. In older process nodes (above 100nm) the rate of degradation process was low enough that it did not raise concern over end of life-time failures.

II. Negative bias temperature instability:

NBTI measurement techniques involve highly invasive experimental setups that require specialized equipment and/or access to individual transistors under test. In this section, to summarize a number of these and other less invasive methods along with their benefits and drawbacks.

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The sensitivity of device lifetime to operating conditions has increased, dynamic control schemes that modulate the voltage, sleep state, and workload of processing elements and circuitry in large systems (Prashant Singh, 2011; Borkar, S.Y., 2005) have been proposed. Dynamic control further complicates a priori reliability qualification and makes a case for on-chip structures to be used for real-time estimation of device and circuit degradation (Keane, J., T 2007; Kim, T.H., 2008). Since the degradation is a statistical process, hundreds or even thousands of sensors are required to estimate bounds on overall chip performance degradation (Karl, E., 2008). Hence it is essential that the sensors are small with low power consumption. *A. Measurement Techniques*

Chen *et al.* were the first to report the partial recovery of pMOS transistor strength when stress conditions are removed, which results in longer device lifetimes [10]. Those authors used an improved direct-current current-voltage (DCIV) measurement technique to monitor the formation of interface traps (N_{it}).This method allowed them to observe a correlation between ΔV_{tp} and ΔN_{it}, but required the sensitive monitoring of base and collector currents in a gate-controlled parasitic BJT of a MOSFET. This paper gives the brief explanation of DCIV method.

On-the-fly techniques that minimize the recovery effect have been examined in. Denais *et al.* proposed a measurement technique in which the stress voltage is kept quasi-constant while the linear drain current is measured to monitor device degradation. However, it still requires extra equipment for the accurate measuring of device current under test which limits its application for run-time NBTI monitoring in actual products. The core circuit for detecting frequency degradation consists of two free-running ring oscillators and a phase comparator. During the stress period, one of the ring oscillators is stressed, while the other remains unstressed.

More recently, Fernandez *et al.* proposed on-chip circuits for the reliable measurement of device degradation due to AC NBTI stress up to the gigahertz range. In this work, I-V curves of single transistors under test, as well as voltage transfer curves of inverters placed under stress, were used to extract. No mention is made of the time required for each reading, and such measurements are not typically made in the timescale needed to avoid unwanted NBTI recovery. The authors also use on-the-fly techniques. This technique describes the wafer probing method. The authors assert that a high frequency stress signal can be reliably applied to the devices under test, and utilize this information to extract data regarding the frequency dependency of NBTI aging.

In Kim *et al.* (2008) introduced an aging monitor which is capable of taking fast and precise frequency degradation measurements by detecting the beat frequency of a pair of simple inverter-based ring oscillators (ROSCs), where one is placed under accelerated stress conditions by raising the supply voltage. However, in this circuit, only half of the PMOS devices in the ROSC are stressed at one time, and frequency degradation is the measured parameter. That frequency change cannot easily be mapped to a threshold degradation due solely to NBTI, since simply raising the supply will cause a combination of accelerated NBTI, positive bias temperature instability in NMOS devices, hot-carrier stress, and possibly other degradation mechanisms to impact circuit performance simultaneously.

The aging monitor technique have a phase comparator which is used as a core circuit for detecting the beat frequency. Any offset in the phase comparator simply shifts the start and end point of the measured time, without affecting the period. In addition, the measured period of the beat frequency is more sensitive to the degradation in ring oscillator frequency than the resolution of the phase comparator.

Ketchen *et al*. also used the beat frequency idea with a new ROSC stage designed specifically to facilitate "pure" NBTI stress (Vs = Vd ;Vg $\leq$ 0 V) (Ferńandez, R., 2006). The authors of this paper did not mention any attempt to execute fast measurements to avoid recovery, and it may be difficult to know the precise stress in their setup if the gate current in the DUTs is comparable to other leakage sources in the ROSC. The authors rely on the fact that the DUTs' drain and source terminals are grounded through all of these other leakage paths when VCC=GND=0 V, which may not be accurate, particularly with a large stress voltage.

III. Nbti sensor design:

A. Existing Design:

The aim of most previous work in NBTI measurement has been in the direction of characterizing NBTI. In the past, researchers have used invasive probing methods that require direct access to the device-under-test (DUT) to monitor currents. One large class of work (Denais, M., 2004; Kumar, S., 2006) employs a direct current probing approach. Ring oscillator based structures have been proposed in (Keane, J., 2007; Keane, J., 2009).

Negative Bias Temperature Instability is a significant reliability concern for digital and analog circuits in current generation CMOS technology. NBTI occurs in negatively biased (VGS < 0V) PMOSFETs at elevated temperatures and is a consequence of interface trap generation at the Si/oxide interface shown in figure3.1. In conventional Si MOSFETs, the transistors are annealed in hydrogen ambient to passivate the dangling Si bonds during manufacture.

This traditional method proved to be an

effective solution to the interface trap instabilities for decades; however the continuing MOSFET miniaturization trends, (i.e., aggressive oxide thickness scaling leading to higher oxide field and process modifications such as nitridation of oxides to prevent Boron diffusion from p+ poly gate) and higher operation temperatures (due to power dissipation from the circuits or ambient conditions) accelerate bond-breaking at the interface over time during the device operation.

The traps increase the threshold voltage, reduce the channel mobility due to scattering and induce parasitic capacitances in the transistors. Overall, the drain current degrades over time and parametric reliability becomes a significant concern. NBTI has become a forefront reliability issue recently, however, it has been known for decades. Present day operating conditions of circuits favor significant NBTI related trap generation in PMOSFETs. In NBTI, the interface trap density increases over time in a characteristic power law behavior, and eventually threatens the operational lifetimes of the transistors and the circuits. Therefore understanding the NBTI degradation is of primary importance for existing and near future technologies.

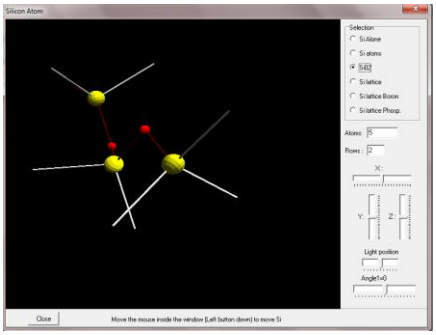

Fig. 3.1: SiO_2 atom structure.

The existing sensor operates in there different modes. In this paper 5 stages NAND oscillator used. Area of this Thus the oxide degradation sensor consist of three main components which can implemented in the form of CMOS circuitry. They are Schmitt trigger oscillator, Gate oxide leakage and differential amplifier shown in figure3.3. The use of differential amplifier in this circuits controlling stress voltage.

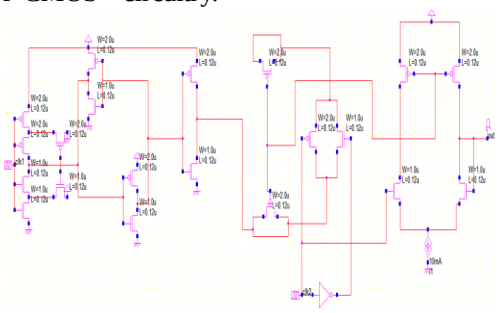

Fig. 3.3: Oxide Degradation Sensor Design.

NBTI circuit is 119mm^2 and which an additional circuitary for proper functioning were required. Thus the threshold voltage will be lowered due to this.

B. Proposed Design:

The design have a less number oscillator design stages for low power and better response with effective area. Circuit monitoring technique is used to avoid the stage problem these structured replaced by CMOS circuitry with 5 stage NAND Oscillator design shown in figure3.2. Device utilization factors like power and area can be analysed here. Oxide degradation sensor design was implemented for initial analysis.

The layout design for NBTI sensor, which trigger with the clock signal designed here with the help of Digital Schematic Editor. This design can be drawn from the verilog file which can be generated. The experimental result, power consumed by these sensor is noted as 15.258µw. From these results the frequency, maximum, minimum and average voltage can be measured.

A. NBTI Sensor:

IV. ***Simulation Result:***

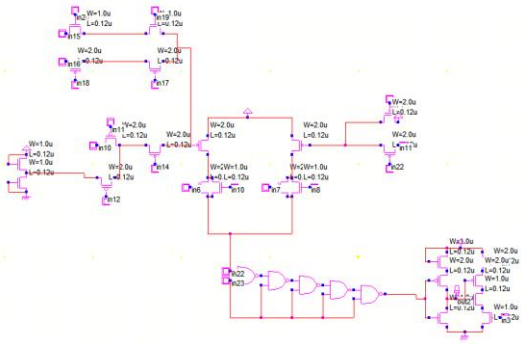

Fig. 3.2: NBTI Sensor Design.

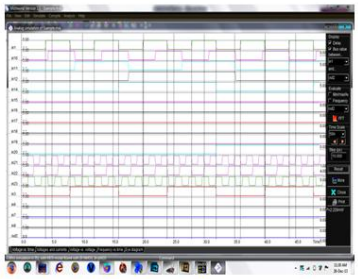

Fig. 4.1: Simulation Output.

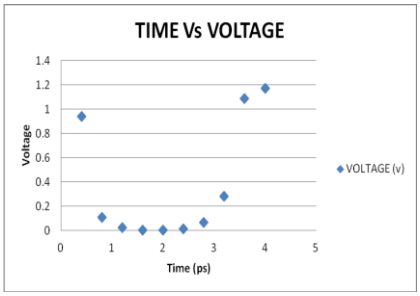

Fig. 4.3: Graphical Representation of Time Vs Voltage.

Table 4.1: Voltage Analysis.

TIME (ps)	VOLTAGE (v)
0.4	0.941
0.8	0.111
1.2	0.023
1.6	0.004
2	0.003
2.4	0.012
2.8	0.065
3.2	0.281
3.6	1.086
4	1.170

Table 4.1 shows the changes in their output voltage according to their time. These variation can be analysed in two different formats that can be mintioned below. They are FFT analysis and the graphical representation.

The Fast Fourier transform of oscillator output is shown in figure 4.2. From the Fast Fourier transform results the relationship between the frequency and voltage can be measured. In this window parameter analysis, frequency variations according to voltage and voltage variations according to time can be listed.

Table 4.2 shows the voltage change in output at the particular level of input during the negative voltage it produces constant output. These are th analysis result for NBTI sensor design alone. Thus the comparison of exsisting and the implemented can be mentioned in Table 4.3 shown below.

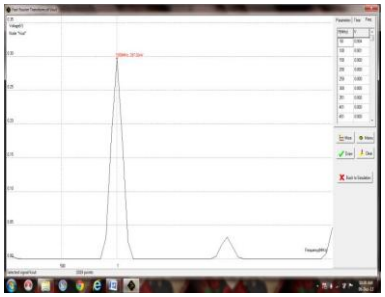

Fig 4.2: Fast Fourier Transform Output.

Table 4.2: Voltage Variation.

INPUT VOLTAGE (v)	OUTPUT VOLTAGE (v)
3.5	2.59
3	0.19
2.5	0.3
2	0.5
1.5	1.43
1	1.53
0.5	1.57
0	1.55
-0.5	1.85
-1	1.85
-1.5	1.85

Table 4.3: Comparision Result For NBTI.

PARAMETERS	*EXISTING SYSTEM*	*PROPOSED SYSTEM*
AREA	119.891mm^2	82.174mm^2
POWER	0.853mw	0.015mw

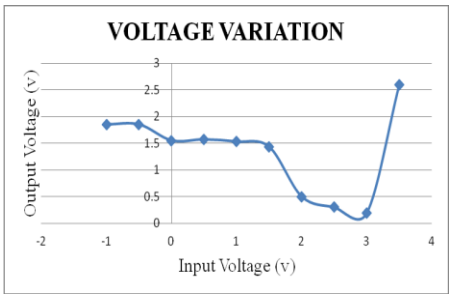

Fig. 4.4: Graphical Representation of Voltage Variation.

B. Oxide Degradation Sensor:

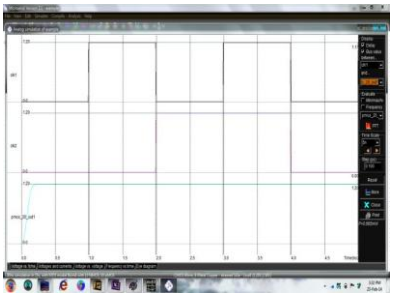

Fig. 4.5: Simulation Output.

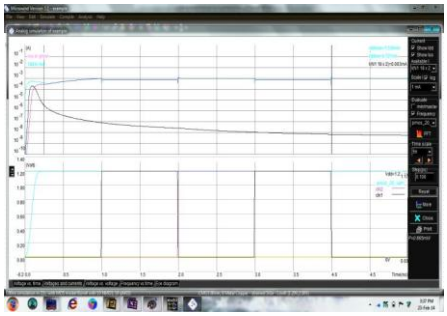

Fig. 4.6: Voltage Vs Current in Logarithmic Scale.

Thus the simulation output of oxide degradation sensor produce the output voltage 0.865mW which can be varied according to the noise added to input voltage. By using these output variation the SNR value can be calculated in future.

Table 4.4: Voltage Analysis.

TIME(ps)	VOLTAGE(v)
0.1	0.008
0.6	0.108
1.2	0.358
1.8	0.678
2.4	0.97
3	1.132
3.6	1.185
4.2	1.196
4.8	1.199
5.4	1.199
6	1.2

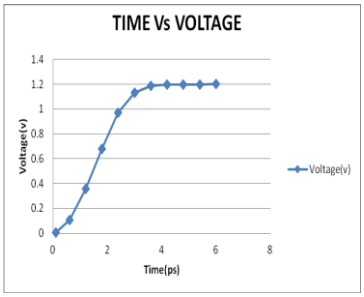

Fig. 4.7: Graphical Representation of Time Vs Voltage.

Table 4.4 shows the voltage change in output at the particular time according to that it produces constant output voltage for varying time initially in has linear variation. These are th analysis result for oxide degradation sensor design with schmitt trigger oscillator.

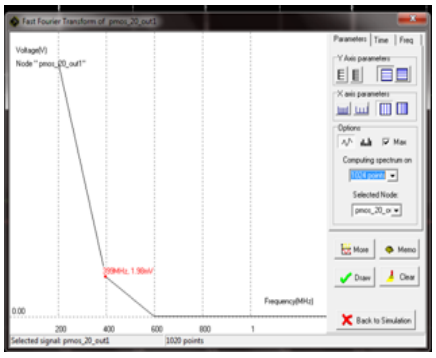

Fig. 4.8: Fast Fourier Transform Output.

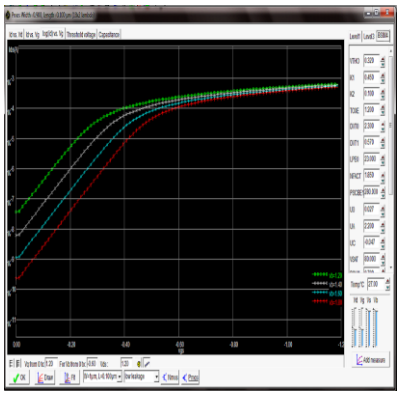

Fig. 4.9: I_D Vs V_G in Logarithmic Scale.

Figure4.9 is the MOS characteristic simulation window it produces capacitance, threshold variation, V_D Vs I_D, log I_D Vs V_G and so on this can be developed in BSIM level with 90nm technology.

Thus the figure4.10 and 4.11 are the various results for parametric analysis. Crosstalk amplitude can be taken in Montoe Carlo Analysis it produce constant amplitude with varying Vdd. Thus the final voltage Vdd =1.2 for varying capacitance.

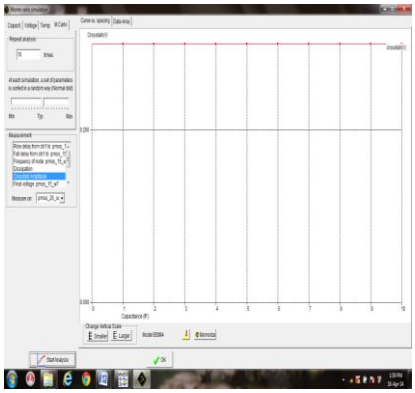

Fig. 4.10: Crosstalk Amplitude.

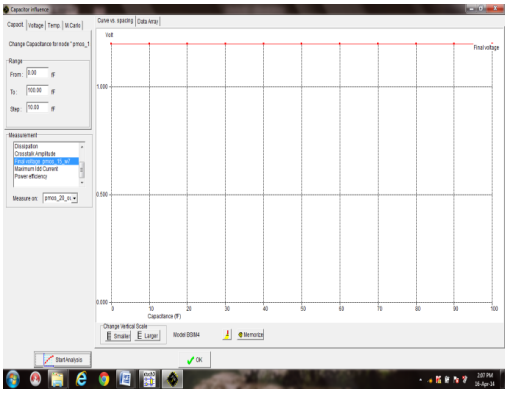

Fig. 4.11: Final voltage (Vdd) Vs Capacitance.

V. Conclusion & future work:

A. Conclusion:

The proposed system design have a less number oscillator design stages for low power and better response with effective area. To avoid the stage problem these structured are replaced by CMOS circuitry with simple PMOS and NMOS design. This project analyses the more number of circuit that was equivalent to the block which can be specified and the results can be taken in the simulation format.

Proposed paper presents two compact low power NBTI and Gate oxide degradation sensor with

digital outputs. The sensor helps in monitoring chip reliability throughout the lifetime of the system. The data supplied by these sensors are useful in understanding and modeling the complex degradation and recovery mechanisms. In this design oscillator using PMOS and NMOS elements can be modified by using inverter chain based ring oscillator and the other logic gates such as NORs and Pass Gates, can also be utilized. The power consumed in the proposed NBTI sensor is 15.258µw it is low when compare to previous device consumed power and for Oxide degradation sesor is 0.865mw.

B. Future Implementation:

In this project the power consumed by the sensor was nominally low and it helps to obtain better results. The analysis of oxide degradation sensor can be done in future which means that the noise can be added to the input voltage and the output voltage changes can be taken up then the SNR value calculated. By using this design the power and area can be reduced.

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