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Comparison of Various controllers for Single Ended Primary Inductor Converter

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ABSTRACT

Background: Design of SEPIC converter is a challenge for engineers due to the user requirements and the intrinsic non linear nature .The controller for the SEPIC converter is a circuit or an algorithm which changes the Pulse Width Modulation (PWM) waveform by adjusting the ON-OFF timings thereby keeping the output at the desired value. Quick settling time and rise time to the desired output along with high efficiency, required phase margin, loop bandwidth are the main constraints on the controller. The design of such controller is the main purpose of this research paper. Three types of controllers are designed, namely the PI controller, Fuzzy Logic Controller (FLC) and Sliding Mode Controller (SMC). PI controller is tuned using Ziegler Nicholas (ZN) method. FLC with optimum number of rules is designed. SMC is designed using state space averaging method. These controllers are compared.

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INTRODUCTION

A DC-to-DC converter is a device that accepts a DC input voltage and converts another DC output voltage. DC-to-DC converters are used to provide voltage regulation, constant output voltage, etc. The specifications are the voltage ratio, the maximum output power, conversion efficiency, number of components, power density, galvanic separation etc. They show complex dynamic behaviour due to their nonlinear nature, resulting from the continual switching operation. The state space averaging technique is used to derive for the boost converter but no simulation or hardware given in the proof of this state space averaging in (Vandana Jha and Pankaj Rai, 2012). Control of SEPIC converter using neural network tuned PI controller has been demonstrated in (Ramash Kumar, 2010). The mathematical modeling of the SEPIC converter has been given. A PI controller has been used in the SEPIC converter in (Kalantar, 2010). Sliding mode controller has been developed to ensure robustness against all variations and Single Ended Primary Inductor converter (SEPIC) is widely used in the biomedical engineering, communication, industrial electronics and power supplies. When the required output does not follow the set-point, a controller is to be used with the objective of keeping the error as a minimum. For a SEPIC converter, the input and load variations are major reasons which alter the proper functioning.

This paper is organized as follows. The mathematical model of SEPIC is reviewed in Section II . PI controller in Section III . Fuzzy logic controller in section IV. Sliding mode controller in section V. Simulation of controllers in section VI. Conclusions are given in Section VII.

Ii. Sepic converter:

SEPIC is useful in applications in which a voltage can be above and below that of the regulator's intended output. The amount of energy exchanged is controlled by switch S, which is typically a transistor such as a MOSFET, IGBT, etc. There are various modeling methods available like Signal flow graph, State space average and Small signal model. In this proposed controller, the state space averaging method is adopted.

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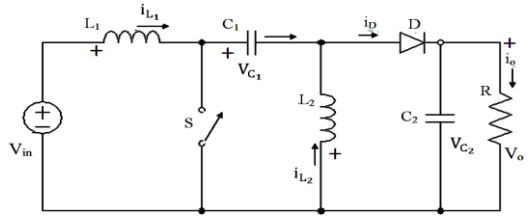

Fig. 1: Basic SEPIC Converter.

SEPIC is useful in applications in which a voltage can be above and below that of the regulator's intended output. The amount of energy exchanged is controlled by switch S, which is typically a transistor such as a MOSFET, IGBT, etc. There are various modeling methods available like Signal flow graph, State space average and Small signal model. In this proposed controller, the state space averaging method is adopted.

A power circuit diagram of the SEPIC is shown in Fig.1. It includes DC input supply voltage V_{in} , the capacitors C_1 and C_2 the inductors L_1 and L_2 the switch S (MOSFET), the diode D and the load resistance R. It is assumed that the components are ideal and also SEPIC operates in CCM.

Fig.2 and Fig 3 show the modes of operation of the SEPIC. In Fig.2 , when the switch s is closed, the diode is reverse biased and open, the Inductor L_1 is occupied by the source voltage Vin, the L_2 charges to the capacitor C_1, and the polarity of the inductor current and, capacitor shown in Fig.2.

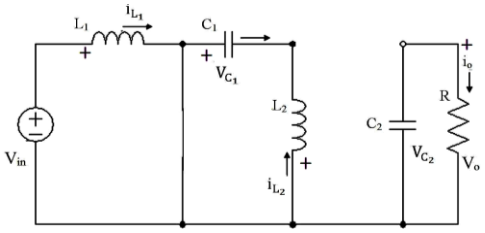

Fig. 2: SEPIC converter during switch On.

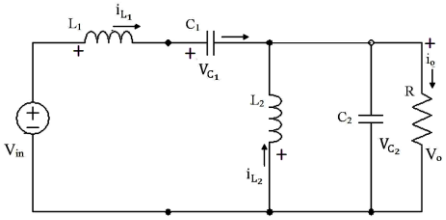

Fig. 3 .SEPIC converter during switch Off

The current i_{L1} increases at the rate of

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1}, 0 \le t \le dT \tag{1}$$

Where V_{C_1} is the voltage across the capacitor C_1. In Fig 2 when the switch is open, diode D is forward biased and closed, Inductor L_1 charges the capacitor C_1 and the Inductor L_2 discharging and C_2 is charging, at this time the equation can be obtained as

$$i_{in} = i_{L_1} \tag{2}$$

$$i_{L_{2a}} = i_{Da} = i_o \tag{3}$$

Where i_{Da} is the average current of diode D and i_o is output current. When the switch is open, the equation can be obtained as

$$V_{in} dT + (V_o (1-d)T]/T = 0 \tag{4}$$

The state variables of a SEPIC (x_1, x_2, x_3, x_4) are considered as currents i_{L_1} and, the voltages v_{C_1} and v_{C_2} respectively when the switch is closed, the state space equation can be obtained as

$$\begin{cases} \dot{x}_1 = \dfrac{-i_{L_1}}{L_1} + \dfrac{v_{in}}{L_1} \\ \dot{x}_2 = \dfrac{-i_{L_2}}{L_2} - \dfrac{v_{C_1}}{L_2} \\ \dot{x}_3 = \dfrac{i_{L_2}}{C_1} \\ \dot{x}_4 = -\dfrac{v_{C_2}}{RC_2} \end{cases} \tag{5}$$

The state space averaging technique,

$$\frac{d}{dt}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} = \begin{bmatrix} \frac{-1}{L_1} & 0 & \frac{-1}{L_1} & \frac{-1}{L_1} \\ 0 & \frac{-1}{L_2} & 0 & \frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{-1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{v_{C_1}+v_{C_2}}{L_1} \\ \frac{-v_{C_2}+v_{C_1}}{L_2} \\ \frac{-i_{L_1}}{C_1}+\frac{i_{L_2}}{C_1} \\ \frac{-i_{L2}}{C_2}+\frac{i_{L_2}}{C_2} \end{bmatrix} \gamma + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \tag{6}$$

$$\dot{X} = AX + B\gamma + C \tag{7}$$

Where γ is the status of the switches and $X, \dot{X}$ are the state variables of currents i_{L_1} and i_{L2}, voltages v_{c_1} and v_{c_2} and their derivatives respectively.

$$\gamma = \begin{cases} 1 \to S \to ON \\ 0 \to S \to OFF \end{cases} \tag{8}$$

iii. controllers:

SEPIC converter is a nonlinear system and the variation in parameters like line voltage, load variation, component variation. In this paper a attempt made to design three types if controllers and compared the performance. PI controller is designed using Ziegler-Nicholas method. The fuzzy logic controller (FLC) is designed with the same parameters using mumdani model. The third method is sliding mode controller (SMC) by considering four parameters of state variables of currents i_{L_1} and i_{L2},

voltages v_{c_1} and v_{c_2} . The specification of SEPIC is given in Table I. This common circuit specification is applied to the three type of controllers viz PI,FLC and SMC. Only controller is changed by maintaining all parameters. The comparisons are made with the same 48V output. The aim is to maintain the constant voltage, stability in change of operating condition.

Table I: Specification of Proposed SEPIC.

Specification/ Parameter	Unit/ Symbol	Value/ quantity
Input Voltage	V_{in}	12
Output Voltage	Vo	48
Inductor	l_{L1},l_{L2}	1300µH
Capacitors	c_1,c_2	50µF ,600µF
Nominal switching frequency	f_s	100kHz
Load resistance	R	50Ω
Range of duty cycle	*d*	0.4 to 0.89
Desired duty cycle	*d*	0.78

Fig.4 shows the block diagram representation of proposed work. Generally feedback controllers are provided to ensure and maintain desired operating conditions.

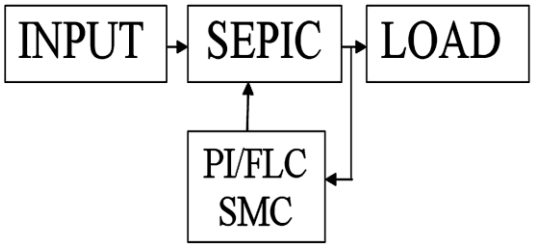

Fig. 4: Proposed controllers for SEPIC.

III.Proportional integral controller:

The PI control is designed to ensure the specifying desired nominal operating point for SEPIC, then regulating SEPIC, so that it stays very close to the nominal operating point in the case of sudden disturbances, set point variations, noise, modeling errors and component variations. The PI control settings proportional gain (*Kp*) and integral time (*Ti*) are designed using Zeigler – Nichols tuning method. (Chung, G.B., 1996) By applying the step test to (8) and (9) to obtain an S – shaped curve of step response of SEPIC as shown in Fig. 4. From the S-shaped curve of step response of SEPIC may be characterized by two constants, delay time L = 0.005s and time constant T = 0.052s. The delay time and time constant are determined by drawing a tangent line at the inflection point of the S-shaped curve and determining the intersections of the tangent line with the time axis and line output response U*(t)* as shown in Fig. 4. Ziegler and Nichols suggested to set the values of Kp = 9.36 and Ti = 0.016s according to the Table II. The PI control, optimal setting values (*Kp* and *Ti*) for SEPIC are obtained by finding the minimum values of the integral of the square of error. The simulink model of a block of PI control section and its transfer function model are shown in Fig. 4. Error in output voltage and change in duty cycle of the power switch *S* (n-channel MOSFET) is respectively the input and output of the PI control.

Table II: Ziegler and Nichols.

Types of controller	Kp	Ti	Td
P	T/L	∞	0
PI	0.9T/L	L/0.3	0
PID	1.2T/L	2TL	0.5TL

The validation of the system performance is verified for various regions like transient region, line variations, load variations, steady state region and also components variations. .Simulations has been performed on the SEPIC converter circuit. The Matlab/Simulink simulation model is depicted in Fig. 4. It can be seen that error in output voltage of the power switch (MOSFET) of PI control input is obtained by the difference between feedback output voltage and feedback reference output voltage, and output of PI control, change in duty cycle of the power switch (MOSFET)

Iv. Fuzzy logic controller:

A Fuzzy control system is a control system based on Fuzzy logic, a mathematical system that analyzes analog input values in terms of logical variables that take on continuous values between 0 and 1. The Fuzzy controller is one of the most active areas for research in the applications of Fuzzy set theory. A Fuzzy logic system is based on the logical system which is much closer in spirit to human thinking and natural language than traditional logical systems. The Fuzzy logic controller based on Fuzzy logic provides a means of converting a linguistic control strategy based on expert knowledge into an automatic control strategy.

A more sophisticated, practical example is the use of Fuzzy logic in high-performance error correction to improve information reception over a limited-bandwidth communication link affected by data-corrupting noise using turbo codes. The front-end of a decoder produces a likelihood measure for the value intended by the sender (0 or 1) for each bit in the data stream. The likelihood measures might use a scale of 256 values between extremes of "certainly 0" and "certainly 1". Two decoders may analyze the data in parallel, arriving at different likelihood results for the values intended by the sender. Each can then use as additional data the other's likelihood results, and repeats the process to improve the results until consensus is reached.

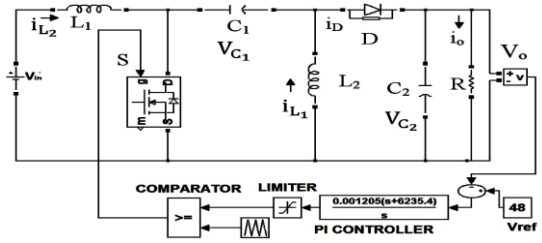

Fig. 5: Simulink model of PI control with SEPIC.

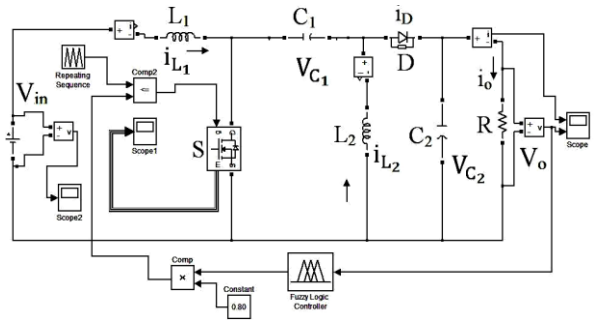

Fig. 6: Simulink model of Fuzzy control for SEPIC.

The variations are compared along with the FLC and SMC controller in section VII.

V. Sliding mode controller:

Sensing of all of the state variables and the generation of suitable references for each of them are the basic requirements of a SMC. According to the principles of a SMC, the capacitor voltages v_{c_1} and v_{c_2} are made to follow their references as dependable as possible. It is difficult to measure the inductor current reference since it usually depends on the load power demand supply voltage and the load voltage. To overcome this problem in implementation, the state variable error for the inductor current $\left(i_{L_1}-i_{L_1ref}, i_{L_2}-i_{L_2ref}\right)$ can be obtained from the feedback variable i_{L_1}, i_{L_2} by means of a high-pass filter under the assumption that their low-frequency component is automatically adapted to the actual operation of converting. As such, It is found that merely the high-frequency component of this variable is needed for control. The system order will be increased due to the high pass filter and can heavily alter the SEPIC converter dynamics. In order to avoid this problem, the cutoff frequency of the high-pass filter must be suitably lower than the switching frequency to pass the ripple, but it should be more to tolerate a quick response of SEPIC converter.

In the design of the converter, a sliding surface equation in the state space, which is expressed by a linear combination of the state-variable errors ε (the respective differences of the feedback reference current/voltage and the feedback actual current/voltage), have to be chosen optimally.

$$S(i_{L_1}, i_{L_2}, v_{c_1}, v_{c_2}) = k_1\varepsilon_1 + k_2\varepsilon_2 + k_3\varepsilon_3 + k_4\varepsilon_4 \quad (9)$$

Where the coefficients, k_1, k_2, k_3 and k_4 are the proper gains ε_1 and ε_2 are current feedback current errors, ε_3 and ε_4 are the feedback voltage errors and obtained the equation

$$s(i_{L_1}, i_{L2}, v_{C_1}, v_{C_2}) = k_1(i_{L_1} - i_{L_1ref}) + k_2(i_{L_2} - i_{L_2ref}) + k_3(v_{C_1} - v_{C_1ref}) + k_4(v_{C_2} - v_{C_{21}ref}) \quad (10)$$

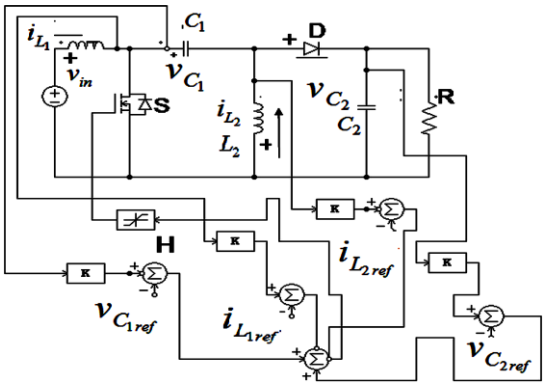

Fig. 7: Principle scheme of SMC for SEPIC.

The signal $s\,(i_{L_1}, i_{L2}, v_{C_1}, v_{C_2})$ is generated using (9a) while a conventional hysteresis modulator generates the gate pulses to the MOSFET switch. The complete control arrangement of a SEPIC is shown in Fig.4. The status of the switch (γ) is controlled by hysteresis block H, which aims to minimize the error of the variables $i_{L_1}, i_{L_2}, v_{c_1}$ and v_{c_2}. The system response is determined by the circuit parameters and the coefficients k_1, k_2, k_3 and k_4.

It is essential to make a note that the switching frequency, the inductor current ripple depend on the reference voltage, the capacitor voltages v_{c_1} and v_{c_2} and the inductor current i_{L_1} and i_{L_2}. It is important to determine circuit parameters and coefficients of k1, k2, k3 and k_4 that agree with the desirable values for a maximum inductor current

ripple, a maximum capacitor ripple, a maximum switching frequency, stability, and a fast response under any operating condition.

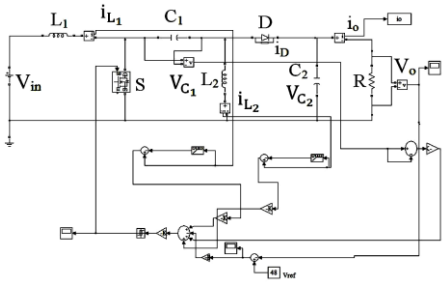

Fig. 9: Simulink model of SMC for SEPIC**.**

Simulation of Controllerss:

The main purpose of this section is to discuss the simulation results of the SEPIC with three different control methods. The parameters are considered as given in Table-II . The controllers are connected separately and verified the results. The comparisons are made for the performance of controller and analyzed the results. The validation of the controllers performance is done for five different conditions viz.

a) Start up transient
b) Steady state condition
c) Load variation
d) Line variation and
e) Component variations

Fig. 10 shows the dynamic behavior at startup for the output voltage of SEPIC for different controllers viz. PI, Fuzzy, SMC. The reference value Vo is set at 48V and the resistance 50 ohm for all controllers. The startup performance is given in Table-III It can be ascertained that the output voltage of the SEPIC has a little rise time 0.03851s using SMC and a less settling time 0.954 for FLC.

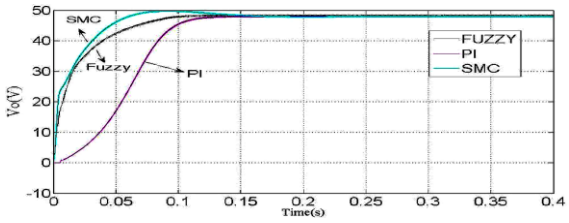

Fig.10: Response output voltage at start up of controllers for input voltage 12V and load 50 Ohm for SEPIC converter.

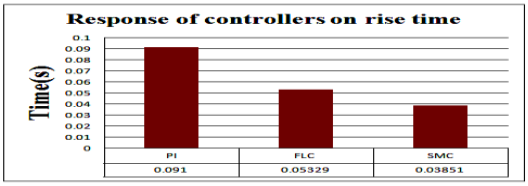

Fig. 11: Response output voltage at startup controllers for input voltage 12V and load 50 Ohm for SEPIC

A. Start-up transients:

Table III: Response of controllers

Controller	Rise Time	SettlingTime
PI	0.091	0.1423
FLC	0.05329	0.0954
SMC	0.03851	0.1453

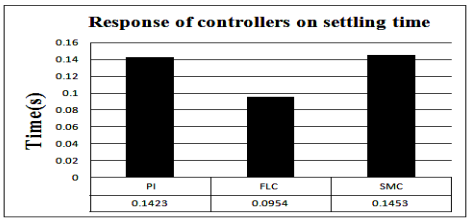

Fig. 12: Response of controllers at startup on settling time.

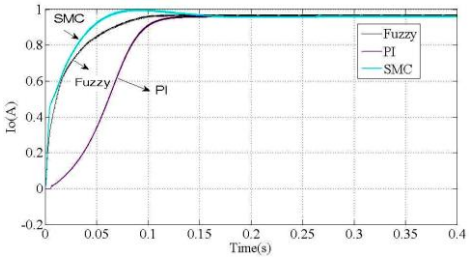

Fig. 13: Response output current of controllers at input voltage 12V and load 50 Ohm for SEPIC converter

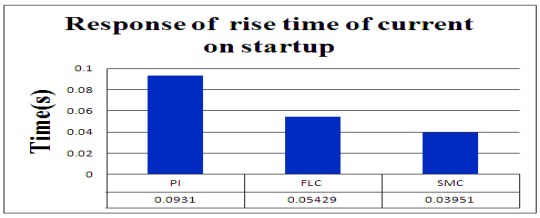

Fig. 14: Response of controllers at startup on settling time.

Fig. 11 shows the dynamic behavior at startup rise time for the output voltage of SEPIC for different controllers viz. PI, Fuzzy, SMC. The reference value Vo is set at 48V and the resistance 50 ohm for all controllers. It can be ascertained that the output voltage of the SEPIC has a little rise time 0.03851s using SMC and a more rise time 0.091 for PI.

Fig. 12 shows the dynamic behavior at a startup settling time for the output voltage of SEPIC for different controllers viz. PI, Fuzzy, SMC. The reference value Vo is set at 48V and the resistance 50 ohm for all controllers. It can be ascertained that the output voltage of the SEPIC has a little settling time 0.0954s using FLC and a more settling time 0.0.1453s for SMC.

The response of current during the startup is also analyzed. Fig.12. shows the load current for48V and the load resistance of 50ohm

Fig. 13 shows the dynamic behavior of current at startup for the SEPIC for different controller's viz. PI, Fuzzy, SMC and it is given in Table –IV. The reference value Vo is set at 48V and the resistance 50 ohm for all controllers. It can be ascertained that the output current of the SEPIC has a little settling time 0.0964s using FLC and a more settling time 0.0.1453s for PI.

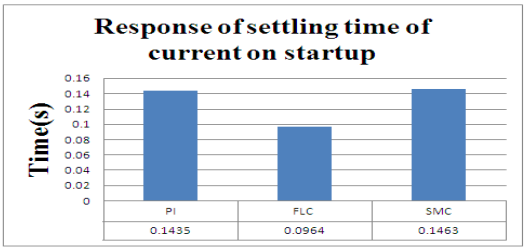

Fig. 15: Response of settling time of current.

Fig. 14 shows the bar graph representation of dynamic behavior at a startup rise time for the output voltage of SEPIC for different controller's viz. PI, Fuzzy, SM Fig. 15 shows the bar graph representation of dynamic behaviour at startup settling time for the output voltage of SEPIC for different controller's viz. PI, Fuzzy, SMC.

B. Steady state region:

Fig. 16 shows the dynamic behavior at steady state region for the output current of SEPIC for Fuzzy. The reference value Vo is set at 48V and the resistance 50 ohm for all controllers. The full load current is 0.96A. It can be ascertained that the output current, has minimum variation in steady state for 0.0097 for Fuzzy controller.

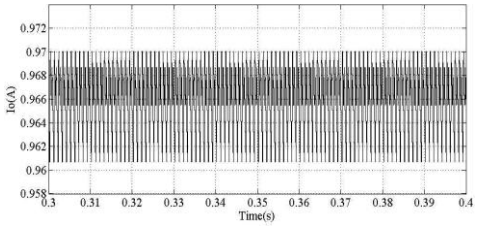

Fig. 16: Fuzzy current at steady state region.

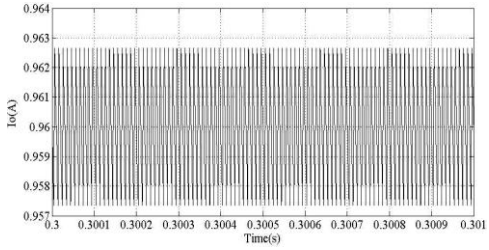

Fig. 17: Steady state current of PI.

Fig. 17 shows the dynamic behavior at steady state region for the output current of SEPIC for PI controller. The reference value Vo is set at 48V and the resistance 50 ohm. The full load current is 0.96A. It can be ascertained that the output current has minimum variation at steady state for 0.0055 for PI controller

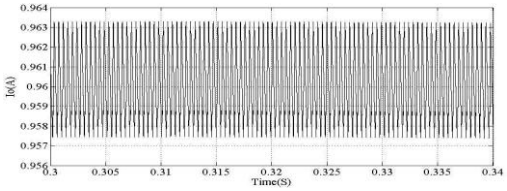

Fig. 18: Steady state current SMC.

Fig. 18 shows the dynamic behavior at steady state region for the output current of SEPIC for SMC controller. The reference value Vo is set at 48V and the resistance 50 ohm. The full load current is 0.96A. It can be ascertained that the output current has minimum variation at steady state for 0.0062 for PI controller

The Table VI gives the response of steady state response of current of SEPIC for various controllers. The reference value Vo is set at 48V and the resistance 50 ohm. The full load current is 0.96A. It can be ascertained that the output current has minimum variation at steady state for 0.0055 for PI controller.

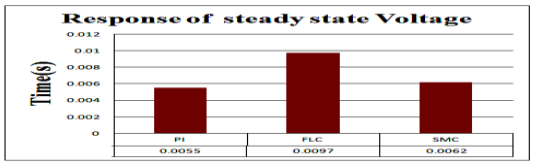

Fig. 19: Response of steady state current.

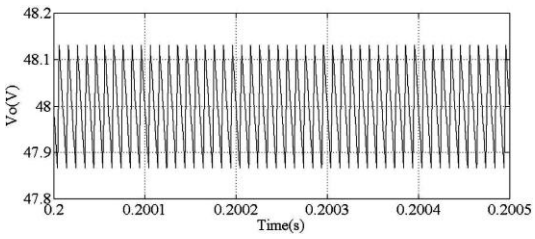

Fig. 20: Steady state voltage of PI.

Fig.19.Shows bar graph representation of the dynamic behavior at steady state region for the output current of SEPIC of SMC controller. The reference value Vo is set at 48V and the resistance 50 ohm. The full load current is 0.96A. It can be ascertained that the output current, has minimum variation in steady state for 0.0055 for PI controller Fig. 20 shows the dynamic behavior at steady state region for the output voltage of SEPIC for PI controller. The output voltage is 48V. It can be ascertained that the output voltage has minimum variation in steady state for 0.29 for PI controller

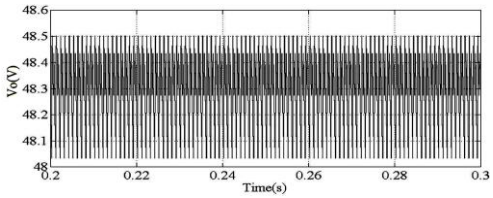

Fig. 21: Steady state voltage of Fuzzy.

Fig. 21 shows the dynamic behavior at steady state region for the output voltage of SEPIC for Fuzzy controller. The output voltage is 48V. It can be ascertained that the output voltage has minimum variation in steady state for 0.47 for Fuzzy controller.

Table III shows the steady state voltage for SEPIC using various controllers. It is found that SMC has less voltage variation during steady state conditions.

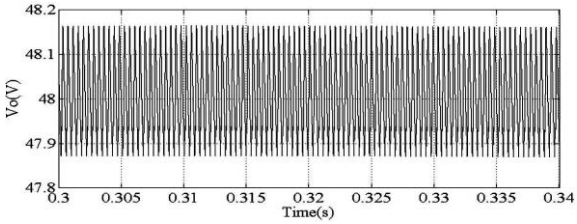

Fig. 22: Steady state voltage of SMC.

Fig. 22 shows the dynamic behavior at steady state region for the output voltage of SEPIC for SMC controller. The output voltage is 48V. It can be ascertained that the output voltage has minimum variation in steady state for 0.28V for SMC controller

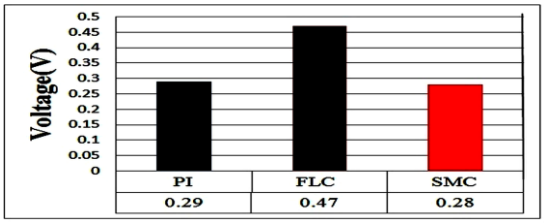

Fig. 23: Steady state voltage.

Table V: Response of controllers.

Controller	Rise Time	Settling Time
PI	0.0931	0.1435
FLC	0.05429	0.0964
SMC	0.03951	0.1463

Table III: Response of controllers on steady state current

Controller	Steady state Voltage
PI	0.29
FLC	0.47
SMC	0.28

Fig. 23. Shows bar graph representation of the dynamic behavior at steady state region for the output voltage of SEPIC for PI, Fuzzy and SMC controller. The reference value Vo is set at 48V and the resistance 50 ohm. It can be ascertained that the output voltage has minimum variation of voltage at steady state for 0.29V for PI controller, fuzzy controller has 0.47V and SMC has 0.28V. The steady state voltage variation SMC has a good response in steady state in maintaining the voltage.

A. Load variation:

Fig.24. show's response of output voltage of the SEPIC converter when load value takes a step changes using PI,FLC and SMC controllers for a load step change from 40Ω to 50Ω (-20% load variations) at time = 0.2s. It can be seen that the output voltage of the paralleled modules using the PI has a small overshoot of 3.55 V with a settling time of 0.0131 s, while the output voltage of the SEPIC using a FLC controller has a maximum overshoot of 4.72V and a settling time of 0.0622s and SMC has a maximum overshoot of 3.73V and a settling time of 0.0644s respectively.

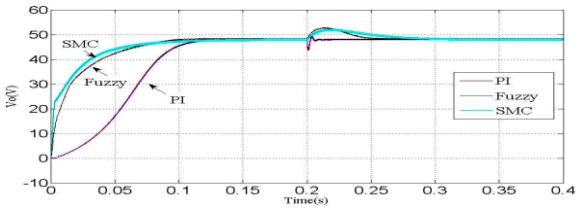

Fig. 24: Load Variation 40 Ω to 50Ω.

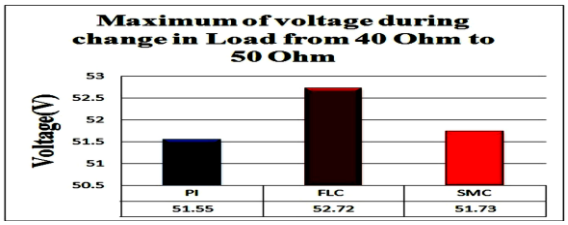

Fig. 25: Load Variation 40 Ω to 50Ω.

Fig. 25. Shows bar graph representation of the dynamic behavior at load change for the output voltage of SEPIC for PI, Fuzzy and SMC controller. The reference value Vo is set at 48V and the load variation from 40Ω to 50 Ω. It can be seen that the output voltage of the SEPIC using the PI has a small overshoot of 3.55 V with a settling time of 0.0131 s, while the output voltage of the SEPIC using a FLC controller has a maximum overshoot of 4.72V and a settling time of 0.0622s and SMC has a maximum overshoot of 3.73V and a settling time of 0.0644s respectively.

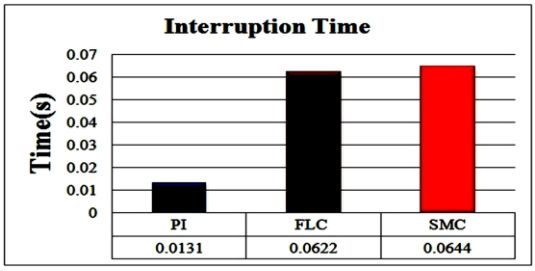

Fig. 26: Load Variation 40 Ω to 50Ω.

Fig. 26. Shows bar graph representation of the dynamic behavior at load change for the output voltage of SEPIC for PI, Fuzzy and SMC controller. The reference value Vo is set at 48V and the load variation from 40Ω to 50 Ω. It can be seen that the output voltage of the SEPIC using the PI has a small settling time of 0.0131 s, while the output voltage of the SEPIC using a FLC controller has a settling time of 0.0622s and SMC has a settling time of 0.0644s respectively.

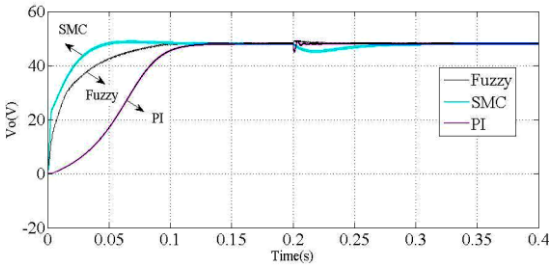

Fig. 27: Load variation from 50Ω to 60Ω.

Fig.27. shows response of output voltage of SEPIC converter when load value takes a step changes using PI,FLC and SMC controllers for a load step change from 50Ω to 60Ω (+20% load variations) at time = 0.2s. It can be seen that the output voltage of the paralleled modules using the PI has a voltage variation of 2.46 V with a settling time of 0.0181 s, while the output voltage of the SEPIC using a FLC controller has a voltage variation of 1V and a settling time of 0.0148s and SMC has a maximum variation of 3.05V and a settling time of 0.0263s respectively. Table V gives the variation of voltage during step change in load.

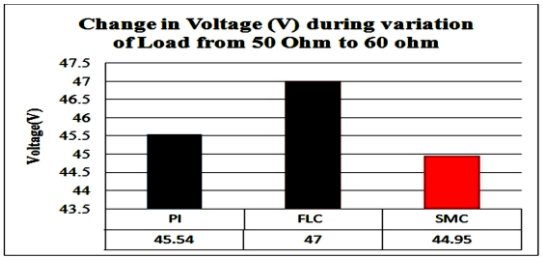

Fig. 28: Load Variation 50 Ω to 60Ω.

Table IV: Response of controllers on load variation 50Ω to 60Ω

Controller	Maximum rise in change in load	Interruption Time
PI	45.54	0.0181
FLC	47.00	0.0148
SMC	44.95	0.0263

Fig. 28. Shows bar graph representation of the dynamic behavior at load change for the output voltage of SEPIC for PI, Fuzzy and SMC controller. The reference value Vo is set at 48V and the load variation from 50Ω to 60 Ω. It can be see that the output voltage of the SEPIC using the PI has a voltage variation of 2.46V, while the output voltage of the SEPIC using a FLC controller has 1V and SMC has a maximum voltage variation of 3.05V respectively.

Fig.29. Shows bar graph representation of the dynamic behavior at load change for the output voltage of SEPIC for PI, Fuzzy and SMC controller. The reference value Vo is set at 48V and the load variation from 50Ω to 60 Ω. It can be seen that the output voltage of the SEPIC using the PI has a settling time of 0.0181 s, while the output voltage of the SEPIC using a FLC controller has a settling time of 0.0148s and SMC has a settling time of 0.0263s respectively.

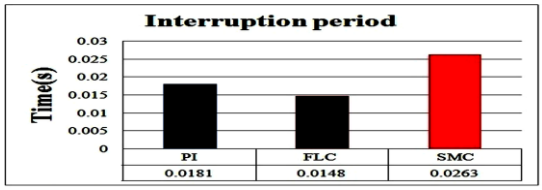

Fig. 29: Load Variation 50 Ω to 60Ω.

d. line variation:

Fig.30. shows response of output voltage of SEPIC converter when line value takes a step changes using PI, FLC and SMC controllers for a load step change from 12V to 9V (+20% line variations) at time = 0.2s. It can be seen that the output voltage of the SEPIC using the PI has a voltage variation of 13.90 V with a settling time of 0.2538 s, while the output voltage of the SEPIC using a FLC controller has a voltage variation of 1.21V and a settling time of 0.2183s and SMC has a maximum variation of 5.17V and a settling time of 0.2945s respectively. Table VI gives the variation of voltage during step change input

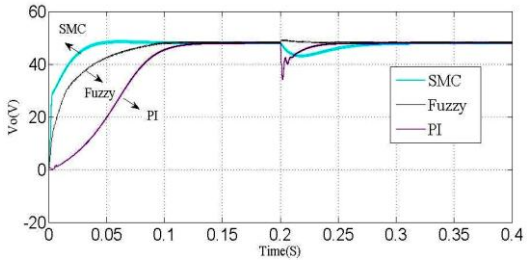

Fig. 30: Input supply variation from12V dc to 9VDC.

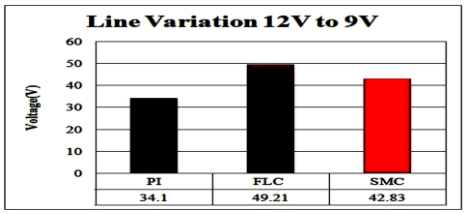

Fig.31: Line Variation 12V to 9V.

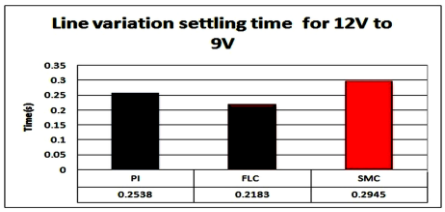

Fig. 32: Line variation settling time for 12V to 9V.

Table VI: Response of controllers on line variation 12V to 9V.

Controller	Voltage change	Settling Time
PI	34.10	0.2538
FLC	49.21	0.2183
SMC	42.83	0.2945

Table V: Response of controllers on line variation 12V to15V.

Controller	Voltage change	Settling Time
PI	67.69	0.2503
FLC	52.16	0.2463
SMC	41.87	0.2699

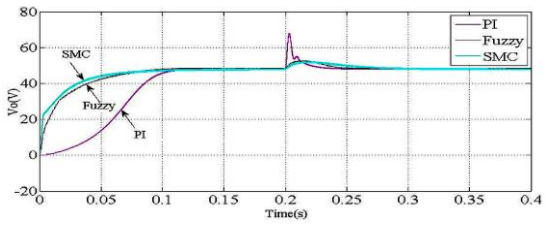

Fig. 33: Input supply variation from12V dc to 15Vdc

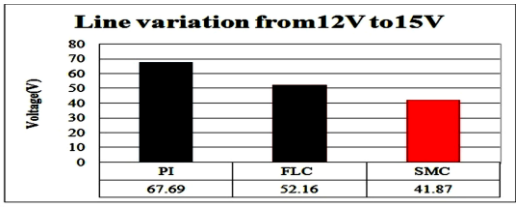

Fig. 34: Variation in output voltage for input supply variation from12V dc to 15Vdc.

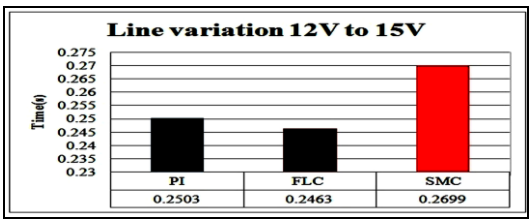

Fig. 35: Settling time for input supply variation from12V dc to 15Vdc.

RESULT AND DISCUSSIONS

This paper proposes a design of controllers and a comparison of the controller performance. SEPIC converter capable of having low rise time, fast settling time and steady state output of startup, line and load variations. In this work, the design of the PI, Fuzzy and SMC are designed for a 12V input and 48V output

voltage specifications. The PI turning method is performed by Ziegler-Nicholas control. Fuzzy logic control is adopted with the fuzzy rules. SMC controller is developed. The outputs are compared with the controller performance.

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