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Low Power 8t Sram Design using Minimum Power Design Method

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ABSTRACT

Low-power Random Access Memory (RAM) has seen a remarkable and rapid progress in power reduction. In nano-scaled devices, standby power needs to be reduced effectively for high performance System on Chip designs. For SRAM memories in 0.25µm, several improved low-power techniques have been applied. This paper explores the possibility of reduction in the power dissipation in 6T-SRAM cell. A novel Eight transistor (8T) CMOS SRAM cell design at 0.25um feature size is presented to improve the power dissipation, stability of the conventional SRAM cell

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INTRODUCTION

Static random access memory (SRAM) has been widely used as memory for logic cell. SRAM memory cell array occupies normally 40% of logic cell, so that the nature of logic cell such as operating speed, power, supply voltage, and chip size is limited by the characteristics of SRAM memory array. Therefore, the good design of SRAM cell and SRAM cell array is to obtain high performance, low power, low cost, and reliable logic cell. For obtaining these we can use modified PG gate structures and voltage scaling techniques. In this paper we deals with 65-nm low-power technology is used for simulation. In Section II, we explain SRAM structures. In Section III, we explain the voltage scaling and dual Vth schemes and its effects on SRAM and six transistors (6T) SRAM energy modelling. In Section IV, we analyze the effects of SRAM structure. Finally, Section V summarizes and concludes this work.

Sram structures:

In this 6t SRAM has been shown in the figure 1.In these four transistors (Q1−Q4) cross-coupled CMOS inverters and two NMOS transistors Q5 and Q6 provide read and write access to the cell. A 6T SRAM cell is the most popular SRAM cell due to its low power and low-voltage operation. This cell is used to detect the less voltage swing. Hence it is used for finding the power reduction in the circuits. When the transistor Q1 is ON it is in the active mode and the data can flow through the next transistor. Hence the leakage power can be reduced and it can be calculated by the capacitor which added to the PD gate method.

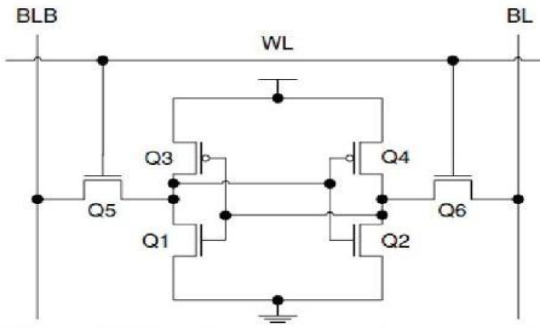

Fig. 1: 6T SRAM Cell.

For the 6T SRAM, the cell stability and the write ability may experience data-flipping with a bit cell changes its state from ’0’ to ’1’ or *vice versa* after being read or write failure that is the data to be written into a bit cell which fails to overwrite its previously stored value. To cope with these problems, several new SRAM cells equipped with some supportive peripheral circuits have been proposed like the P Gate and G Gate and PG gate cells (Evans, 1995; Agarwal, 2006; Zhai, 2008; Verma, 2008; Taniya Siddiqua 2011).

Techniques used:

Voltage scaling:

Supply voltage is a critical parameter in minimizing the SRAM energy. However, as the supply voltage comes around or below the threshold

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voltage, lowering supply voltage is not much effective in the energy minimization due to the increase in the static energy. Thus the delay can be getting increased.

Dual V_{th} Scheme Techniques:

Due to the dual Vth of the access transistors, act according to deep sub micron voltage the access speed of the transistors increases considerably. This helps in faster access of the data stored in the SRAM cell.

Hence using these different techniques we can enhance the energy efficiency. We also achieve low power.

Different sram structures:

A. Modified P Gate:

In these techniques the major problem is if we can for low voltage we want to add another one extra transistor this increases high space and high density. The modified P gate is shown in the figure 2.

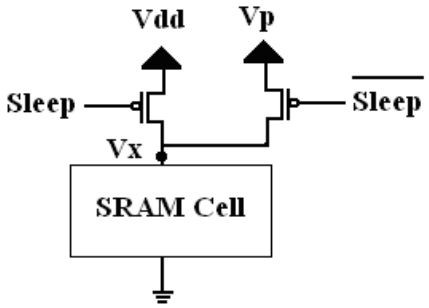

Fig. 2: Modified P gate.

B.Modified G Gate:

In this techniques the main drawback is at not discharge state, the stored data can get lost form the Transistor. But here we didn't go for one more transistor. Hence we go for modified PG gate. This modified G gate diagram can be shown in the figure 3.

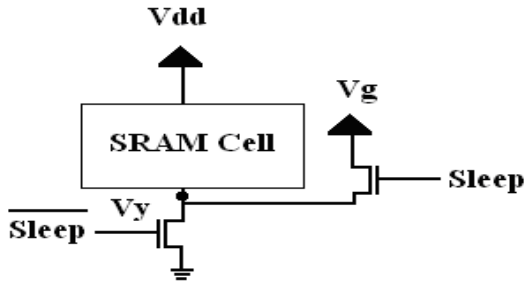

Fig. 3: Modified G Gate

C. Modified PG Gate:

In this type of circuit virtual ground and supply voltage can be selected and has a greater control over the supply voltage provided to the cell this can be shown in the figure 4. But in this we can't find the exact voltage. Hence we go for another one capacitor attached modified PG gate techniques this can be shown in the figure 5.

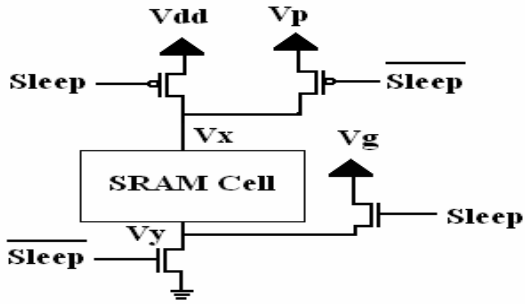

Fig. 4: Modified PG gate.

Minimum power design Method:

In this method two Pmos with capacitor is added with conventional 6T SRAM cell. By introducing two Pmos in the circuit the data stability problem has to be overcomes. The power dissipation is reduced by 37%.In modified P-gated,G-gated, Modified PG gated structure the power dissipation is reduced but not upto the level. Using two PMOS structure the data stability can be improved and capacitance reduce the power dissipation in the circuit.

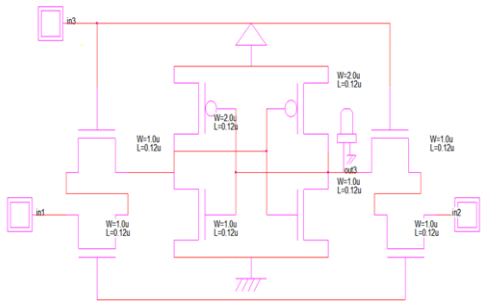

Fig. 5: Modified SRAM Cell with Capacitor.

Output and results:

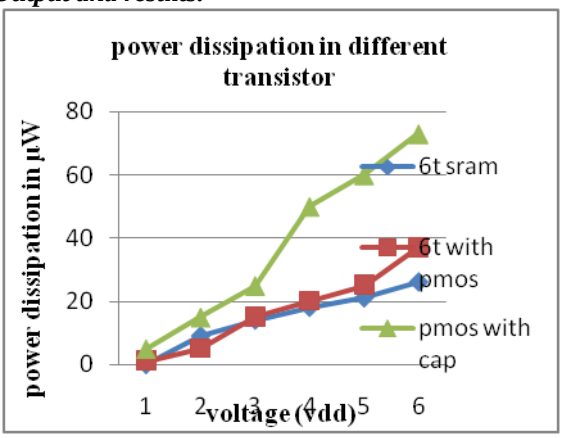

Fig. 6: Power Dissipation in Different structure.

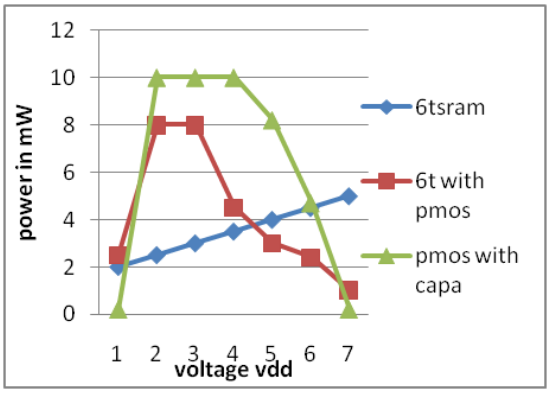

Fig. 7: Power dissipation in capacitance.

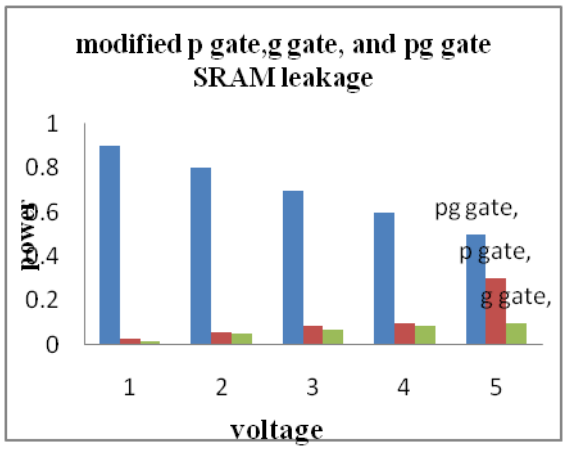

Fig. 8: Modified P-gated, G-gated and PG-gated SRAM cell leakage power reduction in 65nm in chart graph.

The above figure 8 shows that the power reduction in modified p gate, g gate, and pg gate. Hence the pg gate can reduce the voltage in chart graph.

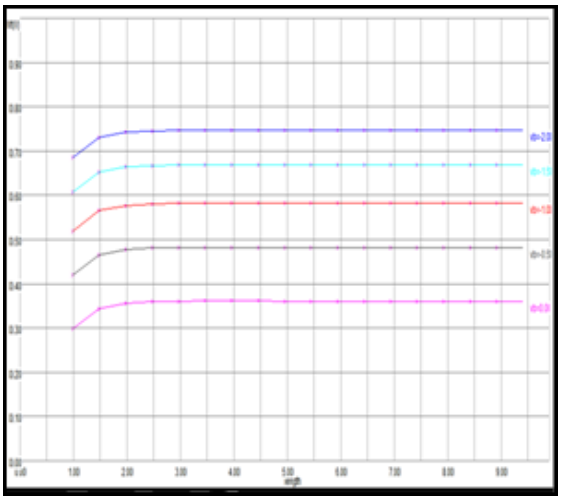

Fig. 9: Threshold voltage of pg gated techniques.

Thus the figure 9 shows that threshold voltage of pg gate techniques. In this the capacitor can reduced the power compared with the modified PG gate techniques.

Monte Carlo simulation:

Monte Carlo methods are a broad class of computational algorithms that rely on repeated random sampling to obtain numerical results; typically one runs simulations many times over in order to obtain the distribution of an unknown probabilistic entity. The name comes from the resemblance of the technique to the act of playing and recording your results in a real gambling casino. They are often used in physical and mathematical problems and are most useful when it is difficult or impossible to obtain a closed-form expression, or infeasible to apply a deterministic algorithm. Monte Carlo methods are mainly used in three distinct problems classes: optimization, numerical integration and generation of draws from a probability distribution.

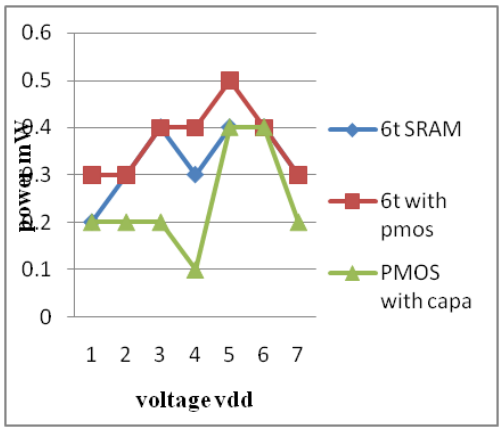

Fig. 10: power Dissipation in Monte Carlo Simulation.

Conclusion:

The 6T SRAM and its modified techniques have been simulated in 25nm feature size. The leakage power dissipation has been compared for related architectures were discussed. This is mainly driven by the increased part of SRAM power leakage in nanoscale CMOS technology at low voltage. Previous technique reduces the power dissipation by 20%. The proposed structure reduce the power by 37%.Thus we conclude that the energy efficiency can be enhanced and the power consumption also get reduced.

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