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Design and Analysis of Hybrid Full Adder Topologies Based on Improved DRPTL

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ABSTRACT

Recently adder circuit is becoming a major part in many applications and the arithmetic circuit is included in it as a fundamental operation. Basically the adder circuit is designed to achieve low power and less delay and by logic gate of the circuit improves the performances. In this paper, for significant process of power saving and efficient performances Hybrid Full Adder Topologies is proposed dynamically based on dual rails pass transistor logic (DRPTL) with the clock signal. For speed process high logic circuit is implemented and also to have less propagation. In hybrid CMOS design style various adder cells and transistor is used, but in proposed circuit DRPTL is implemented with the load condition and the clock signal to manage the power flow in the circuit. Also enhance the device performances and reduce the chip level power consumption. The proposed circuit is simulated for the analysis of performances by the implementation in Cadence Virtuoso Schematics on 45nm CMOS process models and illustrated the results performances delay, power, and transistor count reduction.

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INTRODUCTION

Nowadays, the complex criteria of emerging high speed communication process are increased in CMOS technologies used applications. Based on the logic circuit the complex process is performed the arithmetic division of adder circuit with multiplier in VLSI system. However the growth of electronics is increased with the critic fear of reduction in delay, power and area in any application. In this the high demand and growth are reliabilities, high speed, convenient electronic product, area and battery lives. In logic circuit various techniques are implemented based on the XOR-XNOR circuit.

For better performances and improvement the design chip is scale down the device size of portable device and led the consumption of power system to increase the chip density and the complexity. So, the cooling of portable devices required expensive device and it will affect the life of the battery. Also, it's specified as short circuit power by the time duration power dissipation, static power by the various process of technology and dynamic power based on discharging and charging of load capacitance by equation (Jyotshna Kamath, B., Neetu Bani, 2014). For power consumption reduction of transistor switching is needed. Moreover the whole system is improved by the gate functions and adder enhancement with the adder data path of the circuit.

$$\text{Dynamic Power} = \alpha\,(VDD)\,2\,f\,CL \quad (1)$$

$$P = f_c v_{dd}^{\,2} + f I_{short} v_{dd} + I_{leak} v_{dd} \quad (2)$$

Where, switching activities is denoted as α, supply of voltage as VDD, the load capacitances switching clock frequency as f_c and frequency as f. C denotes the per cycle of clock capacitance, αnas activity factorof n node, node of voltage swing as Viswing, leakage circuit as I1 and the static circuit as Iisc.By the less supply of voltage the delay of the circuit is increased. However, the consumption of CMOS digital circuit power is signifying as in equation (Laya Surendran, E.K., P. Rony Antony, 2014) and the average powerdissipated as given below.

$$P_{total} = P_{dynamic}(Pd) + P_{static} + P_{short\text{-}circuit}$$
$$= V_{DD} \cdot f_{clk} \cdot \Sigma(V_{nswing} \cdot C_{nload} \cdot \alpha n) + V_{DD} \cdot \Sigma I_{isc} + V_{DD} \cdot I_l \quad (3)$$

The hybrid full adder topology input and output of sum and carry relationship is expressed and generating as below.

$$\text{Sum} = A \oplus B \oplus C \text{ and Carry} = AB + C(A \oplus B)$$

The proposed design circuit of hybrid full adder topology is based on dual rail pass transistor logic

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(DRPTL) with clock signal and inverter logic. The circuit flow and criteria for robustness is summarized in section wise. The related review of various adder circuit topologies is discussed in section II. In section III the proposed design circuit and its implementation is explained. In Section IV, the analysis of simulation results of proposed circuit improvement is shown. Finally, the proposed work concludes with future work in Section V.

Related Work:

In this section, the various full adder circuit performances and its functions are discussed. Generally in any application logic circuit is a major part of adder circuit for parameter consumption to enhance of performances and addressing at chip level. In adder cells, arithmetic system block is performed with the influenced of multipliers performances and the style of logic circuit considered is Shannon based adders, Pass transistor logic, Cmos logic and Transmission gates (Laya Surendran, E.K., P. Rony Antony, 2014).

The basis analysis of performances is based on the less propagation delay, less area, efficient power delay product (PDP) and low power (Manisha, Archana, 2014; Mathan, N. and A. Srimathi, 2014). Therefore the design of the logic circuit is built based on required performances and compared to various circuits for analysis of performances. The hybrid CMOS design achieves better performances than the existing by providing less delay, power, area, good drivability, noise robustness, PDP and energy (Sushil, B., *et al*., 2013; 2013; Mohammad ShamimImtiaz, *et al*.,). The circuit of Hybrid-CMOS Full Adder is shown in Fig [1].

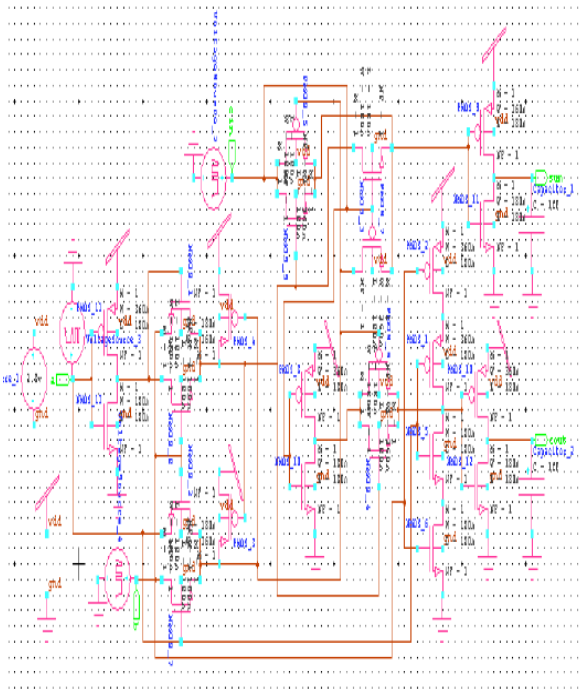

Fig. 1: Hybrid-CMOS Full Adder

The system circuit internal components provide an efficient process with low power and high speed. The essential components are used to design the sophisticated hardware circuits and multiplexer is performed based the topology of pass transistor full adder with less area and transistor count (Dillikumar, B., *et al*., 2012).

As well as the CMOS adder circuit is designed based on Tanner EDA using T-SPICEand define the design of the gate3T-XOR with its significant process (Jyotshna Kamath, B., Neetu Bani, 2014). The performances of the arithmetic and logic circuit of adder are illustrated the system performances as per the gate function. In digital systems, if adder lies on the critical path, then the delay of the overall system will increase (Geetha Priya, M., K. Baskaran, 2013; SubodhWairya, *et al*., 2011).

By using PTL-GDI technique in logic gate the transistor count is reduced in the adder circuit design and also reduces the power, delay and area (Vinaykumar, V., V. Viswanadha, 2014). So the upcoming adder circuit is designed based this technique for reducing the count of the transistor. In circuit implementation the function of sum and carry is carried out by Pass transistor logic and Gate Diffusion Technique (GDI) respectively. Both functions separate the count of transistor equally (Dillikumar, B., *et al*., 2012; HYBRID-CMOS LOGIC STYLE", 2012). The methodology for power consumption and high speed is implemented in the

ALU circuit of the 1-Bit XOR-XNOR full- adder circuits and illustrates the performances and compare results with the existing adder circuits show the proposed circuit best process with the faster efficiency and power (Sushil, B., *et al*., 2013; Vivek Kumar, *et al*., 2012).

In various CMOS logic styles the 1-bit full adder performed with the power dissipation and speed. The circuit is redesigned according to the logic style and the requirement of the transistor. For simulation Mentor Graphics ELDO simulations are used to evaluate the performances of the hybrid adder circuit (Rajkumar Sarma, Veerati Raju, 2012).

Generally PTL is used for the power consumption and the circuit is defined as LEAP (Also Single-Rail Pass-Transistor Logic). The consumption is based on the reduction of Switching activity, each node capacitance, short circuit current and voltage supply. The design of PTL is shown in Fig [2].

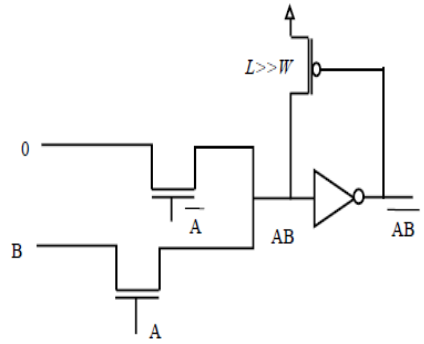

Fig. 2: Design of PTL

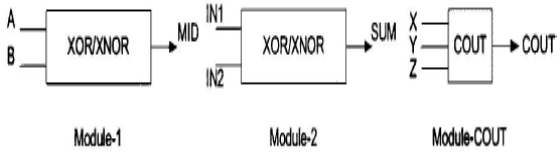

Fig. 3: Hybrid Full Adder Modules

The hybrid CMOS full adder is considering into three modules. In module I contain both the XOR and XNOR circuit else contain either one circuit. In module II contain the passing of intermediate signals and module III consists of generating the functions of the sum and carry output. As shown in Fig [3] the modules are performed. In this paper for better performances the Hybrid Full Adder Topologies is designed based on dual rail PTL with clock signal instead of Single Rail PTL.

Proposed Work:

In this section, the proposed hybrid topology of full adder circuit is designed and implemented with dual or double rail pass transistor logic (DRPTL). The hybrid topology of the proposed design provides better performances in reduction of power, transistor count, PDP, area, EDP leakage current, PEP and propagation delay. By the modification of single pass in to dual pass the performances are varied and show better performances than the existing. Also, it provides low consumption of power and less size of logic operation in VLSI design. The basic function of sum and carry is performed in the arithmetic operations with the reduction of chip power and area.

As per the adder function implementation with transistor the SUM and CARRY function is carried out. The state of the transistor will be varied on or off according to logic 0 and logic 1. Also, if logic is low, then the input of logic 1 else the logic is high by the logic input 0. According to this function the power dissipation is evaluated and it is higher in sum function than the function of carry. As like existing adder circuit the proposed circuit is implemented, but proposed circuit is the implementation of design circuit with DRPTL and clock signal in hybrid topology of full adder.

Proposed Hybrid Full Adder Topology - Sum Function:

The proposed structure is implemented based on inverter logic, dual or double rail pass transistor logic and parallel process with a clock signal to manage the circuit process. According to the style of logic the circuit is built with low consumption of power. Also, it generates with the hybrid function of logic gates.

Proposed Hybrid Full Adder Topologies - Carry Function:

The logic function determining only odd numbers and the output of logic will be equal to 1 only if the logic “1”input is higher than logic “0”. As per the clock function of signal the power management is performed on the circuit with the less transistor count, delay, area, and power; also with more robust, faster and reliable.

Sum = A $\oplus$ B $\oplus$ C;

Carry= AB + C (A $\oplus$ B);

In topology circuit, the complementary CMOS transistor is processed and obtained the results with voltage swings. For low power and complexity the proposed dynamic circuit is performed with fewer transistors and parallel function of dual transistor. Fig [4] shows the dynamic logic function implementation. The difference of single and dual rail system is shown in Fig [5]. In existing single rail signal system is implemented as a static logic design, but in the proposed circuit the design is implemented with the clock signal, Dual rail system, less transistor and dynamic logic. In dual system the process of signal and the logic is consisting at a same time in the circuit. In proposed circuit, as per the pass gate function the circuit is designed and implemented with dynamic access.

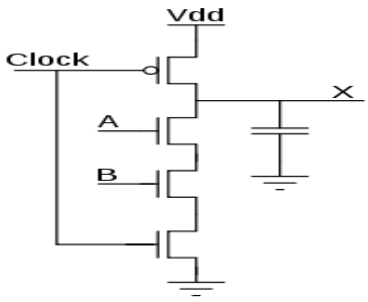

Fig. 4: Dynamic Logic Implementation

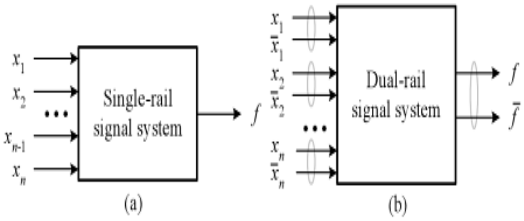

Fig. 5: (a) Single Rail Signal System, (b) Dual Rail Signal System

Proposed Dual Rail Pass Transistor Logic (DRPTL):

In this logic, Pass-Transistor is processed with the design of low power circuit. In pass network transistor is generated according to its function and perform sum and carry function as per the signal of a clock. At the end of generating voltage swing of the logic is performed. This logic provides improvement in speed, eliminating short circuit current in the output of inverter and includes voltage level restoration.

The DRPTL logic leads to have an efficient implementation with a clock signal for efficient dynamic access. It provides fast process and dynamic synthesis of logic functions in transistor network. Fig [6] shows the schematic diagram of the proposed hybrid circuit.

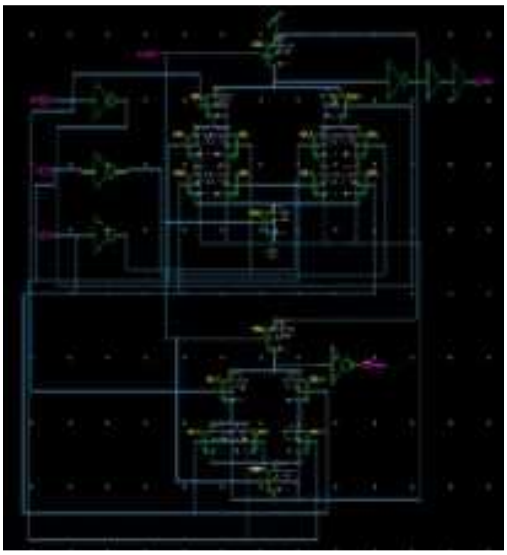

Fig. 6: Proposed SchematicDiagram – Hybrid Circuit based on Improved DRPTL

The proposed logic improves the dynamic circuit speed with the evaluation of clock signal logic with transistor. The supply of voltage is varied based on the charges phases. If the clock signal is equal to 1 in the evaluation phase, then the circuit will be discharged or pre-charge and if equal to 0 in pre-charge phase, then the circuit is charged and applies to voltage supply level from the transistor. This dynamic logic is used to evaluate the power dissipation with the switching of transistor gate to the voltage supply. The block diagram of the proposed Hybrid full adder topology based on proposed improved DRPTL logic is shown in Fig [7].

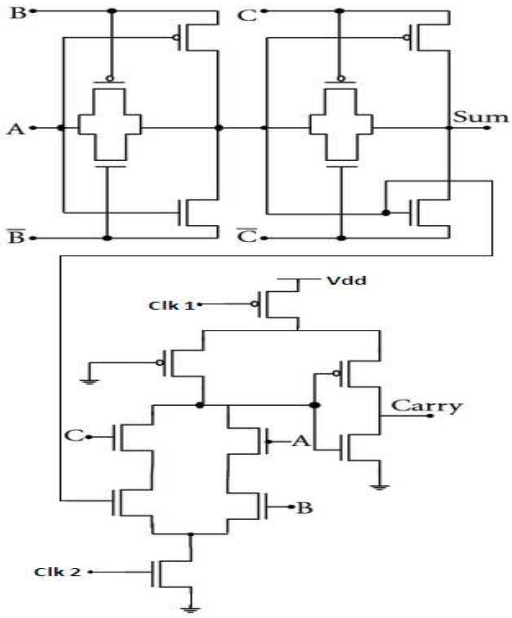

Fig. 7: Proposed – Hybrid Full Adder Topology

Simulation Results:

In this section, the proposed circuit simulation results are analyzed and shown the improved circuit efficiency than the existing circuit. From the range of voltage supply 0.6V to 1.8V the simulation is done for the comparison of design parameters with the existing full adder topology circuits. As well as the circuit is simulated at room temperature and the performancesare analyzed by implementing the proposed circuit using 45nm CMOS technologyon Cadence environment.

In the proposed system, due to less transistor usage only less area is required and the performances of the overall system are average at low supply of voltage. Below 1.1V the proposed design circuit is simulated and occupies the least silicon chip area. The schematic Cadence Virtuoso XL is used for design function of the layout. Fig [8] shows the test bench for simulation.

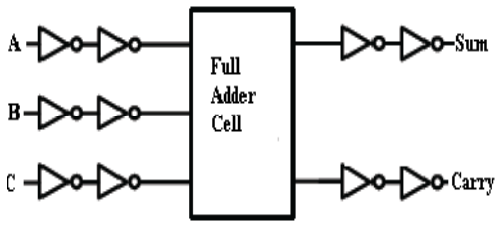

Fig. 8: Simulation Test Bench

The logic output, circuit delay, and the inverter power are estimated in the simulation process. It determines the full adder capacitance parasitic implies. In layout design of proposed circuit is considered with the improvement of system performances and provides more efficient, less area occupies and reliable process than the existing circuit in VLSI circuit by a layout design. By compact design the area reduction is possible and the layout of the proposed circuit is shown with its logic functions. The design style of the proposed circuit is implemented in the programming environment based

on Verilog HDL and the circuit is tested on Cadence tool.

The implementation of the proposed gate circuit is performed well with high redundancy. In VLSI, the proposed system optimizes the enhanced design to utilize the sub blocks in large circuit. The proposed logic design provides less count of transistor, less delay and less power dissipation. For efficient implementation of large VLSI system the proposed circuit is extremely enviable. The proposed design circuit layout is simulatedusing 45nm CMOS technology. The functional layout of sum and carry is shown in Fig [9] and Fig [10].

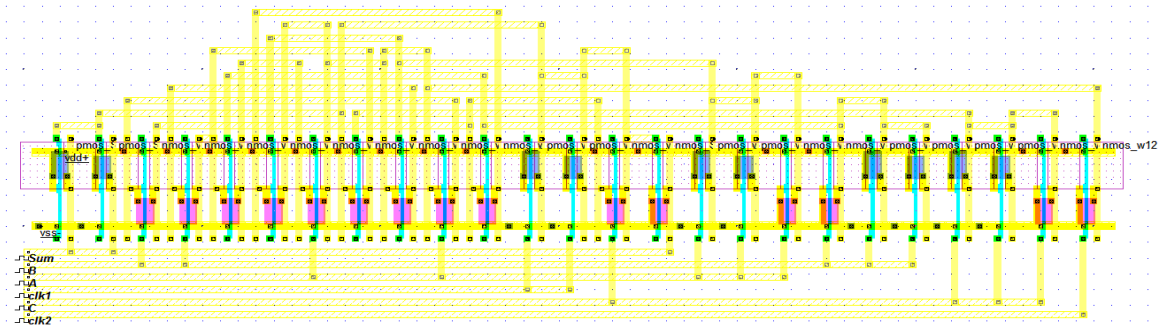

Fig. 9: Proposed Hybrid Full Adder Topology - Sum Function

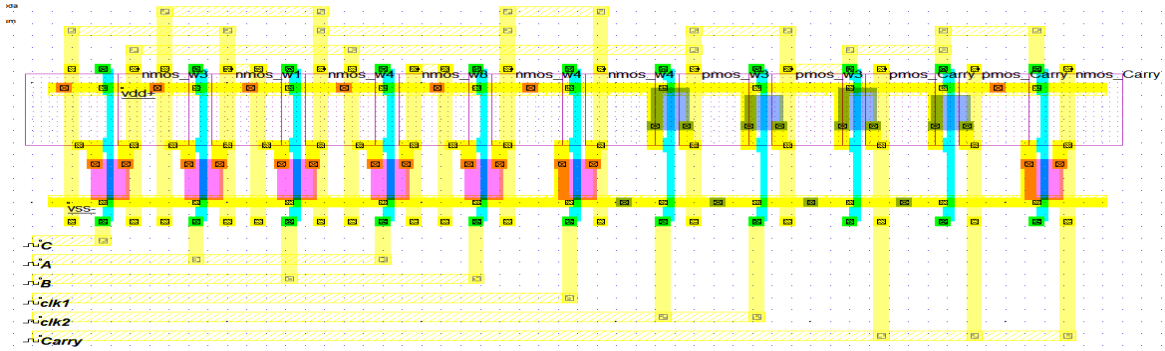

Fig. 10: Proposed – Hybrid Full Adder Topology – Carry Function

Table 1: Comparison of Logic Circuit

Parameters	XOR-XOR	XNOR-XNOR	Centralized	SRPTL	Improved DRPTL
No. Transistors	24	24	24	19	17
Power	0.588mW	0.788uW	84.257uW	3nW	2.5nW
Delay	3000ps	3000ps	3000ps	2000ps	1500ps
PDP(Power Delay Product)(Femto/sec)	1.764	2.364	2.537	6E-3	5E-4
EDP(Energy Delay Product) (Femto/sec)	5.21E-6	7.092E-9	7.611E-7	12E-11	10E-13
Leakage Current	1.525mA	1.498mA	0.486mA	0.001mA	0.85 nA
PEP(Power Energy Product) (Femto/Sec)	6.098	1.812	2.137	5.4E-5	4.3e-5

Proposed Circuit - Hybrid Full Adder Topologies based Improved DRPTL:

As per the results of simulation at every stage of path critical of the circuit the performances are analyzed and optimized the proposed circuits. During the process the logic may degrade to “1” because of the threshold voltage drop else preventing the transistor inverter to ON tuning. Table [1] illustrates the performance comparison of various existing circuits with proposed circuit. The comparison parameters are EDP, Power, Delay, PDP, Transistor Count, PEP and Leakage current. As per the logic process the performance analysis is maintained and considered with less voltage operation.

The sub-threshold voltage leakage is becoming a rigorous control against to low power consumption. But compare to existing leakage in the proposed circuit reduce the leakage level and provides better and efficient power consumption. Also, it improves the speed and maintains the flow dynamically.

The simulation results of proposed circuit are considered with the logical functionof sum and carry. According the circuit simulation the function of a Sum and Carry is carried out as shown in Fig [11] and Fig [12] respectively.

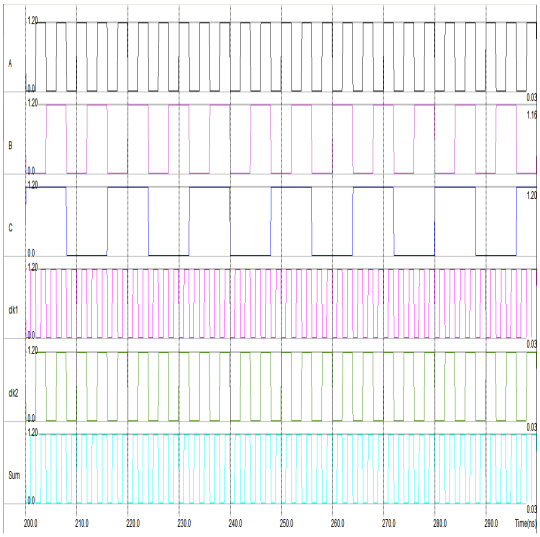

Fig. 11: Simulation of Proposed Circuit - Sum Function

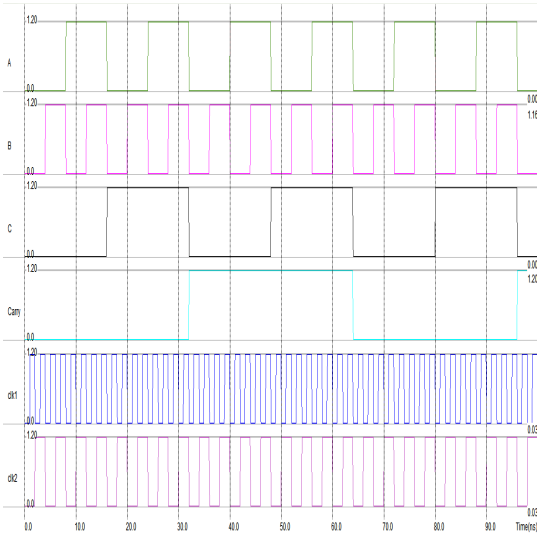

Fig. 12: Simulation of Proposed Circuit - Carry Function

Conclusion and Future Work:

An internal logic circuit is proposed with the proposed approach to design and implement the circuit for efficient performances and analysis than the existing circuit. The proposed approach of the hybrid circuit provides faster process, less delay propagation, less power consumption and reduction in transistor count than the others. The proposed circuit performed with the logic improvement of dual and parallel process with clock signal in the proposed circuit. By the proposedstyle of hybridCMOS design with improved DRPTL the performances are evaluated by simulating the circuit at room temperature in 45 nm CMOS process technology. Finally, the proposed circuit shows more efficient and better performances with its improvement over the existing circuit.

Future work, the logic design simulation is needed to explore with low voltage supplyfor deep submicron technologies. In addition, with complete well-matchedthe logic gates involvement shouldbe implemented for less count of the transistor.

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