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A Novel Coconut-Tree based Clock Distribution Network for High-Speed FFT architecture

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ABSTRACT

Background: Conventionally, there are many types of clock distribution systems such as H-Tree, Binary Tree, Two level X-tree, Fish-bone tree, etc. to provide clock signal to each system block. These systems suffer due to the delay and high power consumption. Hence, an improved clock distribution system is required to overcome the existing issues. **Objective:**This paper proposes a novel clock distribution network for high speed Fast Fourier Transform (FFT) architecture by using the Flip-Flop (FF) clustering method. In this proposed system, a coconut tree based clock distribution system framework is implemented to provide asymmetric clock signal to all the components in the FFT architecture. The merging of FFs is performed by using the Manhattan distance calculating method. Initially, the FFs are arranged into clusters and then merged based on the minimum distance level. Then, clock signal is distributed asymmetrically to each cluster, when the cluster arrangement lies within the acceptable limit of distance. During arrangement of clock distribution, Pulsed-Latches and FFs are placed at each distribution stage. This reduces the load and supplies the clock signal equally to each component with reduced amount of delay level. Effective clock distribution is achieved by using a coconut tree based structure that can handle more number of leaf edges in asymmetrical manner. This type of merging and clock distribution arrangement reduces the wire length, critical path delay due to its reduced amount of area. **Results:**The performance of the proposed system is evaluated by comparing it with the existing system. **Conclusion:**The proposed system achieves better performance in terms of area, delay, clock frequency, power consumption, latency, slice register, slice Look Up Table (LUT), occupied slice and LUT FF pairs.

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INTRODUCTION

The increase in the design complexity and performance of the Integrated Circuits (ICs) requires the clock distribution network (CDN). The CDN consumes more power, due to its operability at high frequency range and high capacitance values. In modern devices, appropriate routing of the multiple clock domains is mainly required to achieve the essential clock arrival time for each register. It is necessary to maintain the correct operation of the circuit, during the occurrence of environmental changes, electrical fluctuations and process variation for devices. While mainly focusing on the device delay, the interconnect delay is also an important issue in the clock networks. The tree-based clock distribution is the most preferred method in Very Large Scale Integration (VLSI) designs.Generally the clock trees are classified as symmetric and asymmetric clock trees(Chattopadhyay & Zilic, 2012). Symmetric clock trees are the most widely studied clock distribution topologies. The clock source is considered as the root and the clock destinations are referred as leaves. The number of levels in the tree is represented by the number of branches in the clock distribution route. In a Y-tree, each branch point divides into a pair of branches of same size and shape, but different orientation. In an H-tree, the clock signal is divided along the two parallel branches. In the H-tree, wire length is constant for every segment and is halved for each succeeding level. Since the wires are located along the horizontal and vertical directions, the H-structures utilize Manhattan routing. An X-tree structure replaces the horizontal and vertical wires with diagonal wires by reducing the interconnect length. But they are not always realizable. Figure.1 shows the three symmetric tree structures.

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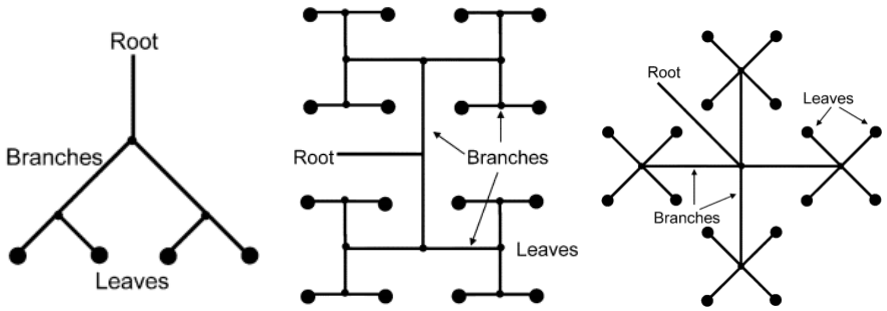

(a) (b)(c)

Fig.1:(a) Y-Tree structure (b) H-Tree Structure and (c) X-Tree Structure

The fan-out for these tree structures is usually too large, irrespective of the complete passiveness of the trees without buffering. There is a need for symmetrical placement of the clock buffers at arbitrary intervals. The impedance needs to be matched at each branching point. Asymmetric Buffered Clock Trees are commonly used in integrated circuits (ICs) and ASICs. The location and timing requirements of each leaf are used to create a suitable tree. The delay is adjusted by varying the size and number of the buffers, fan-out at each branch point and wire length. Due to the dependency of the asymmetric clock tree between the registers, even small change in the design can cause a major impact on the clock network. Figure.2 shows the asymmetric clock tree.

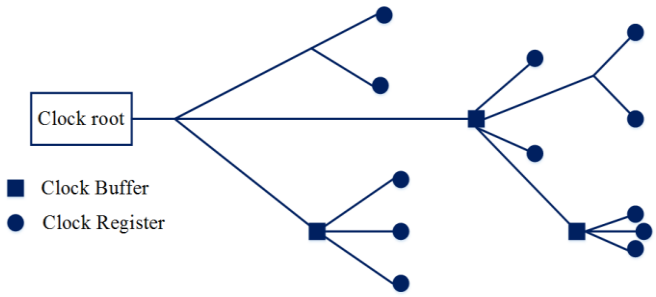

Fig.2: Asymmetric clock tree

To mitigate the drawbacks of the existing clock tree structures, a novel clock distribution network for high speed FFT architecture by using the FF clustering method is proposed in this paper. In this proposed system, a coconut tree based clock distribution system framework is implemented to provide asymmetric clock signal to all the components in the FFT architecture. The merging of FFs is performed by using the Manhattan distance calculating method. Initially, the FFs are arranged into clusters and then merged based on the minimum distance level. Then, clock signal is distributed asymmetrically to each cluster, when the cluster arrangement lies within the acceptable limit of distance. During arrangement of clock distribution, Pulsed-Latches and FFs are placed at each distribution stage.

The major contributions of this paper are

1. Pulsed-Latches and FFs are placed at each distribution stage. The pulsed latches can effectively reduce power consumption of the FF designs. This reduces the load and supplies the clock signal equally to each component with reduced amount of delay level.
2. The coconut tree based structure can asymmetrically handle more number of leaf edges, than the existing tree structures.
3. FF merging and clock distribution arrangement reduce the wire length and critical path delay due to its reduced amount of area.

The rest of the paper is structured as follows: Section II describes about the conventional research works related to the power efficient clock generation and distribution methodologies. Section III explains the proposed coconut tree based clock distribution network in detail. Section IV illustrates the performance evaluation results of the proposed FFT architecture. The conclusion and future scope of the proposed work is discussed in the section V.

Related Work:

This section explains about the conventional research works related to the clock distribution approaches. Non-tree CDN such as mesh and crosslink were employed to mitigate the clock skew variations. However, it leads to the increase in the dissipated power, while consuming a significant amount of metal resources. Several approaches have been proposed to reduce the power consumption and

wire length to reduce the skew in the CDN.A new paradigm for clock distribution was proposed for the distribution of a global clock signal with the reduced power consumption rate. The current-mode (CM) CDN exhibits lower power consumption and higher operating speed, in comparison with the traditional voltage mode clocks. The need for the complex receiver circuit and local Voltage-Mode (VM) buffers to drive the clock sinks was also eliminated (Islam & Guthaus, 2015).

Zhao et al focused on the designing and analysis of the low-power and low-slew clock network for three-dimensional (3D) stacked ICs. A 3D clock tree synthesis method was developed based on the 3D method of mean and median algorithm. The 3D-MMM algorithm was extended to determine the optimal number of through-silicon via to be used in the clock tree, for the efficient reduction of the overall power consumption (Zhao, Minz, & Lim, 2011).*Xu et al* investigated the combined effect of power supply noise and process variations on clock skew and jitter. The tradeoff between the limitations on the jitter constraints, power consumption, skew and slew rate of the CDN were discussed. The effect of the recombinant trees and dynamic voltage scaling in the reduction of skew and jitter were also analyzed (Xu, Pavlidis, Burleson, & Micheli, 2012).

Kancharapu et al presented a current-mode CDN (CMCDN) for low-power and low-skew on-chip clock distribution. The performance of the proposed network was analyzed and simulated under variations of the operating parameters. The power consumption of the proposed network was reduced when compared to the VMCDN (Kancharapu, Dave, Masimukkula, Baghini, & Sharma, 2011).*Abdelhadi et al* introduced an efficient algorithm to minimize the clock skew variations, power dissipation and metal area overhead. A variation-resistant hybrid CDN was produced by using the combination of non-uniform meshes and unbuffered trees. The algorithm was tested on various benchmark circuits and compared with non-uniform mesh construction methods. Effective reduction in the metal area and power dissipation rate was achieved (Abdelhadi, Ginosar, Kolodny, & Friedman, 2013).

A dual edge triggered FF design was proposed to reduce the power consumption in the CDN. The proposed design was compared with the existing Conditional Data Mapping and Clocked Pair Shared FF designs. The redundant transitions of the internal nodes were eliminated by using the proposed design (Noble & Sakthivel, 2013).A novel low-power pulse-triggered FF design was presented to ensure maximum power conservation. The circuit complexity was reduced by using the transistor and gate design. The size of the transistor in delay inverter and pulse generation circuit was reduced to enable power saving. The average leakage power consumption was reduced efficiently, when compared to the traditional FF design (Hwang, Lin, & Sheu, 2012).

The random characteristics of the TSV-based 3D clock networks was studied and several design parameters were investigated. The random effects were reduced by using fewer number of buffers and short interconnects. Low power dissipation and small skew variation in the 3D clock networks were achieved by using the multi-TSV strategy (Zhao, Mukhopadhyay, & Lim, 2011).Presented a novel methodology for low-jitter clock generation and distribution by using Standing Wave Oscillators. The jitter, power consumption and skew of the proposed methodology were reduced, when compared to the existing schemes (Mandal, Bollapalli, Jayakumar, Khatri, & Mahaptra, 2013).Designing a low power clock network in the 3D circuits is a challenging task due to the increase in the power densities. Resonant clock networks were considered as the efficient alternatives for low power dissipation, when compared to the conventional clock distribution schemes. Additional inductive circuits were used to deliver clock signal to the sink nodes and enable reduction in the power consumption when compared to the existing buffered clock network (Rahimian, Pavlidis, & De Micheli, 2011).

Reuben et al designed a clock frequency doubler (FD) circuit to reduce power consumption in the CDN. The frequency around the specific frequency ranges was doubled upto 10%. Reduction in the power consumption rate and propagation delay of the proposed circuit was achieved (Reuben, Anuroop, & Kittur, 2012).A novel 3D CDN was proposed with distributed multi-TSV. The proposed network has achieved better performance in terms of skew, power consumption, jitter and area consumption (Kim *et al*., 2011).*Savidis et al* explored the clock distribution topologies in a three-tier 3D IC. The delay from the root node to the leaf node on each plane of the IC was determined. The resulting modeled delays were compared with the experimental data. Optimal agreement between the simulation and experimental data was achieved (Savidis, Pavlidis, & Friedman, 2011).

A probabilistic prototype of the clock gating network was developed to quantify the expected power saving effect and the indirect overhead. The optimal fan-out of the network was derived based on the toggling probabilities and process parameters of FFs. Reasonable saving of the total clock tree switching power was achieved by the proposed methodology (Wimer & Koren, 2012).A clock skew modeling method was implemented to enable a detailed analysis on the clock skew variations in the clock tree elements due to the temperature. Accurate SPICE-level timing analysis was performed to capture the inverted temperature dependencies of the active transistors. From the simulation results, it was clearly observed that the larger skew variations occurred under thermal conditions (Sassone *et al*.,

2013).Misra and Paliwal proposed a methodology for reducing the power consumption level of the clock distribution system based on the clock voltage and frequency scaling. A frequency doubler and power-saving level converter were used for restoring the clock levels and frequencies at the leaf node of the clock. The power consumption was reduced during transformation from the lower frequency to the higher frequency (Misra & Paliwal, 2014).

A novel dual-edge triggered sense-amplifier FF was presented for deployment in the low-power and high-performance application. A clock-gated sense-amplifier was used for the efficient reduction of the power consumption rate during the low switching activities (Phyu, Fu, Goh, & Yeo, 2011).*Lin* presented a low-power FF design based on the signal feed-through scheme. The problem of the long discharging path was solved successfully to achieve better operating speed and power performance (Lin, 2014).A power-driven FF merging and relocation approach was proposed to reduce the size and power consumption of the CDN. The switching power of the grids connected to the FFs was controlled due to the selective merging of the FFs into multibit FFs and relocation of the FFs under the timing and placement constraints. Finally, the total switching capacitance of the network and grids was reduced (S.-H. Wang, Liang, Kuo, & Mak, 2012).

A novel active deskew technique was proposed for the adaptive reduction in the cross-tier variations and 3D wiring asymmetry. A phase-mixer-based tunable-delay-buffer was designed to withstand process-voltage-termperature variations. An efficient clock distribution network topology was proposed based on the deskew technique abd buffer design. Moreover, a thermal profile-based optimization flow was developed to improve the power efficiency and reduce the design overhead (Chen, Zhu, Davis, & Franzon, 2014).The difficulty of the conventional CDN structures for multi-GHz ICs are increasing nowadays, due to high power consumption rate. To overcome the difficulties, this paper proposes a novel clock distribution network for high speed FFT architecture by using the FF clustering method.

Novel Clock Distribution Network:

This section explains about the proposed methodology in detail. A novel clock distribution network for high speed FFT architecture by using the FF clustering method is proposed in this paper. In this proposed system, a coconut tree based clock distribution system framework is implemented to provide asymmetric clock signal to all the components in the FFT architecture. The merging of FFs is performed by using the Manhattan distance calculating method.

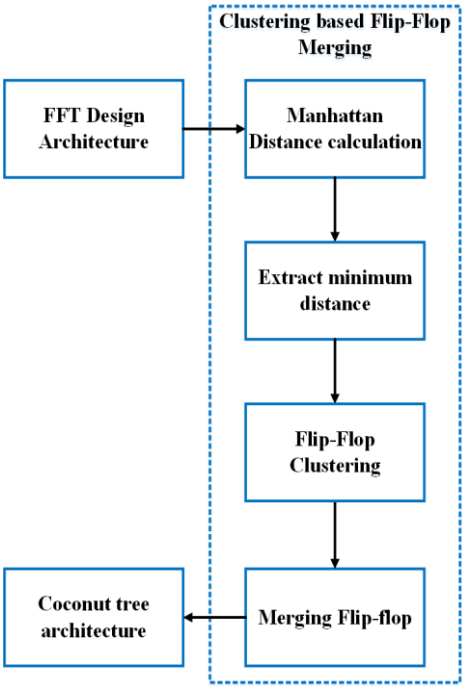

Fig.3: System architecture of proposed system

Initially, the FFs are arranged into clusters and then merged based on the minimum distance level. Then, clock signal is distributed asymmetrically to each cluster, when the cluster arrangement lies within the acceptable limit of distance. During arrangement of clock distribution, Pulsed-Latches and FFs are placed at each distribution stage. The coconut tree based structure can handle more number of leaf edges in asymmetrical manner, to achieve effective clock distribution. Figure.3 shows the system architecture of the proposed system. The main stages of the proposed system are

- Clustering-based FF merging
- Coconut tree architecture
- FFT Architecture
- Proposed FFT RTL

Clustering-based FF Merging:

Merging of FFs avoids the duplicate inverters and reduces the total power consumption of the clock. The wire length and critical path delay are reduced due to its reduced amount of area. In our proposed work, clustering based FF merging is performed. A clustering algorithm is proposed to find the nearest possible clustering of FFs flops for FF merging. Amongall current clusters, the clusters having minimum distance interval is chosen. The selected clusters are replaced with a new cluster, formed by merging the two clusters. This algorithm finds the clusters of FFs and finally combines the FF clusters to reduce the wire length. The flip flops are formed in clusters according to the distance information. This clustering represents the merging of flip flops to form a multi-bit flip flops.

Clustering Algorithm

Input: FF Position, 'F_p'
Output: Cluster result, 'C_o'
Step 1: Coordinated of FFs, $X_{ij} = \{x_{1,1}, x_{1,2}, \dots, x_{m,n}\}$
Step 2: Find distance between FF by using Manhattan distance formula
Step 3: Find minimum distance from D_{ij} table
Step 4: Merge FFs and Update table
Step5:Update coordinates
Step 6: $C_o = X_{ijc}$ //Update Cluster.
Step 7: Repeat Step 2 to 6 until empty of individual FF nodes.

The Manhattan distance function computes the distance between two FFs. The Manhattan distance is the sum of the differences of the points $X_i = (x_{i1}, x_{i2}, \dots\dots, x_{in})$and $X_j = (x_{j1}, x_{j2}, \dots\dots, x_{jn})$. The distance between the FFs is calculated by using the Manhattan distance formula given as

$$D_{ij} = \sqrt{\sum_{k=1}^{l} (X_{ik} - X_{jk})^2} \quad (1)$$

Where, 'i, j' are the indexes of FFs and 'l' is the length of distance matrix.The minimum distance between the FFs is found from the D_{ij} table.

$$mn = \min(D_{ij}) \quad (2)$$

Then, the FFs are merged into clusters and the D_{ij} table is updated. The coordinates of the clusters are updated.

$$X_{ijc} = \{\{x_{1,1}, x_{1,2}\}, \dots, \{x_{m-1,n-1}, x_{m,n}\}\} \quad (3)$$

Where 'c' is the number of clusters. The FF merging process is shown in the Figure.4.

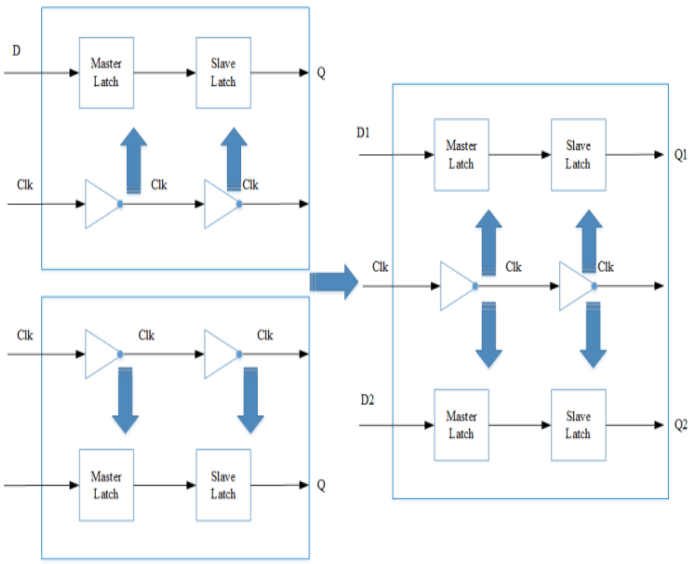

Fig.4: Flip-Flop Merging

Coconut-tree Architecture:

In this process, after extracting the merged FFs of cluster formation, the pulsed latches are placed on the center of the cluster. Pulsed latches are latches triggered by a short clock signal generated from a pulse generator. While triggering a latch with the pulse clock waveform, the latch is synchronized with the clock. The timing behavior of the latch is similar to an edge-triggered FF. Hence the power consumption is reduced effectively. Then, a clock line is connected from the Root clock link to the merged FF groups in the form of tree-shaped structure. A coconut tree based clock distribution system framework is implemented to provide asymmetric clock signal to all the components in the FFT architecture. The coconut tree based structure is able to handle more number of leaf edges in asymmetrical way, to achieve effective clock distribution. The conventional X-tree and H-tree structures comprises 16 nodes. But, our proposed coconut tree architecture provides 20leaf nodes. The coconut tree architecture is shown in the Figure.5.

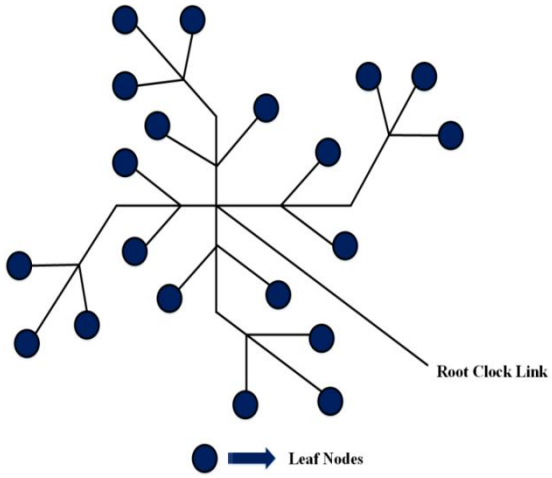

Fig.5: Coconut tree architecture

FFT Architecture:

Using the FFT transform, signals can be moved to the frequency domain where filtering and correlation can be performed with fewer operations. The FFT is calculated by decomposing the given sequence of N-length into smaller sequences and then combining them to get the total transform. The FFT architecture mainly consists of a address generation unit, butterfly processor, coefficient ROM, dual-port RAM and controller. The process of writing data into the dual-port RAM during FFT computation is performed after reading the first data from the RAM. The FFT architecture is formed as shown in the Figure.6. Here, 'D' is the delay lines and 'A' is the adder structure.

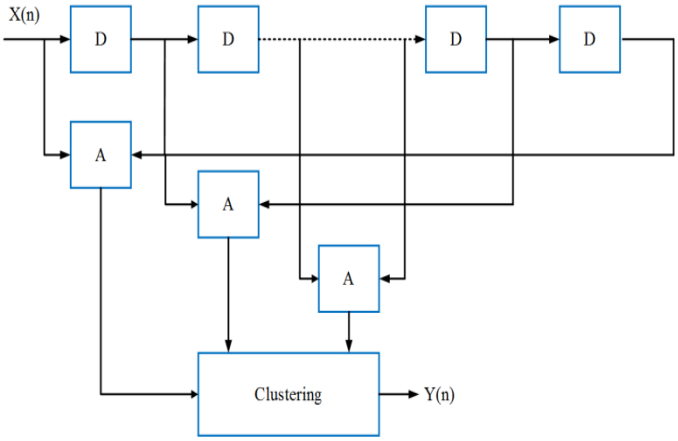

Fig.6: FFT architecture

Proposed FFT RTL:

The schematic diagram of the RTL is shown in the Figure.7. The RTL is implemented using resistors and transistors. RTL obtains a substantial amount of power for each gate, from the power supply. The transistors are used to combine multiple input signals, for amplifying and inverting the combined input signal. A supplementary transistor is included for re-inverting the output signal. This combination provides clear output signals that are either inverted or non-inverted. In the RTL logic, the voltage V_L should be low enough for the corresponding

transistor to be cutoff, when V_L is applied to the gate input. V_H should be capable of driving the transistor into saturation. It is necessary that V_L<0.6, the cut-in voltage of the emitter-base junction and V_H be greater than or equal to the applied voltage, to bring the transistor to saturation. If the input of the RTL gate is high, the corresponding transistor is driven to saturation state. This causes the output to be low, irrespective of the operating states of the other transistors. If all the inputs are low, all transistors will be cut off, because V_{BE}<0.6 V. Hence the output at this state will be nearly the supply voltage.

1) Twiddle Factor:

A twiddle multiplication stage is applied after every butterfly stages. In each twiddle stage, a complex multiplier is used to multiply a corresponding complex twiddle coefficient of unit magnitude with each data sample. Then, the product is then truncated down to the bit width of the data stream before entering the subsequent butterfly stage. The twiddle factor is referred to the complex multiplicative constants during the operations of the butterfly architecture. The twiddle factor is defined as

$$W_N = e^{-\frac{j2\pi}{N}} \quad (4)$$

Where, 'N' is the number of samples. The exponential term of the twiddle factor is resolved by the Euler's identity.The twiddle factor exhibits periodicity property and symmetry property. This is given as

$$W_N^{k+N} = W_N^k \quad (5)$$

$$W_N^{k+\frac{N}{2}} = -W_N^k \quad (6)$$

2) Butterfly Architecture:

The butterfly architecture is the main unit of the FFT processor. It obtains two data words from a memory and computes the two point FFT. The FFT computational results are written to the same memory locations. The butterfly processor comprises a single multiplier and two adders. It computes one butterfly every four cycles. A multiplier computes the partial product value of the complex multiplication and generates a 32-bit signed fraction result. A first adder sums the cross product values of the complex multiplication. A second adder produces the addition and subtraction outputs of the butterfly operation. The butterfly processor has a latency of five cycles. The butterfly processor calculates the sum and difference of two input data, and computes the product of the difference and twiddle factors.

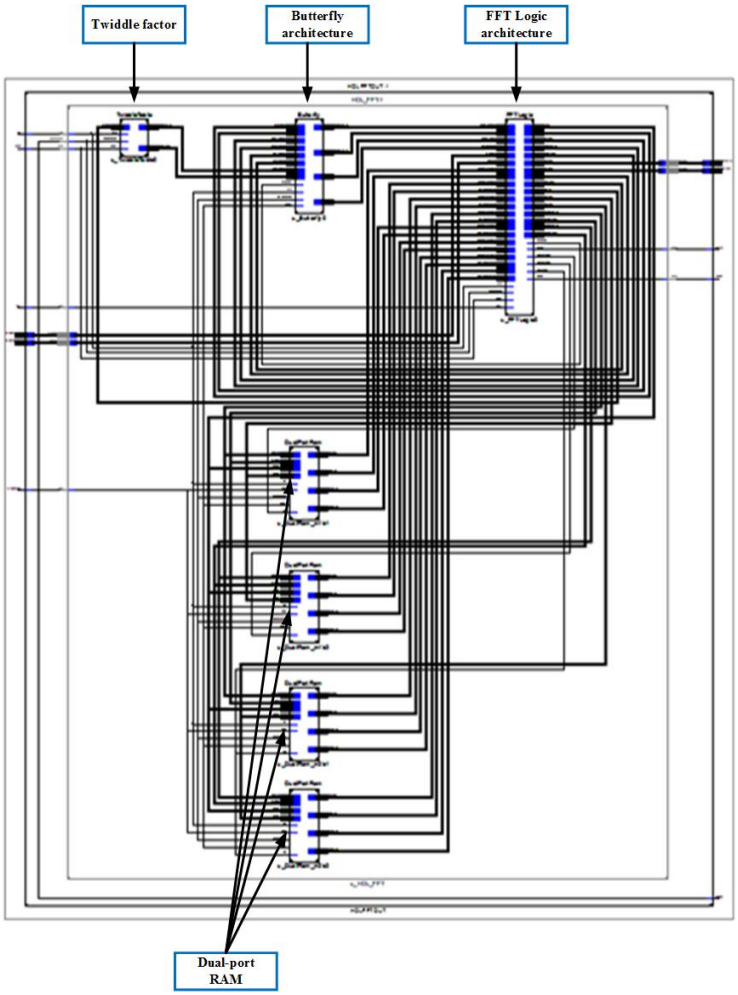

Fig.7: Schematic diagram of RTL

Performance Analysis:

This section presents the performance evaluation results of the proposed framework.The proposed FFT Architecture is compared with the Single-Path Delay Commutator/Single-Path Delay Feedback (SDC/SDF) (Z. Wang, Liu, He, & Yu, 2013) and Radix-2 architecture (Cho, Lee, Park, & Park, 2011). The power consumption level of the proposed FFT architecture is also analyzed.

Table I: Comparative Analysis of the area and performance of the proposed FFT and SDC-SDF architectures

AREA AND PERFORMANCE OF THE PROPOSED FFT ARCHITECTURES FOR 16 BITS						
Methods	Area				Frequency (MHz)	Latency (ns)
	LUTs	FFs	DSPs	BRAMs		
SDC-SDF	672	522	4	0	322	140
FFT architecture	553	343	4	0	349.4	120

Table I shows the comparative Analysis of the area and performance of the proposed FFT and SDC-SDF architecture for 16 Bits. The number of Look-Up Table (LUT), FFs, Digital Signal Processors (DSPs) and Block Random Access Memory (BRAM) of the proposed FFT is found to be comparatively lower than the existing SDC-SDF architecture. The frequency of the proposed FFT is higher than that of the SDC-SDF architecture. The latency of the proposed FFT is lower than the latency of the SDC-SDF architecture.

Table II: Comparative Analysis of Performance of 64-point 1 MHz FFT processor

Performance of 64-point 1MHz FFT processor using 4 real multipliers		
Parameters	Radix - 2	FFT Architecture
Power (mW)	204	114
Latency (Sec)	411 μs	120 ns
Slice Register	614	344
Slice LUT	490	553
Occupied Slice	245	184
LUT FF Pairs	576	576

Table II Comparative Analysis of Performance of 64-point 1 MHz FFT processor using 4 real multipliers. The performance of the 64-point 1MHz FFT processor is compared with the Radix-2 architecture. The proposed FFT processor achieves better performance in terms of power, latency, slice register, slice LUT, occupied slice and LUT FF pairs.

Table III: Logic Utilization Analysis

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	343	93120	0%
Number of Slice LUTs	648	46560	1%
Number of fully used LUT-FF pairs	301	690	43%
Number of bonded IOBs	71	240	29%
Number of Block RAM/FIFO	4	156	2%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	4	288	1%

Table III shows the logic utilization analysis. The utilization rate of the number of slice registers, slice LUTs, fully-used LUT-FF pairs, bonded Input Output Blocks (IOBs), block RAM/First-In/First-Out (FIFO), Global Clock Buffers (BUFG/BUFGCTRL) and Digital Signal Processors (DSP) is illustrated in the table.

Figure.8 shows the on-chip power analysis plot. The leakage power, clock power, power consumed by the logic gate, DSP, Phase Locked Loop (PLL), Mixed-Mode Clock Manager (MMCM), Phaser,Peripheral Component Interconnect Express (PCIE), Input-Output (IO) and Gigabit Transceiver(GTX) are shown in the plot. From the graph, it is clearly evident that the proposed architecture consumes less amount of power. Hence the proposed architecture is found to be efficient.

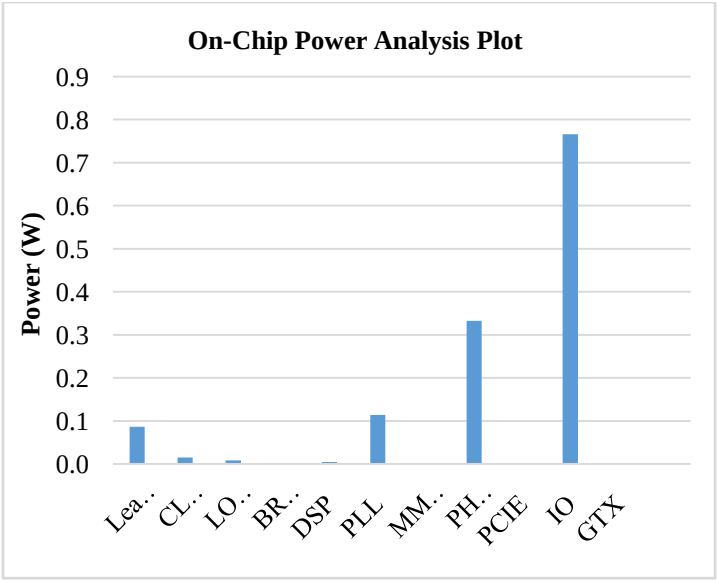

Fig.8: On-Chip power analysis plot

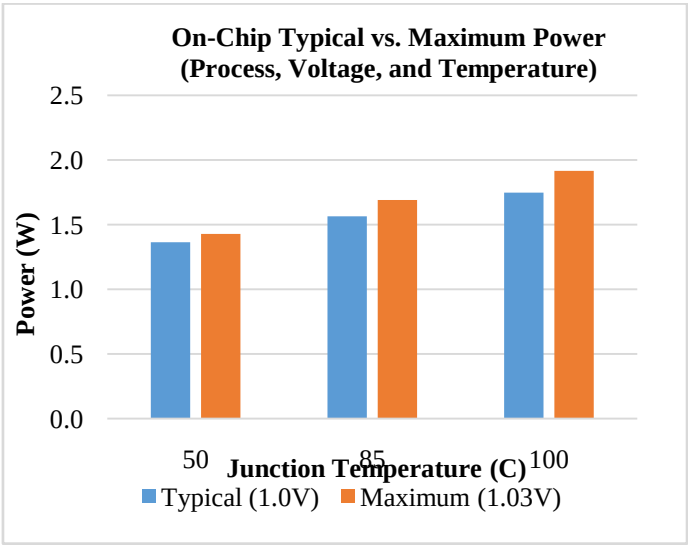

Fig.9: On Chip Typical and Maximum Power analysis plot

Figure.9 shows the on-chip typical and maximum power analysis plot. The proposed architecture achieves maximum power efficiency with the increase in the junction temperature.

Conclusion And Future Work:

The conclusion and future scope of the proposed work are discussed in this section. A novel clock distribution network for high speed FFT architecture is presented in this paper. Merging of FFs is performed by using the FF clustering method. The distance between the FFs is calculated by using Manhattan distance calculating method. Initially, the FFs are arranged into clusters and then merged based on the minimum distance level. Then, clock signal is distributed asymmetrically to each cluster, when the cluster arrangement lies within the acceptable limit of distance. During arrangement of clock distribution, Pulsed-Latches and FFs are placed at each distribution stage. This reduces the load and supplies the clock signal equally to each component with reduced amount of delay level. Effective clock distribution is achieved by using a coconut tree based structure that can handle more number of leaf edge in asymmetrical manner. This type of merging and clock distribution arrangement reduce the wire length, critical path delay due to its reduced amount of area. The performance of the proposed system is evaluated by comparing it with the existing system. The proposed system achieves better performance in terms of area, delay and clock frequency. In future, this form of clock distribution system is presented in the application of Multiplier design in FFT architecture to reduce the number of multipliers and adders.

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