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Efficient Implementation of ESVPWM for Single Phase H-bridge Multilevel Inverter

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ABSTRACT

Nowadays, the technology of multilevel inverter is a major part of energy control with medium voltage and high power. This technology emerges with control and modulation method. Enhanced Space Vector Pulse Width Modulation (ESVPWM) is designed and proposed triangular approach with five level single phase cascaded H-bridge multilevel inverter (SPCHMI). It processes with the reduction of switching loss and harmonic in the area of developmental ESVPWM. It performs under condition changing of load. The turning of IGBT switches is performed efficiently by the proposed circuit with single phase than the existing circuit. The proposed control strategies of the system manage the voltage and make flexible with less switching loss and low voltage distorted. The results are evaluated by simulating the ESVPWM circuit in MATLAB/SIMULINK. The performances of the proposed circuit is analysed the simulation results and shows better performances of waveform, high efficiency, less voltage stress and high speed computational.

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INTRODUCTION

In past few years power converters have grasp attention of the multilevel inverter in various applications. By the contents of harmonic lower order reduction the conventional two-level inverters become a major advantage for usage in power converters. Most of the review of the inverter is based on the generation of modulating signals. Various modulation methods have been used in the inverter for generating the signal according to the topology construction of the inverter. In multilevel inverter stable process of high power and voltage, switching frequency reduction and the switching devices count reduction are included in the modulation circuit.

Due to modularity significance the inverter of Cascaded H-bridge multilevel inverter has become a faster development which is considered in Digital PWM generation as an inverter and modulation technique instead of conventional sinusoidal PWM. The scope of the inverter is possibility of harmonic distortion reduction and simplicity of implementation (Abdul Kadir, M.N., *et al*., 2010).

The multiple carrier signals of Disposition and phase shifting is carried out in some method based on the requirements of inverter operation. In power electronics application digital controller is used for better performances and low cost. It also becomes a common solution for the issues of reusability and portability of the converter in PWM. Basically the choice of the implementation is higher-level language and coupled with the microprocessor parameters specified.

In digital processor the feature availability imposed by changes and cheaper, according to the requirements. It also required programming code revision to provide efficient access with time consuming and less cost. The issue of the tools is almost emerging with the devices and it is resolved by applying a modulation technique and switching components. In fact, the inverter is designed with the control standard and complex algorithm is required to control the device (Fang Zheng Peng, 2002).

In this paper ESVPWM circuit is designed with five levels SPCHMI for efficient process and used to generate the circuit to show better performances than the existing.

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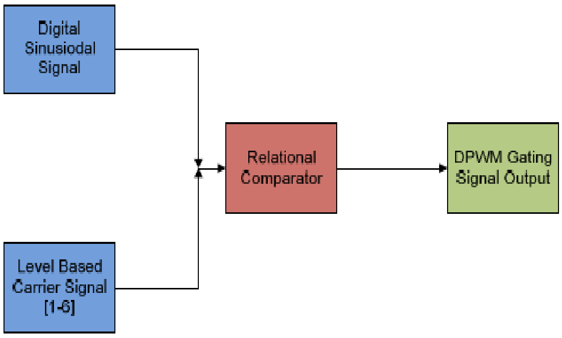

Fig. 1: PWM Signal Model Generation

As shown in Fig (Sameer Pratap Singh, *et al*., 2015) the generating of the PWM signal model is carried out and the index of modulation is defined as:

$$M = V_m / 2V_c \quad (1)$$

Where V_m is denoted the digital sinusoidal wave peak value and V_c as carrier peak value.

In system interfacing the voltage source inverter (VSI) is used for renewable sources of energy. The VSI is managed based on feedback of current and voltage. Also, it preferred the current controlled VSI for the dynamic performances and protection of current characteristics. The Conventionally PWM method is used to generate the pulse of gate for switching the inverter to have the voltage output. As well as various PWM techniques are implemented, but for the technology development of microprocessor space vector modulation (SVM) is used.

In this paper for the development of technology ESVPWM is proposed and designed for line-to-line voltage result based on triangular approach. Also, it provides flexible access with fixed frequency switching, harmonic spectrum reduction, optimum pattern of switching and utilization of voltage DC link.

The rest of the paper is organized into section wise. In section II the related review of the PWM and its inverter operation is discussed. The design and implementation of the proposed ESVPWM are presented in section III. The performance analysis of the simulation results is carried out in section IV. Finally the conclusion of the proposed system and the future scope is presented in section V.

Related Work:

In this section, the literature review of the PWM and Multilevel inverter is discussed. Nowadays PWM become a major part of a power system. In many applications, it is used as a controller of voltage. The PWM Generation- Analogy and Digital Technique are included in the inverter function management (Ranjani, 2014). In order to have efficient AC voltage output the Space Vector Pulse Width Modulation is implemented with three phase bridge Inverter. It regulates less distortion of voltage under condition variation. The modulation circuit is carried out based on carrier triangular. It performs the IGBT switch tuning by the circuit driver. It calculates the time requirement for the process in order to have easy function of inverter (Sameer Pratap Singh, *et al*., 2015; Sandhya Rani, D., A. Appaprao, 2011).

The phase shifted carrier pulse width modulation (PSCPWM) is implemented for minimum distortion of harmonic and to improve the voltage output. In PSCPWM the methodology of phase shifted carrier switching frequency optimal PWM and cascaded multilevel inverters strategy are included to minimize the harmonic distortion. The FPGA is chosen for the implementation of the PSCPWM because of the simple design of hardware and software and fast prototyping (Tamboli, J.I., S.M. Patil, 2014).

The isolated multilevel inverter is connected to the transformer like zig-zag-connected, two-level voltage source inverters) and three phase connection of DC. It provides less stress and efficient, fast access. Moreover, dramatically it reduces the switching frequency and improves waveform (Chung-Ming Young; *et al*., 2011).

The Pulse Width Modulation (PWM) scheme is implemented in the power system for three phases though the balance of multiple carriers. It carried out each group based on the linear feedback shift registers. The random selection of carrier improves the quality of the inverter. By third harmonic injected sine PWM technique the waveform is derived (Muthukumar, P., *et al*., 2014).

The voltage source inverter (VSI) is used in PWM techniques for the quality improvement of waveform and to reduce the harmonic content (Prof, R., Kameswara Rao, *et al*., 2014). In multilevel converter, a harmonic elimination method is developed based on the pattern of pulse in multilevel topologies. However, it manages the elimination process and the control of switching frequency with energy storage (Ilves, K., *et al*., 2011).

Hybrid pulse width modulation technique is used in the power system for the reduction of switching loss. In this modulation soft switched cascaded multilevel inverter is implemented with the source of renewable energy in high power medium voltage applications (RonaldMarian, A., *et al*., 2014).

Multilevel inverter is used for the conversion of high power and voltage. It provides an efficient process with less EMI and high voltage quality. For control circuit generating the digital pulse width modulation (DPWM) signal is proposed with single-phase cascaded H-bridge multilevel inverter. It increases the resolution of the circuit without increasing the unwanted frequency signal (Ahmad, A., R. Gupta, 2013). Fig (Tamboli, J.I., S.M. Patil, 2014) shows the DPWM circuit.

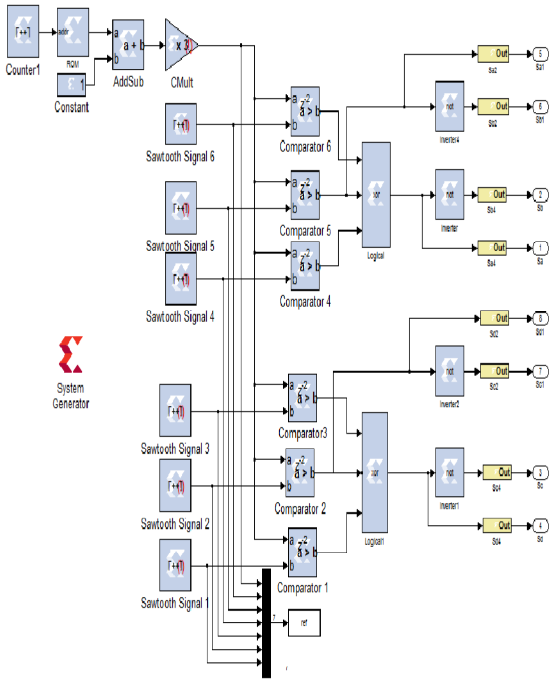

Fig. 2: Existing Circuit - Digital PWM (DPWM)

Improved phase disposition pulse width modulation (PDPWM) is used for the connection of Photovoltaic grid. It is based on the selective virtual loop mapping to balance the voltage without compensation extra signal. The voltage index is processed by the identification of MIN and MAX capacitor. It provides a dynamic process of the control strategy and make easy to grasp FPGA (Mekhilef, S., *et al*., 2013; Jun Mei, Bailu Xiao, *et al*., 2013).

XILINX FPGA based multilevel PWM single-phase inverter is implemented in the power system in bidirectional switching of bridge topology. It performs based on the load variation and provides rapid prototyping efficiency of the device with the inverter switching (Mekhilef, S., A. Masaoud, 2006).

Proposed Work:

In this section, the design and implementation of proposed circuit are explained by its enhancement process. The proposed circuit of Enhanced Space Vector Pulse Width Modulation is designed and developed based on the triangular carrier approach with five level single phase cascaded H-bridge multilevel inverter. Normally the basic generation of the digital PWM signal of the multilevel inverter is performed as shown in Fig (Sameer Pratap Singh, *et al*., 2015). But in the proposed circuit the process is same but the techniques and approach are enhanced for efficiency and better performances in proposed system.

In carrier signals saw tooth waves is used and generated the signal based on the switching condition and by devices of up-counter. In generating signal the counter begins from 0V to 1.0V and for next counter it begins with 1.0V to 2.0V. The differences of each counter are 1.0V. Similarly signal frequency and amplitude is kept constant as 1 KHz. The signal amplitude range is 6.0V and the frequency is 50Hz by using 14 bit ROM and 5 bits up-counter.

In proposing circuit instead of digital PWM, triangular approach of ESVPWM is applied for efficient process and to avoid the burden of the modulation method of existing. By the proposed approach the implementation of the circuit and its efficiency is improved. This approach is executed based on the cyclic duty ratio and its profile is generated by high frequency pulse. The modulation of inverter is implemented in single phase. The signal of modulation is transformed with the constant range of frequency and amplitude. Also, the voltage vector reference is constant in all cyclic process. Fig (Muthukumar, P., *et al*., 2014) shows the proposed circuit system generation.

In zero and active state vector combination the voltage is evaluated and derived the values by the proposed approach equivalence. The mathematical expression of the average voltage pole (V_A, V_B, V_C and VD) is given below:

$$V_A = \frac{V_{DC}}{2}\frac{T_1+T_2+T_6+T_7}{T_S} - \frac{V_{DC}}{2}\frac{T_0}{T_S} = \frac{V_{DC}}{2T_P}\, m_A^* \quad (1)$$

$$V_B = \frac{V_{DC}}{2}\frac{T_2+T_6+T_7}{T_S} - \frac{V_{DC}}{2}\frac{T_0+T_1}{T_S} = \frac{V_{DC}}{2T_P}\, m_B^* \quad (2)$$

$$V_C = \frac{V_{DC}}{2}\frac{T_6+T_7}{T_S} - \frac{V_{DC}}{2}\frac{T_0+T_1+T_2}{T_S} = \frac{V_{DC}}{2T_P}\, m_C^* \quad (3)$$

$$V_D = \frac{V_{DC}}{2}\frac{T_7}{T_S} - \frac{V_{DC}}{2}\frac{T_0+T_1+T_2+T_3}{T_S} = \frac{V_{DC}}{2T_P}\, m_D^* \quad (4)$$

Where, m_A^*, m_B^*, m_C^*, and m_D^* represent the signal modulation and the inverter gain is represented as $\frac{V_{DC}}{2T_P}$ .The intersection point of falling ramp is the switching state waveform in proposed circuit. The voltage vector is not equal to zero and it is expressed as given below:

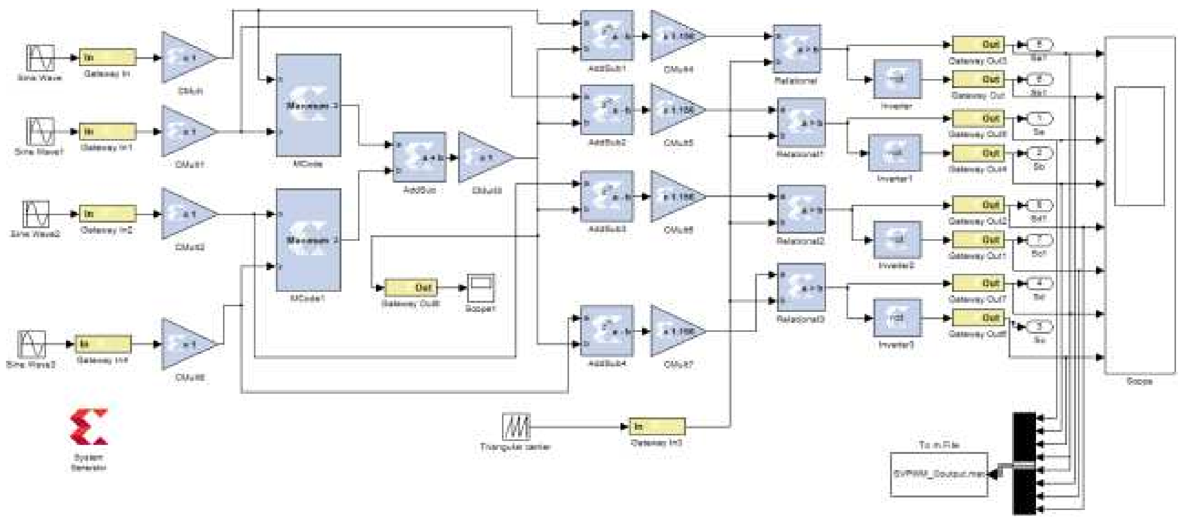

Fig. 3: Proposed Circuit - ESVPWM

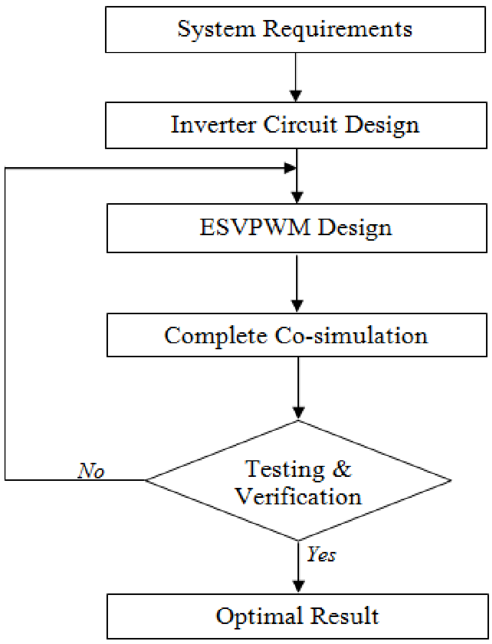

Fig. 4: Proposed Circuit – Flow Work

$$V_A + V_B + V_C + V_D \neq 0 \quad (5)$$

As well as the signal modulation also not equal to zero. In each level of the process the voltage of common mode is included as in equation (RonaldMarian, A., *et al.*, 2014). As shown in Fig (Ranjani, 2014) the proposed approach flow work is carried out and the each stage of the modulating signal is shown in Fig (R., Kameswara Rao, *et al.*, 2014).

$$m_A^* + m_B^* + m_C^* + m_D^* \neq 0 = 4m_{CM} \quad (6)$$

$$m_{CM} = 0.5(m_{MAX} + m_{MIN}) \quad (7)$$

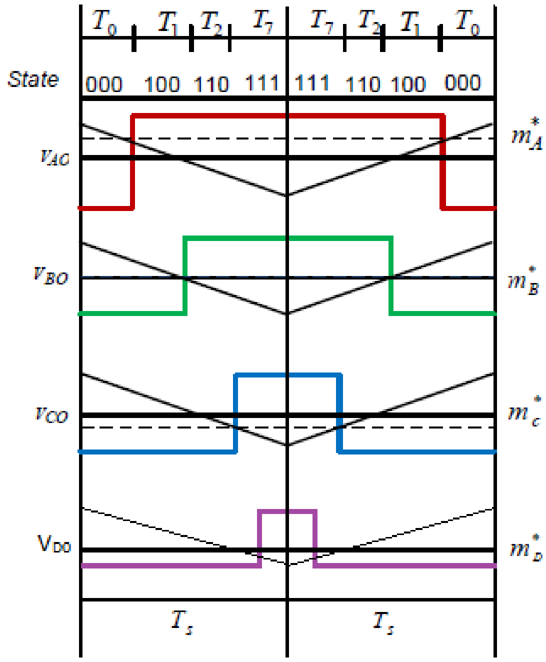

Fig. 5: Modulation signal of each state - ESVPWM

By applying the proposed approach the calculation of each mode voltage value is evaluated. Actually the carrier of the proposed approach will not be equal to zero. The estimation of maximum and minimum is done by the following equations.

$$m^*_{MAX} = m_{MAX} + 0.5(m_{MAX} + m_{MIN}) \quad (8)$$
$$m^*_{MID} = m_{MID} + 0.5(m_{MAX} + m_{MIN}) \quad (9)$$
$$m^*_{MIN} = m_{MIN} + 0.5(m_{MAX} + m_{MIN}) \quad (10)$$
$$m^*_{MAX} + m^*_{MIN} = 0 \quad (11)$$
$$m^*_{MAX} + m^*_{MIN} + 2(0.5(m_{MAX} + m_{MIN})) = 0 \quad (12)$$

The inverter circuit of five levels SPCHMI is shown in Fig [6]. The each level of the inverter in single phase is represented as N=(n-1)/2. In proposed system there is no change in the inverter circuit but PWM is enhanced with the space vector based on triangular approach. Fig [7] shows the inverter circuit of the proposed system. The voltage output of the circuit is equal to the module H-bridge (h) of inverter and defined as given below:

$$V_{ac}=V_{dc/2} + V_{dc/2} + ...+ V_{mh} \quad (13)$$

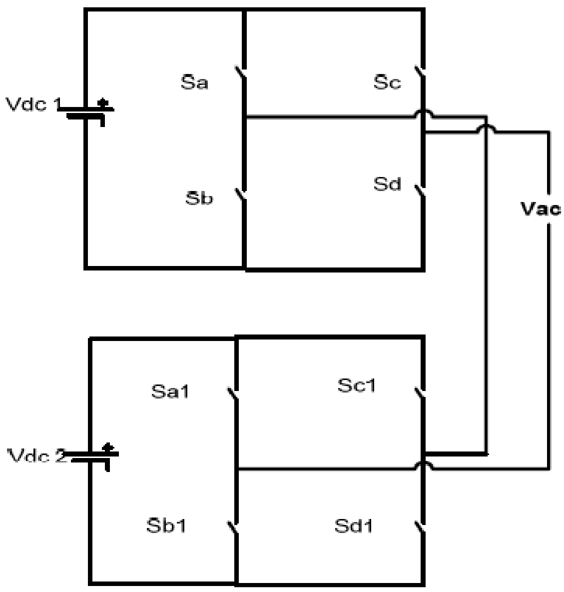

Fig. 6: Five Levels SPCHMI

In inverter circuit, four power switching devices Sa, Sb, Sc, and Sd are considered and the voltage is produced in three levels (+V, 0 and –V). So the connection between the DC sources to AC is become

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possible. It is a simple process and incorporates with the input and output. It provides flexible process and the output of voltage and the signal switching is given in Fig [8].

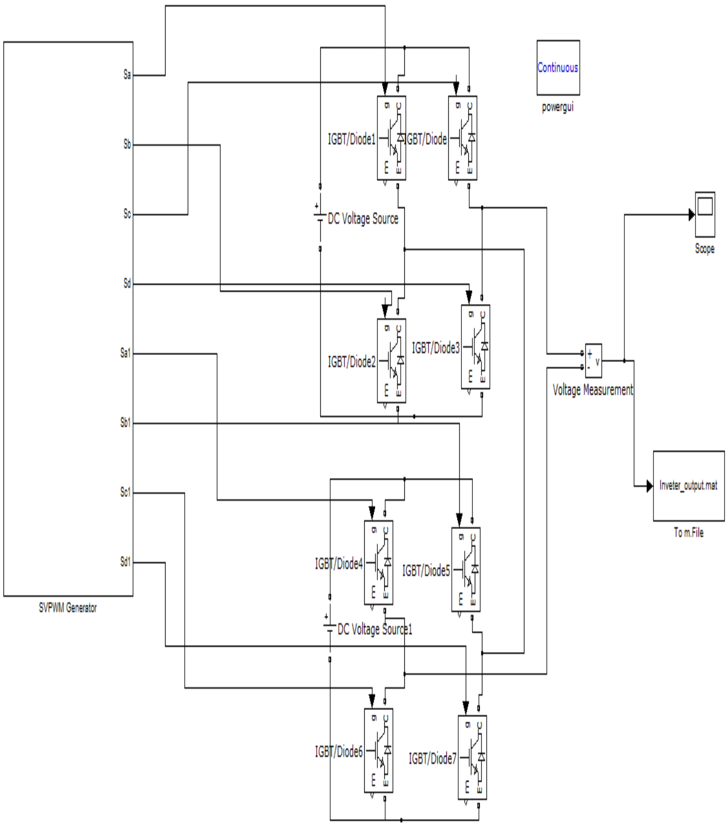

Fig. 7: Proposed Circuit Inverter – SPCHMI

S_{a1}	S_{b1}	S_{c1}	S_{d1}	S_a	S_b	S_c	S_d	V_{ac}
0	1	1	0	1	0	0	1	V_{dc}
0	1	1	0	1	0	1	0	$V_{dc}/2$
0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0	$-V_{dc}/2$
1	0	0	1	0	1	1	0	$-V_{dc}$

Fig. 8: Signals of Gate Switching

Simulation Results:

The performance analysis of the simulation results of proposed ESVPWM is discussed in this section. The five levels of single phase inverter and the proposed circuit is simulated by using MATLAB/Simulink and Xilinx system generator. The proposed system is stimulated and tested to show better performances of the circuit in a flexible process.

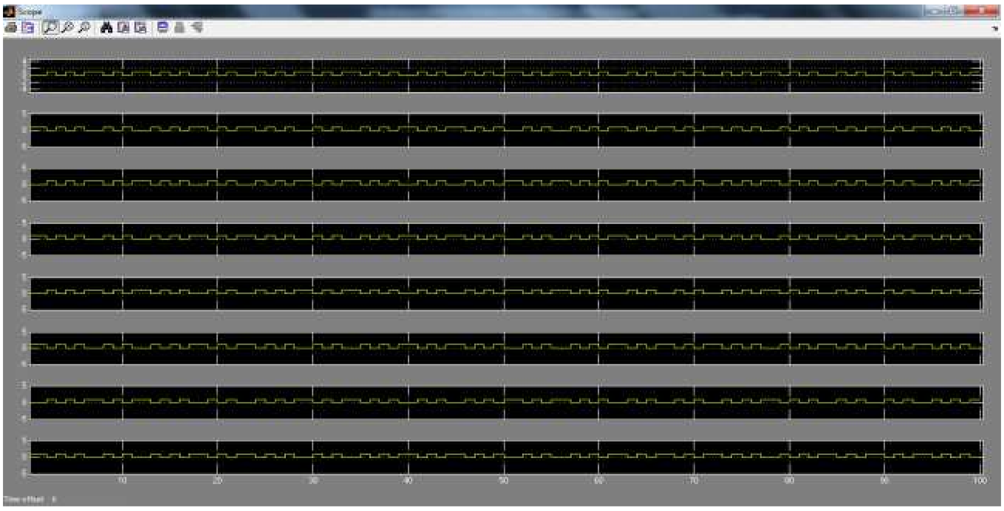

Fig. 9: Simulation results of ESVPWM Circuit

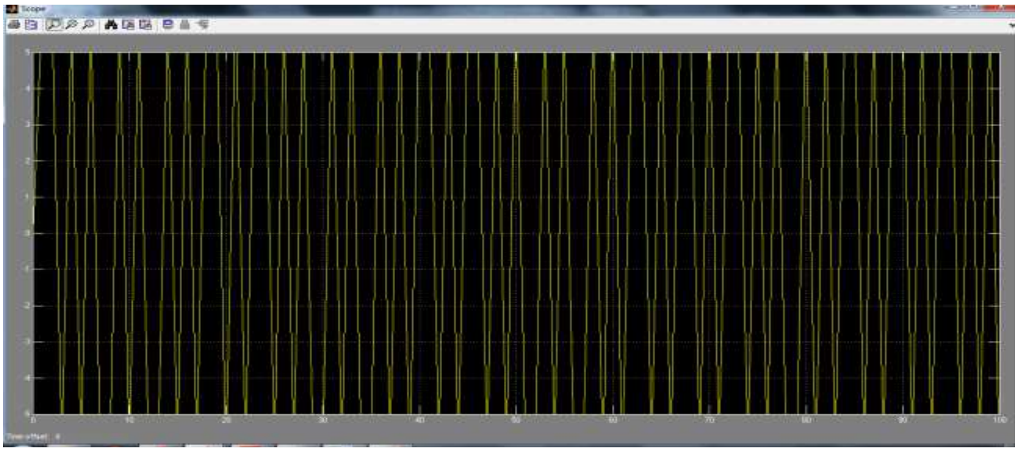

Fig. 10: Simulation result of SPCHMI

The simulation of the system is carried out with the proposed approach. The results of the PWM and the inverter are evaluated and provide improvement in the proposed circuit. Fig [9] shows the proposed circuit simulation result and Fig [10] shows the results of inverter levels (SPCHMI) with ESVPWM. Both results are simulated using a Simulink system generator. The MATLAB simulation results of the ESVPWM and SPCHMI between the voltage data and time are shown in Fig [11] and Fig [12].

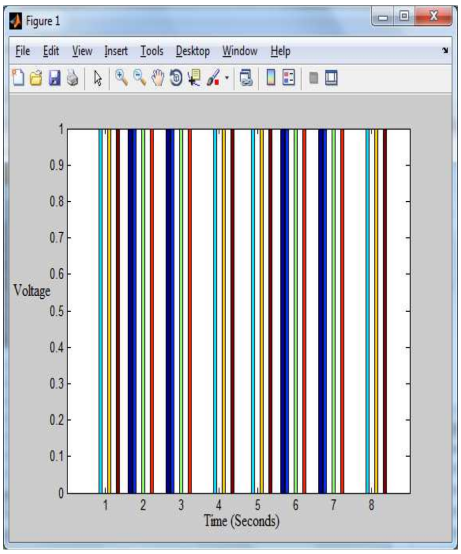

Fig. 11: MATLAB Simulation result of ESVPWM

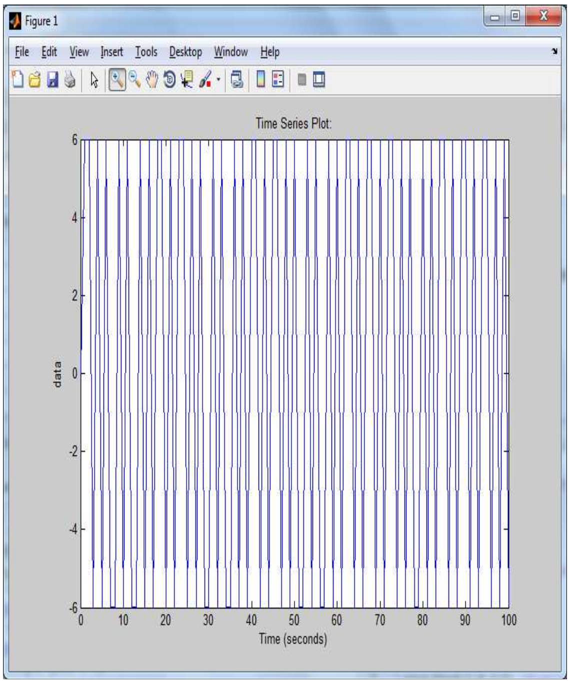

Fig. 12: MATLAB Simulation result of SPCHMI

Conclusion and Future Work:

In this paper, a design of ESVPWM based on triangular approach is proposed with five levels SPCHMI and the implementation of control strategy is performed. It performs the operation as per the switching signals and gives better voltage output. The control signal of the proposed system is managed and gives improvement in performances with flexible access. The inverter controller performs most effective and economical. The proposed circuit provides improvement in complexity reduction, less voltage stress, highly efficient and flexible access.

The future scope is to design an improved inverter controller strategy and to improve the quality of inverter output voltage waveform shape.

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