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Design and Analysis of Improved Sparse Channel Adder with Optimization of Energy Delay

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ABSTRACT

Normally the power density and dissipation are the main objective and rapid growth in portable systems. In VLSI design, the widely used adder component provides better performances in the integrated circuit. The analysis and design of Carry Select adder (CSLA) is proposed with Modified AOI in a cadence 45nm CMOS. It reduces the delay process with efficient access of better performances. It processes in parallel prefix with sum and carry generating for the high and fast process of circuit. The modified CSLA circuit observed less power consumption and area than the existing circuit with less gate count. By the proposed circuit the gate-level are performed in a simple and easy manner. Based on modification of CSLA bits the process of the circuit is performed in an efficient manner in terms of gate count, power and delay.

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INTRODUCTION

In VLSI industry, the design area and power consumption circuit are rapidly increasing the necessary for high-speed systems. In digital circuits, according to the limits of adder speed the propagation of the carry is performed as per the requirement of time. The generating of carry function is performed sequentially as per the carry propagates each bit one after the next. With the indices of a table the address is evaluated.

Multiplier-Accumulator (MAC) unit is a DSP processor and the whole system is performed significantly. Hence the adder circuit is essential to implement with the reduction of delay propagation, low power and high speed process of the circuit. Basically, in parallel computation based on multiplexers (MUX) the sum and carry function is performed. Various algorithms such as FFT, FIR and IIR are accessed in the integrated circuit of digital signal processing adder for high speed performances.

In recent digital circuit, the reduction of consumption in a similar speed is process as per the requirement of the data path. In Arithmetic and logic unit (ALU) and digital signal processing (DSP) systems widely used the adder hardware blocks. The computational system of CSLA is used to generate the multiple query function after the sum function. Carry Select Adder (CSLA) is a faster function of arithmetic in DSP. However, the selection process of RCA multiple pairs is performed by using MUX.

Ripple Carry Adder (RCA) is implemented for deriving fast process performances of circuit with less consumption of the area, but it required high computation time to perform in a compact design. Binary to Excess-1 Converter (BEC) [10] is used instead of RCA to achieve consumption reduction in power and area. Both the adders are used for the same purposes, but the performance of BEC is improved than the existing. The general 4-bit circuit of various adders with 8:4 MUX is shown in Fig [1].

The basic requirement of complex adder like Carry look--Ahead Adder, RCA, Carry Select Adder and BEC are designed with fast process and time computation time for some critical applications. It leads to have a less area consumption with the delay process as per the adder circuit. As well as AOI is implemented in the circuit design instead of the BEC or RCA to have less consumption and to reduce the gate count. The circuit design code is based on the gate.

In this paper, the various adders' comparisons are analyzed and design a SQRT-CSLA circuit with the performance improvement than the existing circuit. The proposed circuit is modified the AOI and implemented to have low power consumption and delay. The proposed circuit is modified by placing the Modified AOI in the place of other adders.

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The rest of the paper is organized in sections wise; in section II the related review of CSLA and various adder circuits for less consumption and efficient process of the circuit are discussed. The methodology of the circuit is explained in section III. The proposed design circuit flow work is explained in Section IV and in section V the implementation of the proposed circuit SQRT – CSLA is presented. In Section VI the performance analysis of simulation results is discussed. Finally the conclusion of the proposed circuit and the future work is in Section VII.

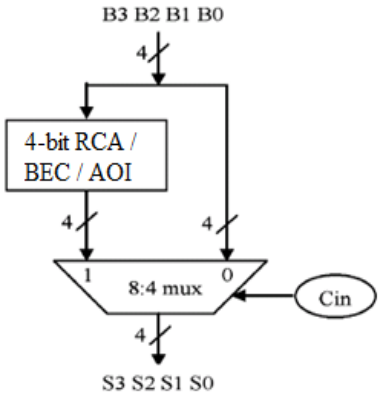

Fig. 1: 4-bit Adder circuit with 8:4 MUX.

Literature Survey:

In this section, the logic adder circuit process related survey is discussed with various types of adder. In The energy efficiency is essential for the execution cores in the arithmetic unit. In adder the power density is a part of the processor block and creates a sharp temperature gradients and thermal hot spots for high performances of system operation. In modern superscalar processors, multiple ALUs are occurring and the circuit reliability impact is associated with the chip execution cores. For the design purposes the cost of cooling is increased.

As well as, the significant process of adder under various region, FPUs data path and appearances of the ALU is performed. Ripple Carry Adder have a flow of carry for the next adder from "N" single bit and the output is passed as input next adder. Therefore, the data path worst case delay passes the path through the N stage. It is a linear process of increasing the value of adder delay. So the propagation delay of the adder consists with low speed, but in BEC the structure is designed using less logic gates than the RCA N-bit full adder.

Binary to Excess- 1 converter (BEC) with conventional CSLA (Cin=1) is placed instead of RCA in order to have low power an area. In BEC N+1 bit is used but in RCA N bits is used for the process. Therefore the Modified CSLA is balancing the delay and other parameters than the RCA. In RCA it process with dual RCA but in modified circuit single RCA and BEC is used. Fig [2] shows the BEC function table and Fig [3] shows the modified circuit of BEC instead of RCA.

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

Fig. 2: Function Table of BEC.

Ripple carry adders exhibits compact design with slow speed, but carry look ahead provide a faster process with the consume of more area. As well as it acts as a negotiation between adder. In 2002, a hybrid carry look-ahead/carry select adder is developed for speed process and less power multipliers. By analyzing the circuit using VLSI with 32-Bit Multiplier shows improvement of speed than the RCA is almost double.

For consumption reduction of circuit BEC is used. For the improvement of the performances D latch is used for enabling the signals. In RCA, N delay linear proportional is processed so the adder performed highest delay process. Normally it

provides more delay by the fan-in and the logic gates.

The carry select adder (CSL) design exhibits the structure with gate depth and dual ripple-carry adder (RCA) implementation. It performs in space-time tug-of-war and optimizes the constraints in VLSI design. It reduces the gate level and provide better performs in the consumption of power, area and delay.

The issues of Regular CSLA, modified CSLA, modified CSLA using BEC, AOI, D-Latch and Carry look ahead adder is simulated with the proposed design system to give better performance than the others. The proposed architecture evaluated in terms of area, delay and power. Also, the gate level is performed according to the requirement of the system. The analysis of the results shows the improvement of performances in speed and consumption. Also, it makes VLSI hardware implementation simple and efficient way.

Methodology:

In this section, the explanation of methodology function performs to have less power, delay and area. The adder blocks perform with low consumption and evaluate it by using the theoretical approach which shows the implementation process effects with area and power. Fig [4] shows the XOR gate implementation in AND, OR, and Inverter (AOI). The consuming of the gate generating level and the evaluation of methodology considered the consumption by having 1 unit for each for maximum delay.

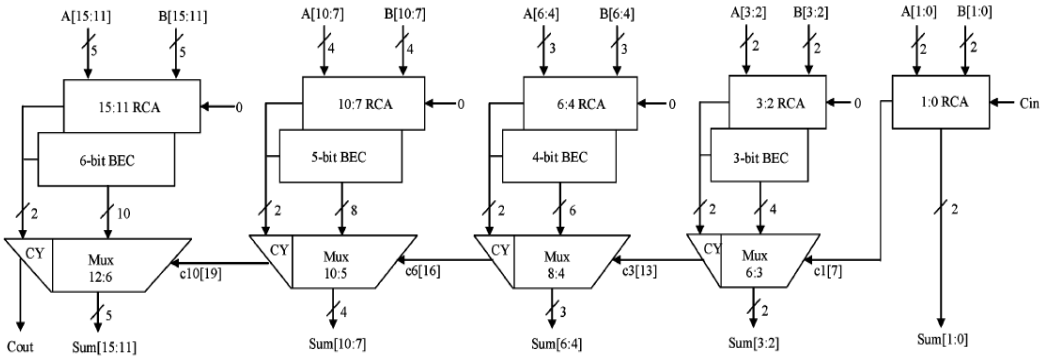

Fig. 3: Modified 16-b SQRT CSLA.

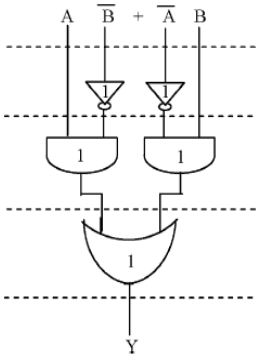

Fig. 4: Evaluation of XOR gate.

The performance of gate operations is done in parallel and indicates the delay for each gates representation. The evaluation of methodology is considered with a maximum delay by the logical block of the gate. By the counting of AOI gates of each block the area evaluation is considered. For better performances of speed and consumption reduction RCA and BEC is replaced with AOI when Cin=1. In modified design the performances are evaluated by using gate counts than the structure of n-bit Full Adder. For simple and efficient manner the existing system is modified. Fig [5] shows the replacement of AOI.

In this paper, the modified circuit is again modified the AND gate with MUX in order to show better performance in consumption than the existing circuit. The replacement of modified adder in the circuit is considered when Cin =1.

Architecture of Modified 64-Bit SQRT CSLA:

In this section, the proposed design architecture of 64-bit SQRT CSLA is explained. The existing system modification is shown in Fig [5] with Cin=1. The replacement of AOI is grouped the function of adder in block wise and illustrates the evaluation results of grouped circuit.

In proposed work, Modified AOI (M-AOI) is performed as same as the operation of other adders but the gate of AND is replaced with MUX in the proposed circuit. For logic function one bit is higher as per the bits requirement. The input is split into various groups with the AOI function, MUX and RCA.

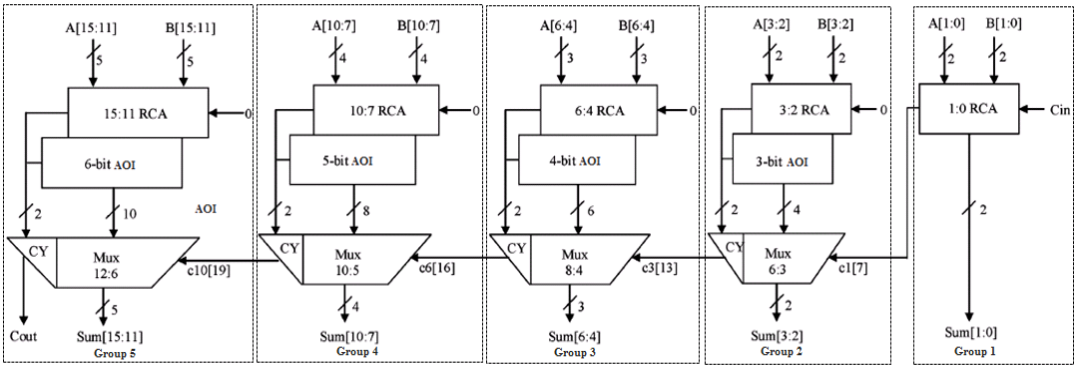

Fig. 5: Modified 16-b SQRT CSLA. The parallel function replace of BEC when Cin =1 with AOI.

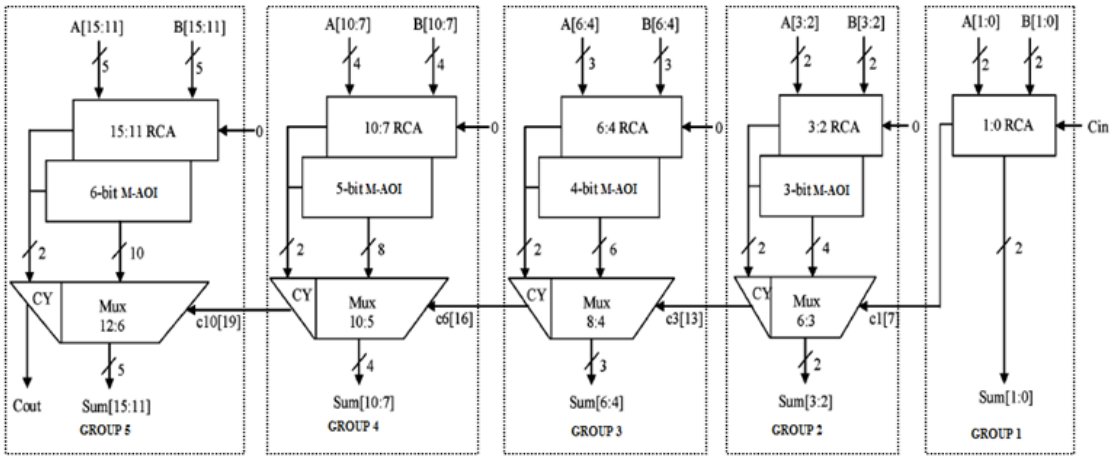

Fig. 6: Modified 16-bit SQRT CSLA. The parallel process circuit with replacement of existing adder when Cin =1 with Modified-AOI.

The significant system process is carried out the sum and carries function. The significant bit of Group 1 have lower bit and the output is given as input to the next stage of Group 2 in the circuit as shown in Fig [6]. In AOI adder, the gate function is modified by the replacement of MUX instead of AND gate and the modified function is implemented in the proposed system.

In group 1, only RCA adder is used but in other groups RCA and Modified AOI are used. As similar to group 1 the process function is done with both the adder but here the input is taken from the previous output. The logic modified AOI is replaced in the position of RCA, BEC and AOI when Cin=1. The input selection is considered by the timely arrival and delay. The pervious sum of RCA and AOI is given as input to the next group and the MUX output is computed respectively with the adder. The multiplexer design implementation is coded from 6:3 to 24:11. By using gates the design code is performed on the circuit. The evaluation of the proposed method is implemented in the modified area efficient of 16-bit SQRT CSLA.

The proposed circuit is optimized the each level of the group and evaluated the parameters as shown in Fig [7]. In group 2, one half and full adder (2-bit RCA) is considered with Cin=0. If Cin=1 then 3bit AOI is used and includes one output. The gate count is obtained for group 2 as follows:

Gate count = Sum (FA, HA, MUX, AOI)

Group 2: FA=11(11*1); HA=5(5*1); NOT=3; AND=4; OR=2; MUX=12(3*4).

Implementation:

In this section, the circuit design flow and implementation of kit design is explanation and the design is done using Cadence 45nm CMOS process technology. The common Boolean logical terms are shared with the operation of modified AOI gates. The logic gates determine the perform time of the structure with the present input in the combinational circuit. As well as the signal state of logic selection is

done through the multiplexer. Therefore, the proposed design performed with less delay, area and power than the existing.

The group structure of the proposed circuit is designed and implemented for the performance improvement of the system. The modifications of the proposed circuit consider the gate replacement. As per the design logic, the hierarchical process proceeds with the specification of logic circuit and also the complete circuit determine the functions by the Carry look ahead network, pre and post processing. Fig [7] shows the existing structure of AOI with and without the signal and Fig [8] shows the modified AOI Circuit. The proposed M-AOI circuit is implemented in the groups. Fig [9] shows the modified adder of CSLA (MA-CSLA) with all groups. The proposed structure of group 1 to 5 is shown in Fig [10a] to Fig [10e] respectively.

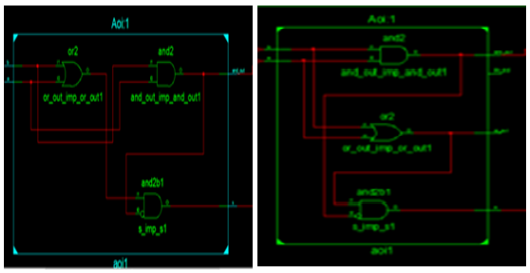

Fig. 7: Schematic Diagram – Existing AOI with and without Signal.

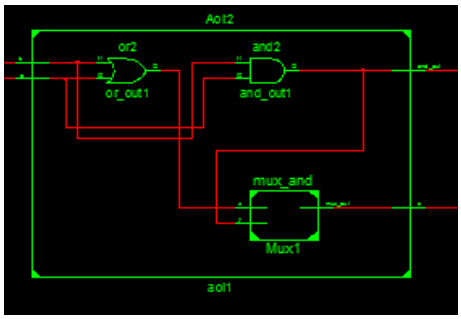

Fig. 8: Schematic Diagram – Proposed Circuit of Modified AOI.

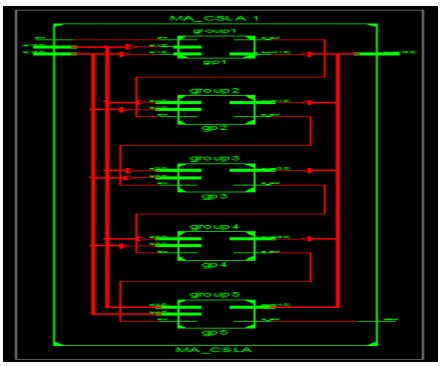

Fig. 9: Schematic Diagram - Proposed Circuit with all groups.

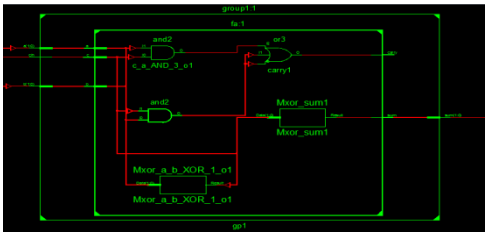

Fig. 10a: Schematic Diagram - Proposed Circuit of Group 1.

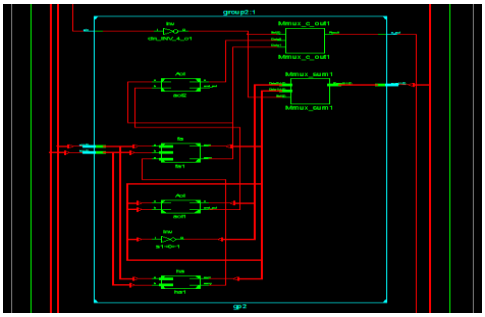

Fig.10b: Schematic Diagram - Proposed Circuit of Group 2.

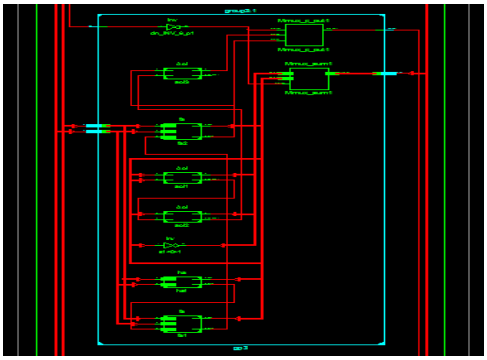

Fig.10c: Schematic Diagram - Proposed Circuit of Group 3.

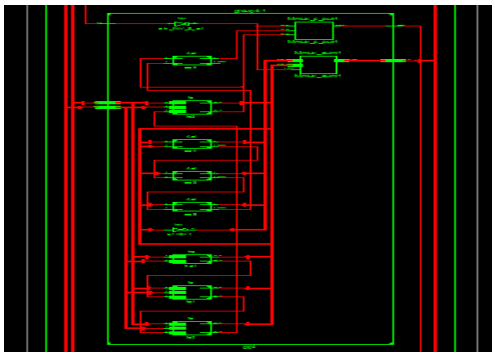

Fig. 10d: Schematic Diagram - Proposed Circuit of Group 4.

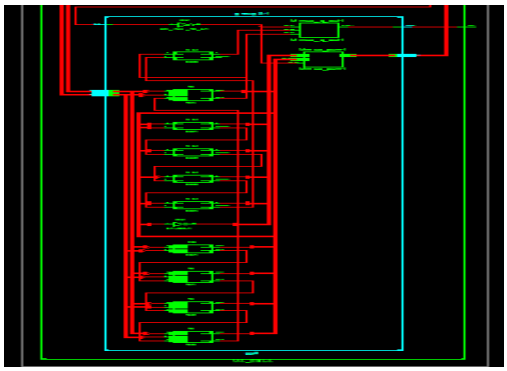

Fig. 10e: Schematic Diagram - Proposed Circuit of Group 5.

Simulation Results:

The analysis of proposed circuit simulation results is explained and illustrated in this section. The simulation process specification are Power (460 uW), Max frequency (374.94 MHz) and Area (440 µm X 300 µm = 0.132 mm^2). The common inputs of CMOS for the process are randomly generated by the CMOS inverter. The layout of the proposed design

circuit is done using Cadence Virtuoso Layout Editor Tool. The layout of all groups implementation is shown in Fig [11] and the proposed methodology function is performed successfully. The proposed structure schematic diagram is shown in Fig [12]. The RTL diagram of the proposed circuit of adder is simulated and analysis as shown in Fig [13].

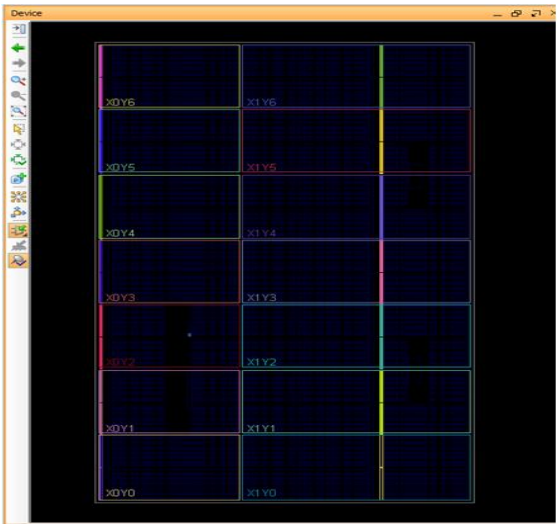

Fig. 11: Schematic Diagram - Proposed Circuit Layout.

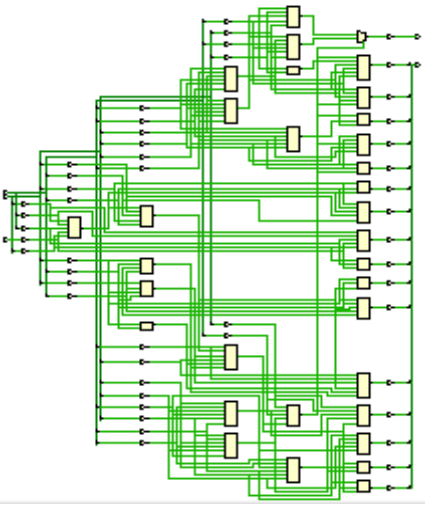

Fig. 12: Schematic Diagram - Proposed Circuit.

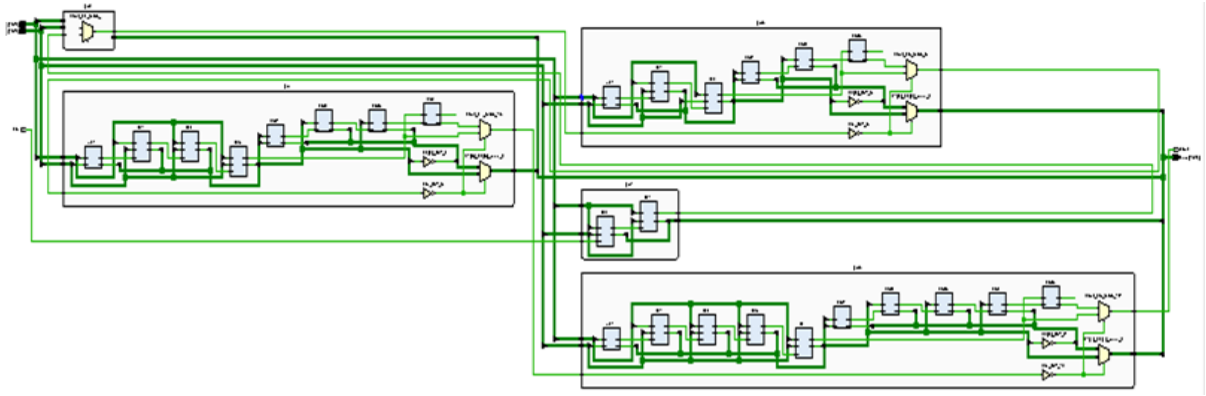

Fig. 13: RTL Schematic Diagram of Proposed Circuit.

Table 1: Performances analysis of various adder circuits.

Adder (Word Size 8 Bit)	Area (gate count)	Delay (ns)	Power (mW)	Power Delay Product (pWs)
Conventional (Dual RCA)	198	14.62	95.60	1366.36
Modified conventional (with BEC)	154	16.52	85.32	1445.47
Modified Conventional (with AOI)	148	15.56	82.65	1286.034
Modified Conventional (with M-AOI)	112	13.89	80.95	1124.40
Regular SQRT (Dual RCA)	132	10.98	182	2300.56
Modified SQRT (with BEC)	128	12.25	175	2464.2
Modified SQRT(with AOI)	120	11.91	169	2012.79
Modified SQRT(with M-AOI)	105	10.82	151	1633.82

Table [1] shows the performance analysis of proposed circuit and various adder circuits. It proposed circuit provides better performances in power delay product, gate count, power and delay than the existing. Fig [12] shows the simulation results of the proposed modified AOI circuit with MUX and the overall proposed circuit simulation result is shown in Fig [13]. Fig [14] and Fig [15] shows the performances analysis of area and power for various circuit.

Conclusion:

In VLSI design, the essential factors of any circuit are area, delay and power for analysis of performances. In this paper, the proposed circuit is designed in order to overcome the issues and limits of the various existing circuits. The Modified 16-bit SQRT CSLA is proposed for the improvement of performances in gate count reduction, less delay and lower power than the existing. Also provides faster process and provide implementation in a simple and easy manner. In VLSI, the proposed hardware implementation is performed in an efficient access by simulating the circuit using the library function of gpdk in a Cadence 45nm CMOS process. The analysis of proposed modified SQRT CSLA shows the improvement by providing less consumption of power and delay. Future thinks to test the proposed design by increasing the bits (128 bits) and to improve the performances of parameter level.

Fig. 13: Simulation results of M-AOI with MUX.

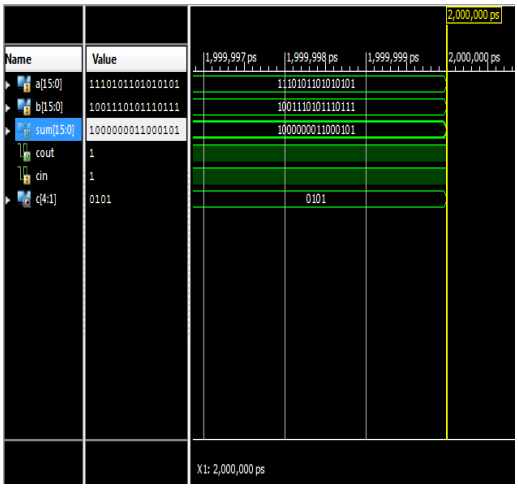

Fig. 14: Proposed circuit Simulation results.

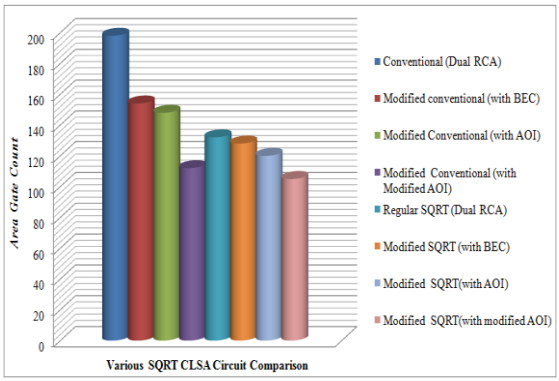

Fig.15: Performances analysis of Area (gate count).

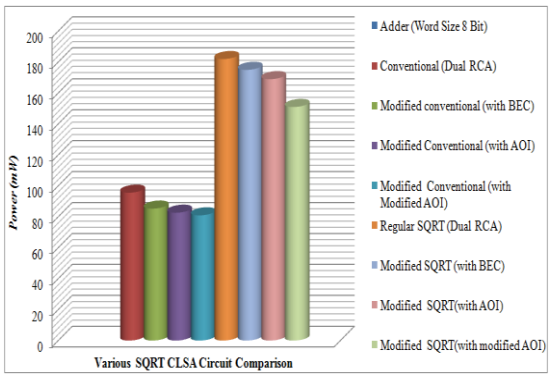

Fig. 16: Performances analysis of Power.

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