



AENSI Journals

Australian Journal of Basic and Applied Sciences

ISSN:1991-8178

Journal home page: www.ajbasweb.com



Design of Low Power FIR Filter Using 6T Full Adder

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ARTICLE INFO

Article history:

Received 19 August 2014

Received in revised form

19 September 2014

Accepted 29 September 2014

Available online 12 November 2014

Keywords:

FIR Filter, CMOS transistor, low

Power VLSI

ABSTRACT

Background: Today the designers make their effort to reduce the power consumption in digital signal processing systems, portable systems and cellular networks. Low power dissipation will allow the system to operate for a longer life efficiently. **Objective:** Low-power techniques are necessary for the design of DSP-based systems. Finite Impulse Response (FIR) filter plays a vital role in almost all DSP-based applications. The reduction of power consumption of FIR filter will lead to overall power reduction of the system. The 6-transistor full adder is designed using 2 transistor XOR gate for low power combinational circuit design. This technique allows the reduction in power consumption and area of digital circuits, maintaining low complexity of the design. In the FIR filter, ripple carry adders and array multipliers are designed using 6 transistor (6T) full adder. **Results:** The FIR filter consumes only 17.5mW power which is 31% less than conventional FIR filter. FIR filter structure is designed and simulated using HSPICE in 90nm technology with a supply voltage of 1.2 V. **Conclusion:** The reduced power usage in the proposed adder with its sub-blocks like Ripple Carry adder, hybrid array multiplier leads to overall power reduction of FIR filter.

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To Cite This Article: M. Madheswaran and D. Malathi, Design of low power FIR filter using 6T Full adder. *Aust. J. Basic & Appl. Sci.*, 8(18): 72-78, 2014

INTRODUCTION

Digital signal processing (DSP) is used in wide range of applications such as telephone, radio, video etc. Most of DSP computations involve the use of multiply accumulate operations and therefore the design of fast and efficient multiplier is imperative. FIR filters are widely used in digital signal processing (DSP) systems that are characterized by the extensive sequence of multiplication operations. Finite Impulse Response (FIR) filters are digital filters whose response to a unit impulse (unit sample function) is finite in duration. This is in contrast to infinite impulse response (IIR) filters whose response to a unit impulse (unit sample function) is infinite in duration. FIR and IIR filters each have advantages and disadvantages, and neither is best in all situations. FIR filters can be implemented using either recursive or nonrecursive techniques, but usually nonrecursive techniques are used. In some applications, the FIR filter circuit must be able to operate at high sample rates, while in other applications, the FIR filter circuit must be a low-power circuit operating at moderate sample rates. Parallel (or block) processing can be applied to digital FIR filters to either increase the effective throughput or reduce the power consumption of the original filter.

Traditionally, the application of parallel processing to an FIR filter involves the replication of the hardware units that exist in the original filter. The topology of the multiplier circuit also affects the resultant power consumption. Choosing multipliers with more hardware breadth rather than depth would not only reduce the delay, but also the total power consumption. A lot of design methods of low power digital FIR filter are proposed, FIR filters were implemented using registered address and hardwired shifts. Modified common sub expression elimination algorithm is used to reduce the number of adders. A novel approach for low power FIR filter using digital baseband processing was proposed. The filter coefficients are represented by optimized bit width. A new reconfigurable architecture for implementing FIR filters with low complexity was capable of operating for different word length filter coefficients without any overhead in the hardware circuitry. An architectural approach to the design of low power reconfigurable finite impulse response filter is well suited when the filter order is fixed and not changed for particular applications.

Low power circuit design has been a challenge for a long time and it is now one of the most important goals of today's CMOS designs. Signal processing is one of the most power hungry applications. Adders are the main

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building blocks for signal processing applications. Saving power in adders would reduce the power consumption significantly at the chip level. Low power can be achieved at four different levels of the design process, the architectural, the circuit, the device or the layout levels. Power consumption in CMOS digital circuits is divided into three major components as follows:

$$P_{\text{tot}} = P_{\text{dynamic}}(P_d) + P_{\text{static}} + P_{\text{short circuit}} \quad (1)$$

Recently, building low-power VLSI systems are highly in demand because of the fast growing technologies in mobile communication and computation. The battery technology doesn't advance at the same rate as the microelectronics technology. There is a limited amount of power available for the mobile systems. So designers face more constraints in designing with high speed, high throughput, small silicon area, and at the same time low-power consumption. So building low-power, high-performance adder cells is of great interest. Designing systems aiming for low power is not a straight forward task, as it is involved in all the IC design stages, beginning with the system behavioral description and ending with the fabrication and packaging processes. In some of these stages there are guidelines and steps to reduce power consumption, such as decreasing the power-supply voltage. While in other stages there are no clear steps to follow, so statistical or probabilistic heuristic methods are used to estimate the power consumption of a given design.

The dynamic component is the part of power consumption, when the circuit is switching from one state to another. To estimate the worst case or max power consumption, the circuit has to be matched through all of its states. Added to this is the power used to charge and discharge the load capacitance. The load capacitance is identical for all cells and simulations performed in this paper, so it will not play a role in the relative comparison of the power consumption. Actual layout will affect the load capacitance which constitutes the routing capacitance and the fanout capacitance. Layout effects and their minimizations are not considered here. The less and less is the characteristic dimension of a technology, the routing load factor starts to dominate the total loading on gates. This is very noticeable in submicron technologies and low fanout designs. The static component is due to the reverse bias leakage between diffusion regions and the substrate. In conventional CMOS there is no direct path from VDD and GND at steady stable static state so there is no DC current path, hence power consumption is zero.

The short circuit component is due to the direct path from VDD to GND during switching of the gate. The slower the rise and fall times the bigger the current spike and consequently the power dissipated. Since the outputs of some adders are not fully driven rail to rail, short circuit power dissipation occur in the next stage of a bigger design. Hence, loads had to be included in the simulation—two minimum sized buffer inverters—to the sum and carry out account for the power dissipated in the total design. It would be an unfair to find power consumption comparison without these loads. The second issue in the simulation is that the inputs are driven from two minimum sized inverters for each input. This results in a finite output impedance of the input signal driver, which account to the loading of the input impedance of the different inputs of different adder circuits.

The basic dynamic power consumption of a conventional CMOS digital circuit is given by:

$$P_d = \alpha * f * V_{dd}^2 * C_{load} \quad (2)$$

α : is the activity factor which represents the switching activity of the cell on a probabilistic/statistical basis. This is the same for all simulations for all circuits so it is a don't care for relative power consumption analysis.

f : frequency switching of the input signals. This is considered as the max frequency of the inputs.

V_{dd} is the positive supply voltage.

C_{load} : is the load on the output node. This is the same for all circuits.

At the device level, reducing the positive supply voltage V_{dd} and reducing the threshold voltage accordingly would reduce the power consumption significantly. At the layout level, some tricks can be used including the use of short smaller transistors, poly and diffusion areas and the use of shorter metal lines for connections of different devices. These mainly reduce the loading i.e. parasitic capacitances in different parts of the device and circuit.

Design of Fir Filter:

Digital filters are typically used to modify or alter the attributes of a signal in the time or frequency domain. The most common digital filter is the Linear Time-Invariant (LTI) filter. An LTI interacts with its input signal through a process called linear convolution, denoted by $y = h * x$ where h is the filter's impulse response, x is the input signal, and y is the convolved output. The linear convolution process is formally defined by:

$$y[n] = x[n]h[n] = \sum_{k=0} x[n]h[n - k] \quad (3)$$

An FIR with constant coefficients is an LTI digital filter. The output of an FIR of order or length L , to an input time-series $x[n]$, is given by a *finite* version of the convolution sum given in (1),

$$y[n] = \sum_{k=0}^{L-1} h[k]x[n-k] \quad (4)$$

where $h[0] \neq 0$ through $h[L-1] \neq 0$ are the filter's L coefficients.[4]

Fig.1 shows the basic block diagram for an FIR filter of length N . The delays result in operating on prior input samples. The $h[k]$ values are the coefficients used for multiplication, so that the output at time n is the summation of all the delayed samples multiplied by the appropriate coefficients.

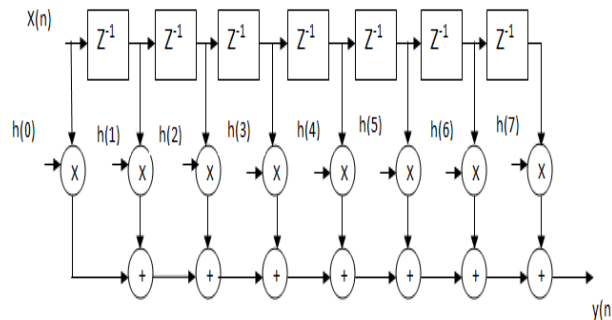


Fig. 1: Direct form 8-tap FIR filter.

XOR Gate:

The XOR gate is the basic building block of full adder circuit. It is used in generating the sum output of full adder circuit. The size of the full adder circuit mainly depends on the number of transistors t utilized to perform the required logic. Reducing the transistor count may reduce the physical area required by the full adder for the same logic. If the XOR gate can be realized with less number of transistors then it may be possible to reduce the number of transistors in realizing the full adder thereby reducing the size of the overall chip. The main intention of reducing this transistor count is to reduce the size of XOR gate so that large number of devices can be configured on a single silicon chip thereby reducing the area and delay.

In the present work a high speed XOR gate has been proposed. In the proposed logic the XOR gate can be realized with the help of two pMOS transistors. The circuit diagram for 2 transistor XOR gate is shown in Fig.2

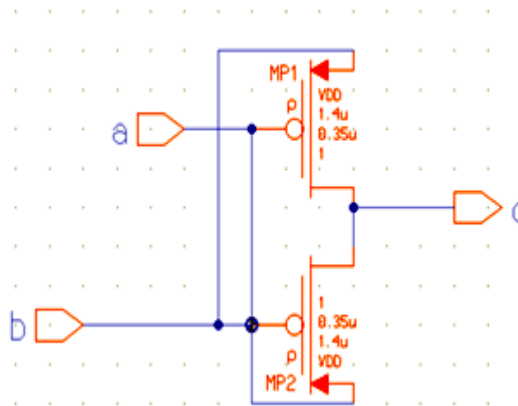


Fig. 2: Design of Two Transistor XOR Gate.

When $A=B=0$, both the transistors MP1 and MP2 are in ON state and the output is logic low output. When $A=0$ and $B=1$, then the transistor MP1 is in OFF state and the transistor MP2 is in ON state which results in logic high output. When $A=1$ and $B=0$, the transistor MP1 is in ON state and the transistor MP2 is in OFF state which results in logic high output. When $A=B=1$, both the transistors MP1 and MP2 are in OFF state results in logic low output.

The size of the full adder can be reduced to a great extent as it requires less number of transistors. If the size of the device decreases then it is possible to integrate large number of devices on a single silicon chip. The 2 transistor XOR gate also minimizes the delay and the power to be dissipated to a great extent. Compared to the existing 3 transistor XOR gate the proposed 2 transistor XOR gate is advantageous because the 2

transistor XOR gate requires less number of transistors compared to the 3 transistor XOR gate for the same logical operation. The delay associated with the sum output of the 2 transistor XOR gate is also less than the delay associated with the sum output of 3 transistor XOR gate. With these advantages the proposed XOR gate may be used in many of the consumer electronic goods and portable electronic devices where less power and delay is the primary requirement.

Full Adder:

The full adder is designed with a minimum of 6 transistors using 2 transistor XOR gate is a modified version of the existing 8 transistor full adder. It uses both the pMOS and nMOS transistors in its hardware circuitry. The 2 transistor XOR gate plays a dominant role in minimizing the transistor count from 8 to 6. In addition to XOR gate the proposed full adder also uses one XNOR gate which can be obtained by modifying the basic equations of sum and carry of a full adder. It plays an important role in minimizing the transistor count. The main advantages of the proposed 6 transistor full adder circuit are small size and less power dissipation compared to the previously designed full adder circuits and the speed of operation is also high. The proposed full adder also reduces the two stage delay associated with the sum and carry elements of eight transistor full adder circuit. The 6 transistor full adder is shown in Fig.3.

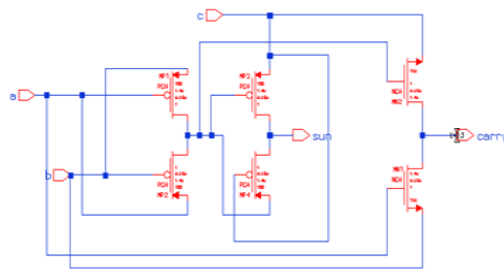


Fig. 3: 6T Full Adder.

Ripple Carry Adder:

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N-bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delay inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. The carry propagation delay is the time elapsed between the application of the carry in signal and the occurrence of the carry out (C_{out}) signal.

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a C_{in} , which is the C_{out} of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder. The 8 bit Ripple Carry Adder is shown in Fig. 4.

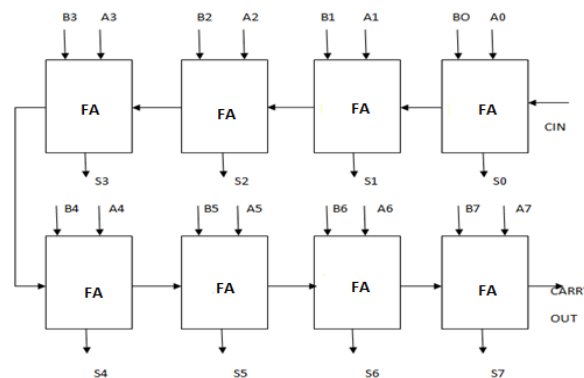


Fig. 4: Ripple Carry Adder.

The layout of a ripple-carry adder is simple, which allows for fast design time; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full

adder. The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic. In a 32-bit ripple-carry adder, there are 32 full adders, so the critical path (worst case) delay is 2 (from input to carry in first adder) + 31 * 2 (for carry propagation in later adders) = 64 gate delays. A design with alternating carry polarities and optimized AND-OR-Invert (AOI) gates can be about twice as fast. Thus, the sum of the most significant bit is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage. As a result, the final sum and carry bits will be valid after a considerable delay. The speed of ripple carry addition operation is very slow when many bits are to be added. In fact, the carry chain propagation delay is the determining factor in most microprocessor speeds.

A 8-Bit Ripple Carry Adder can be constructed using 8 full adder circuits connected in parallel. The carry output of each adder is connected to the carry input of the next higher-order adder. The least significant position, carry input of the first full-adder is made zero. A single full adder is capable of adding two one-bit numbers and an input carry. In order to add a binary numbers with more than one bit, additional full adder can be employed.

Array Multiplier:

Multiplication is one of the most frequently encountered arithmetic operations in floating point processors and digital signal processing applications such as digital filtering, DCT, FFT, CDMA and many others. The logic diagram of 8*8 array multiplier is shown in the Fig.5. The basic building block of array multiplier are Full Adder (FA), Half Adder (HA) and AND gates. The total numbers of FA required is 48, the HA required is 8 and the AND gate required is 64.

Array multiplier is well known due to its regular structure. Multiplier circuit is based on add and shift algorithm. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product are shifted according to their bit orders and then added. The addition can be performed with normal carry propagate adder. N-1 adders are required where N is the multiplier length. Final product is obtained in a final adder by any fast adder (usually carry ripple adder). In array multiplication we need to add, as many partial products as there are multiplier bits. When 2's complement partial products are added in carry save arithmetic all numbers to be added in one adder stage have to be of equal bit length. Therefore, the sign bits of the partial product(s) in the first row and the sum and carry signals of each adder row are extended up to the most significant sign bit of the number with the largest absolute value to be added in this stage. The sign bit extension results in a higher capacitive load (fan out) of the sign bit signals compared to the load of other signals and accordingly slows down the speed of the circuit.

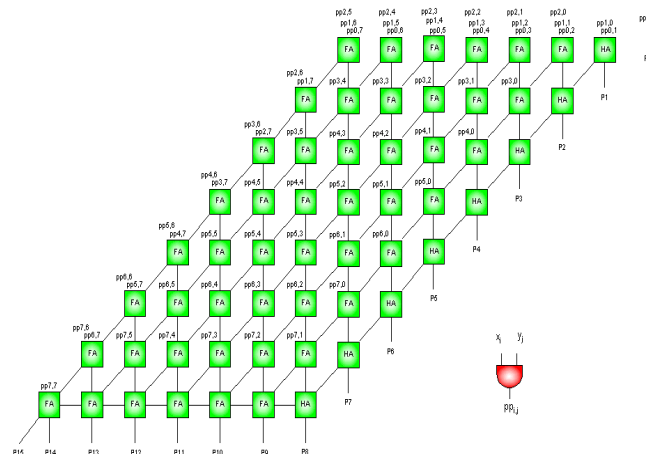


Fig. 5: Array Multiplier.

D Flip Flop:

The D flip-flop is widely used. It is also known as a "data" or "delay" flip-flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line. The D flip flop is shown in Fig.6.

These flip-flops are very useful, as they form the basis for shift registers, which are an essential part of many electronic devices. The advantage of the D flip-flop over the D-type "transparent latch" is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. An exception is that some flip-flops have a "reset" signal input, which will reset Q (to zero), and may be either asynchronous or synchronous with the clock. The above circuit shifts the

contents of the register to the right, one bit position on each active transition of the clock. The input X is shifted into the leftmost bit position.

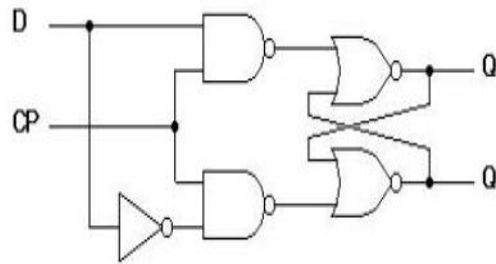


Fig. 6: D flip flop.

RESULTS AND DISCUSSIONS

FIR filter using 6 transistor Full Adder is designed using 90nm Technology and simulated in HSPICE.

Table 1: Transistor Utilization.

	Conventional FIR Filter	6T FA Based FIR Filter
INVERTER	2	2
AND	6	6
EXOR	12	2
HALF ADDER	18	8
FULL ADDER	42	6
RCA 16 BIT	672	96
MULTIPLIER (8*8)	2880	736
D F/F 8BIT	36	36
FIR8TAP	28878	7812

About 50% of Transistors are minimized in 6T Full Adder based FIR filter compared to conventional FIR filter.

Table 2: Parameters Analyzed.

LOGIC STYLES	Parameters		
	Power (mW)	Delay (ns)	Power Delay Product $\times 10^{-15}$ (Ws)
Conventional FIR Filter	27	1.089	29403
FIR Filter using 6T Full Adder	17.5	1.32	23100

The Power Delay Product(PDP) is 30% reduced in FIR filter using 6T Full Adder compared to the conventional FIR filter.

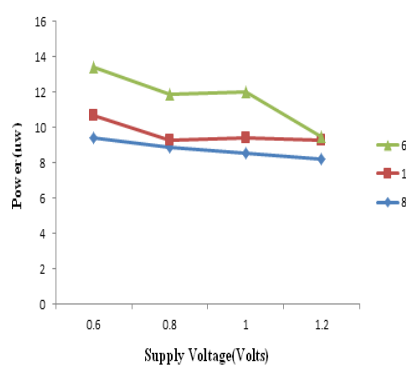


Fig. 7a: Power vs Supply Voltage.

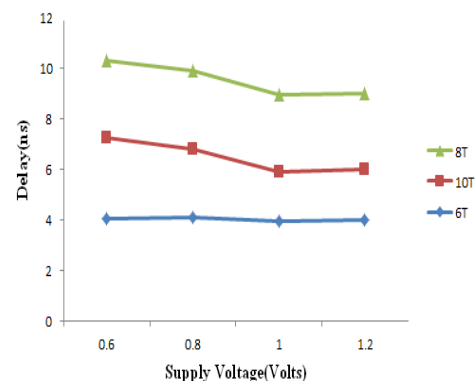


Fig. 7b: Delay vs Supply Voltage.

In the Fig.7a and 7b for various supply voltage the power dissipation and delay for FIR filter using different number of transistor Full Adder are compared respectively.

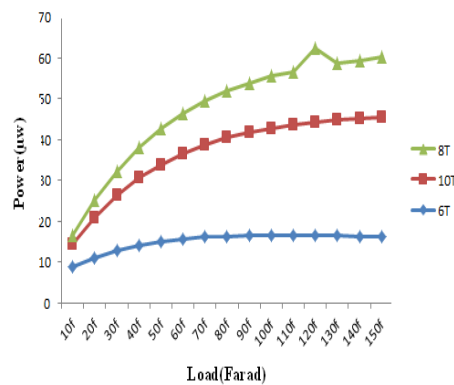


Fig. 8a: Power vs Load.

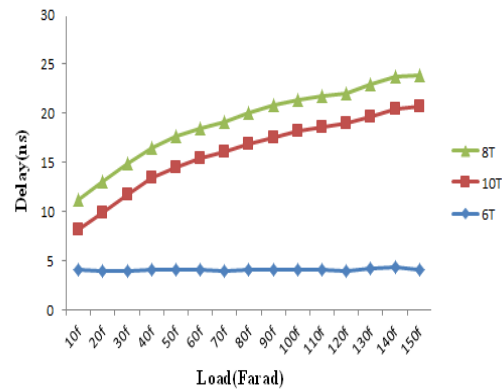


Fig. 8b: Delay vs Load.

In the Figure.9a and 9b for various Load Capacitance the power dissipation and delay for FIR filter using different number of transistor Full Adder are compared respectively.

Conclusion:

The 8-tap, 8-input FIR filter is designed using 6 Transistor Full Adder. The FIR filter is found to be energy efficient due to low power delay product and less switching activity. The FIR filter consumes only 17.5mW power which is 31% less than conventional logic. The proposed filter is designed in Custom Designer tool and has been simulated in HSPICE 90nm Technology. Thus the reduced power usage in the proposed adder with its sub-blocks like Ripple Carry adder, hybrid array multiplier leads to overall power reduction of FIR filter.

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