



AENSI Journals

Australian Journal of Basic and Applied Sciences

ISSN:1991-8178

Journal home page: www.ajbasweb.com



Performance comparison between Modified and Improved Bridgeless Boost Converters

¹Tamizhselvan Annamalai and ²Dr.V.Rajini

¹Research Scholar, Department of Electrical and Electronics Engineering, SSN College of Engineering, OMR Salai, Kalavakkam, Chennai, Tamilnadu, India

² Professor, Department of Electrical and Electronics Engineering, SSN College of Engineering, OMR Salai, Kalavakkam, Chennai, Tamilnadu, India.

ARTICLE INFO

Article history:

Received 19 August 2014

Received in revised form

19 September 2014

Accepted 29 November 2014

Available online 15 December 2014

Keywords:

Modified Bridgeless converter,
Improved Bridgeless converter,
Switching controller, Unity power factor,
Total Harmonic distortion,
Performance Comparison.

ABSTRACT

Background: Performance Comparison of Single Phase Bridgeless converters. **Objective:** Simulation of a Resistive input behaviour of Single Phase Bridgeless converters is presented. **Results:** The proposed approach provides unity power factor operation for all dynamic load conditions and all dynamic source operations. **Conclusion:** The Single Phase Resistive Bridgeless Converters with proposed switching controller is analyzed and simulated using MATLAB-SIMULINK. In order to transfer an efficient power from an irregular source in to a load or to a battery, a new control technique for a modified bridgeless boost converter is designed and developed and its performance is also analyzed. Based on the operation of modified bridgeless converter circuit, a new input resistance relationship is obtained. Then a novel modeling of switching controller is developed that regulates the input resistance to a desired value. Hence input power factor is unity and also the total harmonic distortion is controlled to a tolerable limit. Finally the performance of the modified bridgeless converter is compared with the basic improved bridgeless converter.

© 2014 AENSI Publisher All rights reserved.

To Cite This Article: Tamizhselvan Annamalai and Dr.V.Rajini., Performance comparison between Modified and Improved Bridgeless Boost Converters. *Aust. J. Basic & Appl. Sci.*, 8(18): 554-564, 2014

INTRODUCTION

Power supplies with active power factor correction (PFC) techniques are becoming necessary for many types of electronic equipment to meet harmonic regulations and standards such as the IEC 61000-3-2 and IEEE 519. Most of the PFC rectifiers utilize a boost converter at their front end. However, a conventional PFC scheme has lower efficiency due to significant losses in the diode bridge. Also the input operating power factor is lagging in nature. Operation under unity power factor is an important feature in AC to DC Boost power converters. In this regard, the previous researchers have used only sinusoidal input voltage and currents with known input frequencies for power line applications (Liu and Chang, 2009). The conventional methods of converting AC to DC are not sufficient to meet the requirements in high efficiency power applications. So, various topologies of switch-mode boost converters are developed for efficient power conversion. In (Kazerani et al., 1991; Vazquez et al., 2005) the PFC method with active current wave shaping was presented. A boost converter topology was introduced in (Louganski and Lai, 2007) to eliminate the leading phase distortion. One more boost converter topology was presented in (Kwon et al., 2008) to reduce the reverse recovery losses of the diode. Various solutions to reducing the reverse recovery losses were mentioned in (Zhao et al., 2001; Lu et al., 2003; Su and Lu, 2010). In (Crebieret et al., 2005), the merits and demerits of various boost converter topologies were discussed. In (Martinez and Enjeti, 1996), the demerits of conventional boost type PFC circuit were eliminated. The advantages of using boost converters were discussed in (Huber et al., 2008). Classification of single stage converters with respect to the AC source frequency and the absence of large bulk capacitor in the DC link was discussed in (Moschopoulos and Jain, 2005). The safety isolation in an isolated boost converters were presented in (Mi et al., 2003; Chow et al., 2000; Zhu et al., 2003). Mixed mode operation of a boost rectifier for a wide range of load variations was presented in (Tripathi et al., 2002). A theoretical study of switching power converters with PFC were discussed in (Tse and Chow, 2000; Tse, 2003) in which the resistive behaviour were elaborated in an open loop.

The above works have mainly focussed on the boost power converters using sinusoidal input with known input frequencies. In wind energy conversion systems the input voltage amplitude and input frequency are time

Corresponding Author: Tamizhselvan Annamalai, Research Scholar, Department of Electrical and Electronics Engineering, SSN College of Engineering, OMR Salai, Kalavakkam, Chennai, Tamilnadu, India

varying in nature and also in SMPS and UPS applications constant regulated voltage is required. To achieve maximum power absorption and to reduce the total harmonic distortion we should enforce the resistive input behaviour at the input of the boost converters that is independent of the input characteristics. In this paper the proposed switching controller provides the desired resistive input behaviour. The performance comparisons between modified bridgeless boost converter and improved bridgeless boost converter have been elaborated in closed loop.

MATERIALS AND METHODS

PFC Circuit:

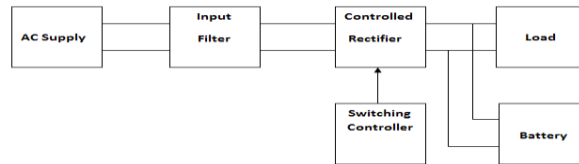


Fig. 01: Schematic of a PFC Circuit.

The general schematic of a PFC circuit is shown in Figure 01. The controlled rectifier may be a modified bridgeless boost converter circuit or improved bridgeless boost converter circuit.

Modified Bridgeless Boost Converter:

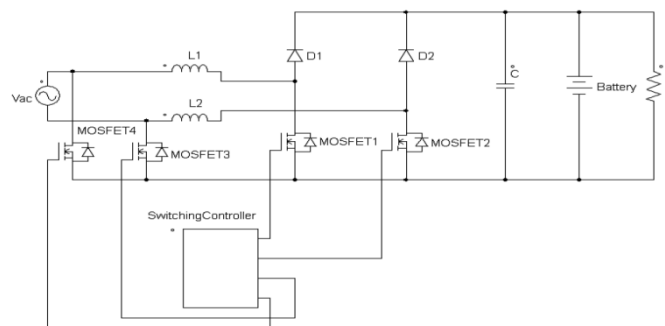


Fig. 02: Modified Bridgeless Boost Converter Circuit.

The basic topology of the Modified Bridgeless AC–DC PFC boost converter is shown in Figure 02. The Schottky Diodes and MOSFETs are used to achieve the lower conduction losses. To decrease the conduction losses, MOSFET 2 is kept on when the time varying input voltage Vac is positive. Similarly, MOSFET 1 is kept on when the time varying input voltage is negative.

Operating Principle:

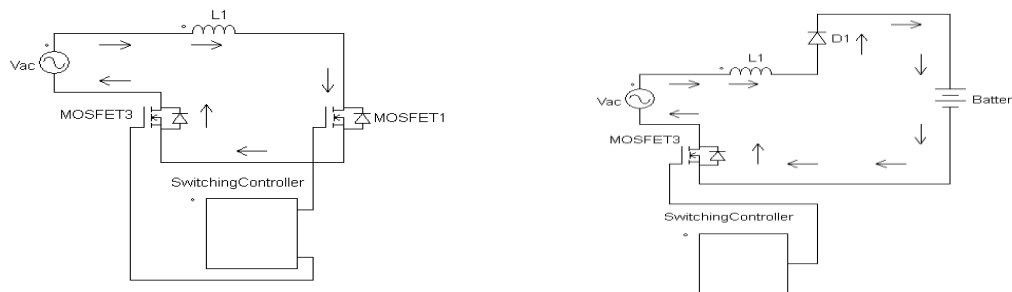


Figure.03(a): Mode 1 Operation.

(b): Mode 2 Operation.

Mode 1 Operation:

When $V_{ac} > 0$ and MOSFET1 is turned on, the current starts flowing from Vac towards L1, MOSFET1, MOSFET3 and back to Vac, Thus energy starts building in the inductor and inductor stores energy in the electromagnetic fields. We denote this as a Mode 1 of operation. Refer the Figure 03 (a).

Mode 2 Operation:

When MOSFET1 is turned off, the potential across the inductor is gets added to the source voltage and this net potential charges the battery.Thus current starts flowing from Vac towards L1,D1,Battery,MOSFET3 and back to Vac. We denote this as a Mode 2 of operation.Refer the Figure 03 (b).

Similarly, When Vac < 0 L2, MOSFET2, D2 and MOSFTE4 are active.

Improved Bridgeless Boost Converter:

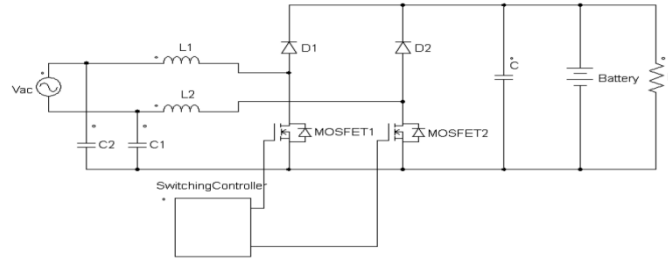


Fig. 04: ImprovedBridgeless Boost Converter Circuit.

The basic topology of Improved Bridgeless AC–DC PFC boost converter is shown in Figure 04.

Operating Principle:

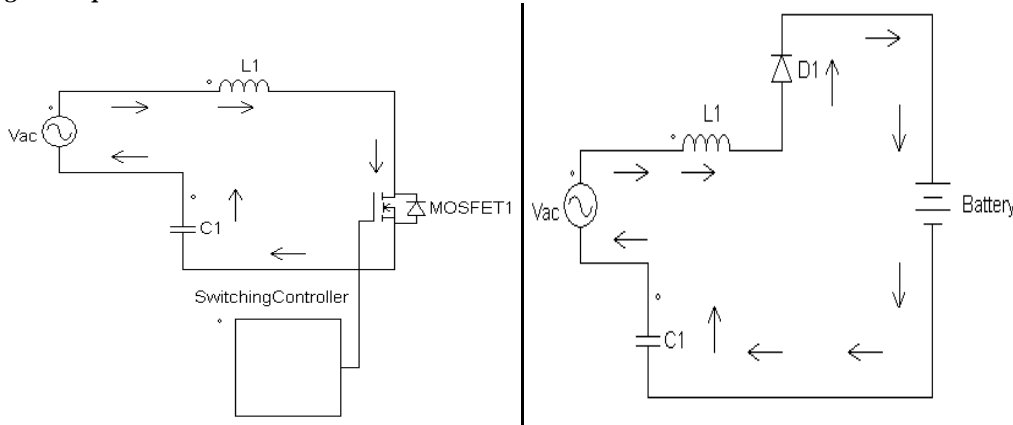


Fig. 05(a): Mode 1 Operation.

(b): Mode 2 Operation.

Mode 1 Operation:

When Vac > 0 and MOSFET1 is turned on, the current starts flowing from Vac towards L1,MOSFET1,C1 and back to Vac, Thus energy starts building in the inductor and inductor stores energy in the electromagnetic fields. We denote this as a Mode 1 of operation.Refer the Figure 05 (a).

Mode 2 Operation:

When MOSFET1 is turned off, the potential across the inductor is gets added to the source voltage and this net potential charges the battery.Thus current starts flowing from Vac towards L1,D1,Battery,C1 and back to Vac. We denote this as a Mode 2 of operation.Refer the Figure 05 (b).

Similarly, When Vac < 0 L2, MOSFET2, D2 and C2 are active.

Transient Analysis:

In Mode 1 operation the inductor current can be written as

$$iL(t) = iL(t_1) + \frac{1}{L} \int_{t_1}^t Vac(t) dt, \quad t_1 \leq t \leq kTs \tag{1}$$

Where k – Sampling Time, Ts – Switching period of MOSFET1 and t1– starting time of switching cycle

When time t = t1, MOSFET 1 is turned on and the total inductor current is the sum of initial inductor current due to previous switching cycle and the inductor charging current between the instants t1 to kTs. The MOSFET voltage drop is ignored when it is on.

In Mode 2 operation the inductor current equation can be written as

$$iL(t) = iL(kTs) + \frac{1}{L} \int_{kTs}^t (Vac(t) - VB - VD1) dt, \quad kTs \leq t \leq t_2 \tag{2}$$

Where V_B – Battery Voltage and V_{D1} – Voltage drop across the diode $D1$

When time $t = kT_s$, MOSFET 1 is turned off and the total inductor current is the sum of initial inductor current during charging and the inductor discharging current between the instants kT_s to t_2 . Again the MOSFET voltage drop is ignored.

By using averaging technique the inductor current can be written as

$$i_L(t) = \frac{\Delta Q}{T_s} = \frac{1}{2LT_s} V_{ac} t_{on} \left(1 - \frac{V_{ac}}{V_{ac} - V_B - V_{D1}}\right) \quad (3)$$

Where Q – Total charge passing through the inductor and t_{on} – On time

From the above equation, there exists a non- linear resistance between the input terminals.

After some algebraic manipulations, the input resistance can be written as

$$R_{in} = \frac{2LT_s}{t_{on}} \left(1 - \frac{V_{ac}}{V_B + V_{D1}}\right) \quad (4)$$

From the above equation it is very clear that the input resistance is proportional to L , T_s and inversely proportional to t_{on} .

Condition for Resistive Input Behaviour:

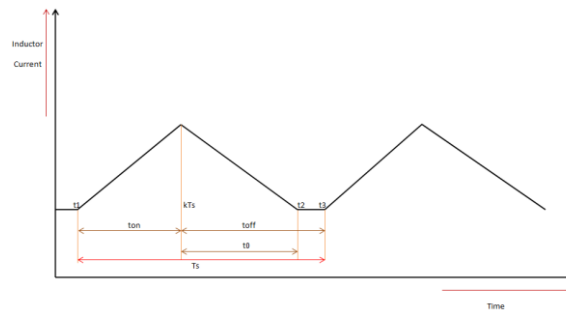


Fig. 06: Transient Characteristics of Inductor Current.

We know that, from the Figure 06, $t_0 \leq t_{off}$

To find t_0 , we set $i_L(t_2) = 0$. Hence,

$$t_0 = \frac{V_{ac} t_{on}}{(V_B + V_{D1} - V_{ac})} \quad (5)$$

The on time and off time can be written in terms of duty cycles are as follows

$$t_{on} = dT_s$$

$$t_{off} = (1-d) T_s \quad (6)$$

Using (5) and (6) and after performing some algebraic manipulations

$$d(V_B + V_{D1}) \leq V_B + V_{D1} - V_{ac} \quad (7)$$

Therefore the condition to achieve resistive input behaviour is as follows

$$d \leq \left(1 - \frac{V_{ac}}{(V_B + V_{D1})}\right) \quad (8)$$

Thus the duty cycle is depends only on the input voltage, Battery Voltage and Voltage drop across the diode. That is the circuit can be activated in to a pure resistive mode only when the duty cycle satisfies the above equation.

Proposed Control System Methodology:

From (4), R_{in} depends on Switching Time, on time and Inductance. Since switching frequency is fixed, hence switching period T_s is generally cannot be a proper control variable, inductor is also fixed and then the only parameter which changes and affects the value of input resistance is on time. Thus we can select t_{on} as a control variable and also it is depends on duty cycle d .

Now Let us consider,

$$\text{Let } b = V_B + V_{D1}, R_{in} = V_{ac}/i_L, c = \frac{2LT_s}{t_{on}}, V_{ac} = v \quad (9)$$

Using (9) in (4)

$$R_{in} = c \left(\frac{b-v}{b}\right) \quad (10)$$

Now Let us define,

$$c = R_d + \Delta R \quad (11)$$

Where R_d – Desired resistance of the input circuit

Using (11) in (10)

$$R_{in} = (R_d + \Delta R) \left(\frac{b-v}{b} \right) \quad (12)$$

By defining

$$\text{Error } \delta e = R_d - R_{in} \quad (13)$$

Using (12) in (13)

$$\delta e = R_d - \left[(R_d + \Delta R) \left(\frac{b-v}{b} \right) \right] \quad (14)$$

If ΔR is defined as

$$\Delta R = \left(1 - \left(\frac{v}{b} \right) \right)^{-1} (z + (v/b) R_d) \quad (15)$$

By using (15) in (14)

$$\delta e = -z \quad (16)$$

If z is the output of the PI Controller

$$\text{Then } z = K_p \delta e + K_i \int \delta e \, dt \quad (17)$$

Using (17) in (16)

$$(1 + K_p) \delta e + K_i \int \delta e \, dt \quad (18)$$

Using (15) in (11) and after some mathematical manipulations

$$c = b / (b - v) (R_d + z) \quad (19)$$

The value of duty cycle d is calculated using (9) and c is given by (19).

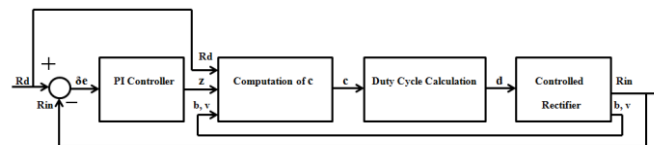


Fig. 07: Proposed Control System Methodology.

The above Figure 07 illustrates the block diagram of proposed control system methodology in which PWM signals are generated by the controller and duty cycle is adjusted by the controller to obtain the resistive input behaviour.

RESULTS AND DISCUSSION

Simulation Results:

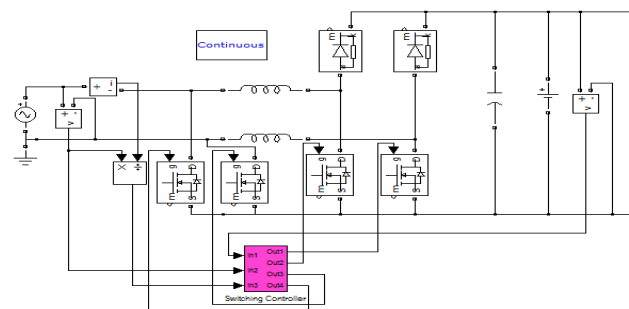


Fig. 08: Simulink Model of the Modified Bridgeless Boost Converter with Proposed Controller.

A Simulink model of the resistive bridgeless converters and its proposed controllers were developed using MATLAB with the following parameters: V_{ac} (Peak) = 6V, $C = 100\mu\text{F}$, $R = 1\text{k}\Omega$, $L_1 = 0.1\text{H}$, $L_2 = 0.1\text{H}$, $C_1 = 0.1\mu\text{F}$, $C_2 = 0.1\mu\text{F}$, $f_i = 50\text{Hz}$ and $f_s = 1\text{kHz}$; Where f_i and f_s are the input and switching frequencies respectively. The Simulink model of the modified bridgeless converter and improved bridgeless converter with proposed controllers are shown in the Figures 08 and 09 respectively.

The resistive bridgeless converter circuits are simulated. For different loads, it has been observed that the source currents are exactly in phase with the voltages. The input power factor is 0.99, nearly unity. This is achieved by tuning the duty cycle of the PWM signals. Figures 10, 11, 12 and 13 stretches the results obtained for a desired input resistance of $R_d = 5\text{k}\Omega$ and a duty cycle of $d = 0.20$.

The above Figures 14 and 15 illustrates the harmonic current patterns of modified and improved bridgeless boost converter circuits respectively. The THD contents are 2.71% and 2.15% which is less than the guidelines

given in the IEC 61000-3-2 and IEEE 519 standards. The PWM signals of the MOSFETs are shown in the Figure 16 and Figure 17.

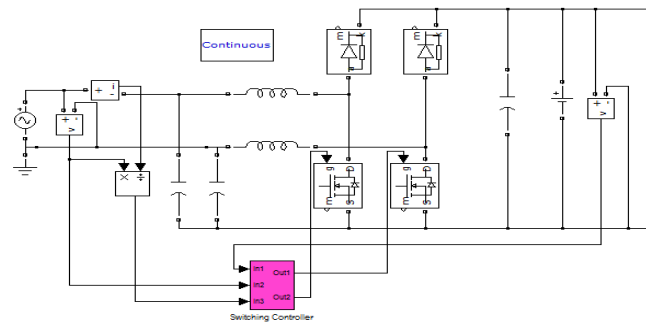


Fig. 09: Simulink Model of the Improved Bridgeless Boost Converter with Proposed Controller.

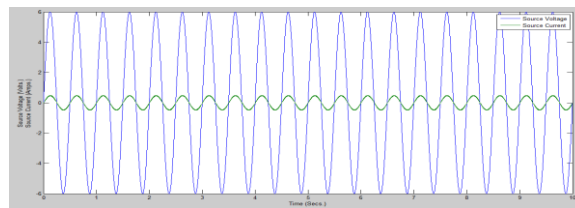


Fig. 10: Source Voltage and Source Current Waveforms of modified bridgeless boost converter.

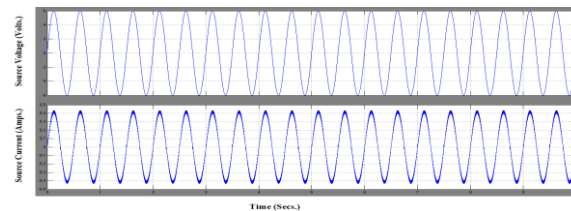


Fig. 11: Source Voltage and Source Current Waveforms of modified bridgeless boost converter for resistive input behaviour.

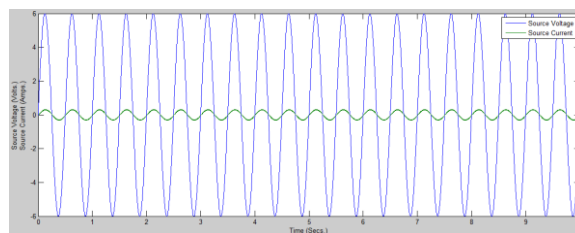


Fig. 12: Source Voltage and Source Current Waveforms of improved bridgeless boost converter.

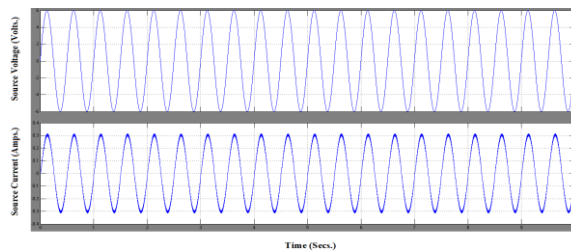


Fig. 13: Source Voltage and Source Current Waveforms of improved bridgeless boost converter for resistive input behaviour.

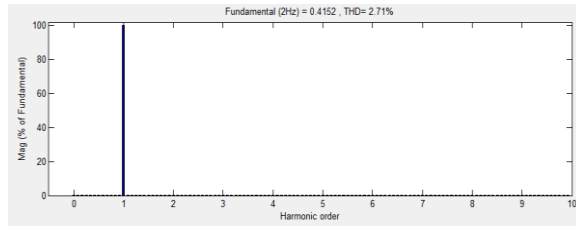


Fig. 14: Harmonic Current Pattern of modified bridgeless boost converter.

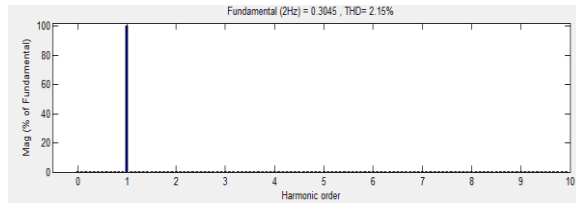


Fig. 15: Harmonic Current Pattern of improved bridgeless boost converter.

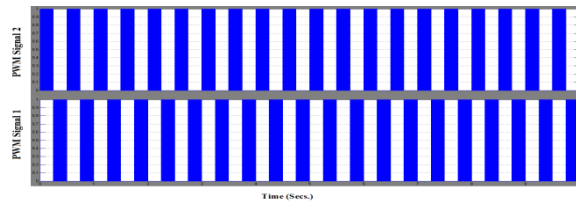


Fig. 16: PWM Signals.

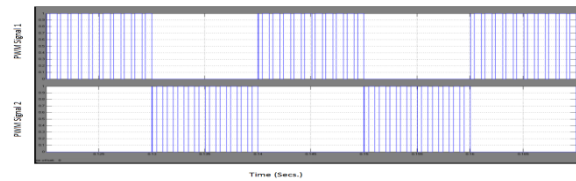


Fig. 17: PWM Signals.

When the duty cycle is less than the bound given by (8) (ie., $d \leq 0.7561$); hence the circuit operates in the pure resistive mode. The proposed controller is used to achieve the desired resistance by adjusting the duty cycle of PWM signals. The duty cycle oscillation at 36% is shown in the Figure 18. Since $b/(b - v)$ is very close to unity, this term is assumed to be one in controller implementation. Considering (4) and ignoring the term $\frac{V_{ac}}{V_B + V_{D1}}$ which is typically small for a boost converter, which yields the resultant $R_{in} = 5k\Omega$, when the duty cycle of the PWM signal is 20%. The duty cycle oscillation at 20% is shown in Figure 19.

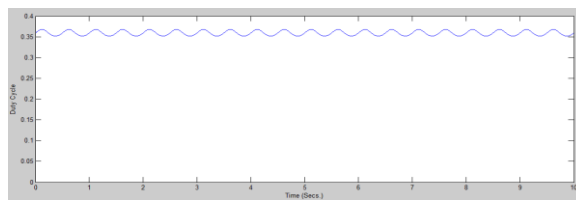


Fig. 18: Duty Cycle of PWM Signal (d = 36%).

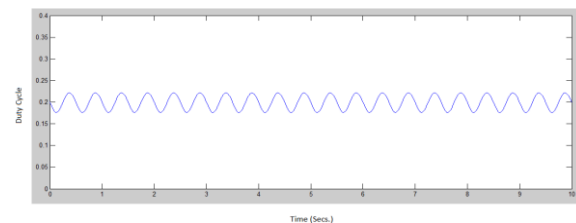


Fig. 19: Duty Cycle of PWM Signal (d = 20%).

Performance Comparison:

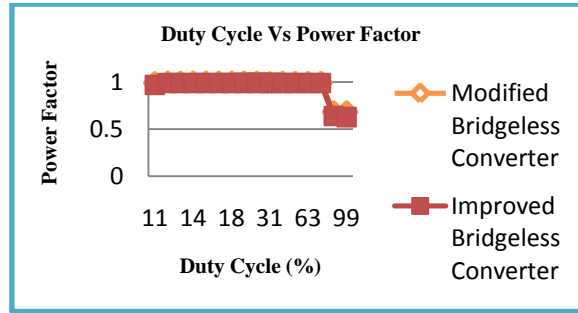


Fig. 20: Comparison of Duty Cycle Vs THD.

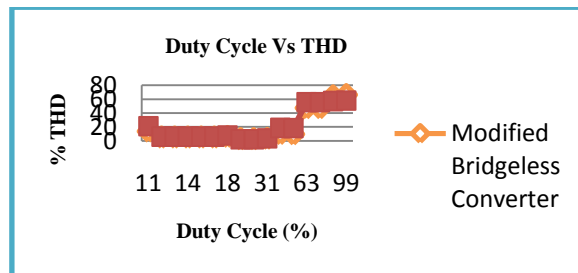


Fig. 21: Comparison of Duty Cycle Vs Power Factor.

In order to vary the duty cycle the desired resistance R_d has been adjusted and the corresponding changes in power factor and THD has been obtained. From the Figure 20, it is very clear that when $d \leq 0.7561$, the power factor is unity and the bridgeless converters are operated in pure resistive mode and when $d \geq 0.7561$, the power factor immediately decreases which indicates the inductive nature of the converter circuits. Hence when the duty cycle is more than the bound given by (8), then the bridgeless converter enters in to inductive mode.

It has been observed that Duty Cycle Vs current THD and Duty Cycle Vs Power factor characteristics of both the converters are almost similar. Figures 20 and 21 gives the results obtained for a load resistance of 1 k Ω and the source voltage of 6 V.

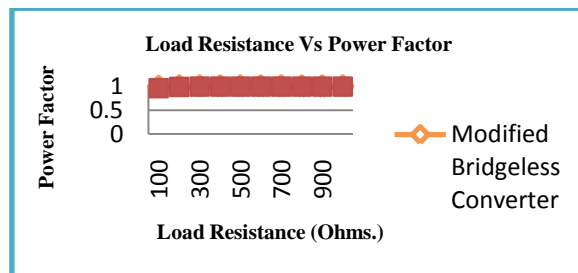


Fig. 22: Comparison of Load Resistance Vs Power Factor.

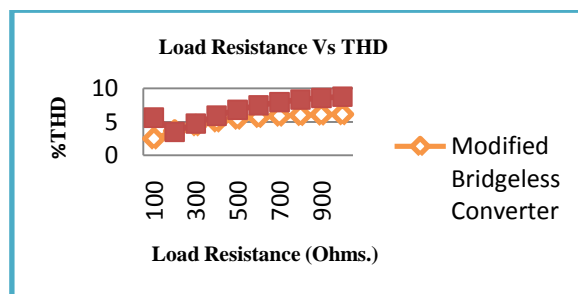


Fig. 23: Comparison of Load Resistance Vs THD.

The load resistance has been changed in the steps of 100 ohms and the corresponding variations in power factor and THD has been obtained. It has been observed that irrespective of load variations, the power factor is always unity in both the converters. The THD contents of modified bridgeless boost converter is very less compared to improved bridgeless boost converter during dynamic load conditions. Figures 22 and 23 stretches the results obtained for a desired input resistance of $R_d = 5 \text{ k}\Omega$ and a duty cycle of $d = 20\%$.

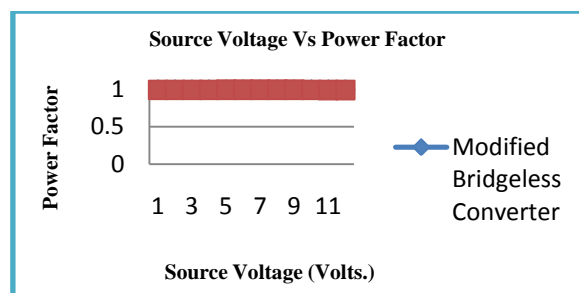


Fig. 24: Comparison of Source Voltage Vs Power Factor.

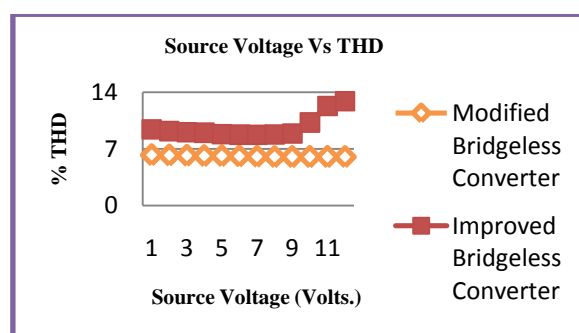


Fig. 25: Comparison of Source Voltage Vs THD.

The source voltage has been changed in the steps of 1 Volts and the corresponding variations in power factor and THD has been obtained. It has been observed that irrespective of source voltage variations, the power factor is always unity in both the converters. When dynamic source is used, the THD contents of modified bridgeless boost converter is very less compared to improved bridgeless boost converter. Figures 24 and 25 gives the results obtained for a desired input resistance of $R_d = 5 \text{ k}\Omega$ and a duty cycle of $d = 20\%$.

Table 1: Standard Simulation Data, Performance parameters and Operating Behaviour.

Name of the Topology	Vac = 6 V; Duty Cycle d = 20%; Load Resistance = 1 k Ω ; Desired Input Resistance Rd = 5 k Ω			
	%THD	Power factor	Resistive Mode	Inductive Mode
Modified Bridgeless Converter	2.71%	0.99	When $d \leq 0.7561$	When $d \geq 0.7561$
Improved Bridgeless Converter	2.15%	0.99	When $d \leq 0.7561$	When $d \geq 0.7561$

Table 2: Dynamic Source Condition Data and Performance parameters.

Name of the Topology	Duty Cycle d = 20%; Load Resistance = 1 k Ω ; Desired Input Resistance Rd = 5 k Ω		
	%THD		Power factor
	Minimum Value	Maximum Value	
Modified Bridgeless Converter	5.99%	6.25%	0.99
Improved Bridgeless Converter	8.75%	12.91%	0.99

Table 3: Dynamic Load Condition Data and Performance parameters.

Name of the Topology	Vac = 6 V; Duty Cycle d = 20%; Desired Input Resistance Rd = 5 k Ω		
	%THD		Power factor
	Minimum Value	Maximum Value	
Modified Bridgeless Converter	2.48%	6.10%	0.99
Improved Bridgeless Converter	3.49%	8.76%	0.99

The various performance comparisons are shown in the Tables 1, 2 and 3. From the Tables 1, 2 and 3 it can be inferred that when dynamic source and dynamic loads are used, the THD contents of modified bridgeless boost converter is very less; hence this converter can be used where the input power and loads are changing frequently.

In modified bridgeless boost converter circuit, the parasitic capacitance effect and common mode-noise has been suppressed by using two additional MOSFET's in the line current path. The drawback of modified bridgeless converter is that it requires two inductors, but this converter has better thermal performance compared to improved bridgeless converter.

In improved boost converter circuit, the additional capacitors C1 and C2 are creates high frequency path between the output voltages to the ac input line and hence low common-mode noise. So EMI problem is limited.

Conclusion:

A single phase resistive modified bridgeless boost converter has been designed and its performance was analyzed. The switching controller has been implemented using MATLAB Simulink. The duty cycle of the PWM signals was controlled to get a resistive input behaviour (When $d \leq 0.7561$). When the duty cycle is more than 0.7561, then the circuit enters in to inductive mode; that is the input current vector lags the input voltage vector. The modified bridgeless boost converter with proposed switching controller circuit provides the unity power factor. The THD also has been controlled to a tolerable limit. Finally the performance comparisons between modified bridgeless and improved bridgeless boost converters have been done. When dynamic source and dynamic loads are used, the THD content of modified bridgeless boost converter is very less. For dynamic load variations as well as for dynamic source variations, the input power factor is always unity.

REFERENCES

- Crebier, J.C., B. Revol and J.P. Ferrieux, 2005. Boost chopper derived PFC rectifiers: Interest and Reality. *IEEE Transactions on Industrial Electronics*, 52: 36-45.
- Chow, M.H.L., Y.S. Lee and C.K. Tse, 2000. Single stage single switch isolated PFC regulator with unity power factor, fast transient response and low voltage stress. *IEEE Transactions on Power Electronics*, 15: 156-163.
- Huber, L., Y. Jang and M.M. Jovanovic, 2008. Performance evaluation of bridgeless PFC boost rectifiers. *IEEE Transactions on Power Electronics*, 23: 1381-1390.
- Kazerani, M., P.D. Ziogas and G. Joos, 1991. A novel active current wave shaping technique for solid state input power factor conditioner. *IEEE Transactions on Industrial Electronics*, 38:72-78.
- Kwon, J.M., W.Y. Choi and B.H. Kwon, 2008. Cost effective boost converter with reverse recovery reduction and power factor correction. *IEEE Transactions on Industrial Electronics*, 55: 471-473.
- Liu, Y.M., L.K. Chang, 2009. Single-stage soft-switching AC-DC converter with input current shaping for universal line. *IEEE Transactions on Industrial Electronics*, 56: 467-479.
- Louganski, K.P., J.S. Lai, 2007. Current phase lead compensation in single phase PFC boost converters with a reduced switching frequency to line frequency ratio. *IEEE Transactions on Power Electronics*, 22(1): 113-119.
- Lu, D.D.C., D.K.W. Cheng and Y.S. Lee, 2003. A single switch continuous conduction mode boost converter with reduced reverse recovery and switching losses. *IEEE Transactions on Industrial Electronics*, 50: 767-76.
- Martinez, R., P.N. Enjeti, 1996. A high performance single phase rectifier with input power factor correction. *IEEE Transactions on Power Electronics*, 11: 311-317.
- Mi, N., B. Sasic, J. Marshall and S. Tomasiewicz, 2003. A novel economical single stage battery charger with power factor correction. *IEEE of Applied Power Electronics Conference and Exposition*, 2: 760-763.
- Moschopoulos, G., P. Jain, 2005. Single phase single stage power factor corrected converter topologies. *IEEE Transactions on Industrial Electronics*, 52: 23-35.
- Su, B., Lu, Z., 2010. An interleaved totem pole boost bridgeless rectifier with reduced recovery problems for power factor correction. *IEEE Transactions on Power Electronics*, 25:1406-1415.
- Tripathi, R.K., S.P. Das and G.H. Dubey, 2002. Mixed mode operation of boost switch mode rectifier for wide range of load variations. *IEEE Transactions on Power Electronics*, 17(6):999-1009.
- Tse, C.K., 2003. Circuit theory of power factor correction in switching converters. *International Journal of Circuit Theory Applications*, 31(1):157-198.
- Tse, C.K., M.H.L. Chow, 2000. Theoretical study of switching power converters with power factor correction and output regulation. *IEEE Transactions on Circuits Systems – I: Fundamental Theory Applications*, 47: 1047-1055.
- Vazquez, N., J. Lopez, J. Arau, C. Hernandez and E. Rodriguez, 2005. A different approach to implement an active input current shaper. *IEEE Transactions on Industrial Electronics*, 52: 132-138.

Zhao, Q., F. Tao, P.C. Lee, P. Xu and J. Wei, 2001. A simple and effective method to alleviate the rectifier reverse recovery problem in continuous current mode boost converters. IEEE Transactions on Power Electronics, 16: 649-658.

Zhu, L., K. Wang, F.C. Lee and J.S. Lai, 2003. New start up schemes for isolated full bridge boost converters. IEEE Transactions on Power Electronics, 18: 946-951.