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Design of A Low Power and Wide Band True Single-Phase Clock Frequency Divider

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Abstract: The design of frequency synthesizer, often implemented by a phase-locked loop (PLL), is a challenging task for RF designers in terms of power dissipation. In this paper an ultra-low power wide band 2/3 prescaler simulated by CEDEC 0.18 μm CMOS technology is presented. The proposed prescaler is capable of operating up to 8 GHz with smooth output waveform for divide-by-2 operation. Compared with concurrent extended true single phase clock (E-TSPC) circuits at supply voltage of 1.8 V, more than 50% reduction in total power consumption is achieved for both divide-by-2 and divide-by-3 operations. It consumes 0.05 mW and 0.68 mW of power during divide-by-2 and divide-by-3 modes respectively.

Key words: Frequency divider, Prescaler, True single-phase clock (TSPC), E-TSPC.

INTRODUCTION

In wireless communication systems, a phase-locked loop (PLL) is one of the main components for transceivers (Akter *et al*., 2008; Reaz *et al*., 2006; Mohd-Yasin *et al*., 2004). PLLs are mainly used for frequency synthesis to generate a local oscillator signal to up-conversion in the transmitter and down-conversion in the receiver. It is also used in producing high frequency oscillations in modern communication equipment (Marufuzzaman *et al*., 2010; Reaz *et al*., 2003; Zhang *et al*., 2011). The basic building blocks of a PLL are given in figure 1. A PLL is composed of a phase frequency detector (PFD) followed by an analog filter and a voltage-controlled oscillator (VCO). There is also a frequency divider (FD) or prescaler stage to be used as synthesizer feedback loop (Bazzazi and Nabavi, 2009; Gu *et al*, 2011).

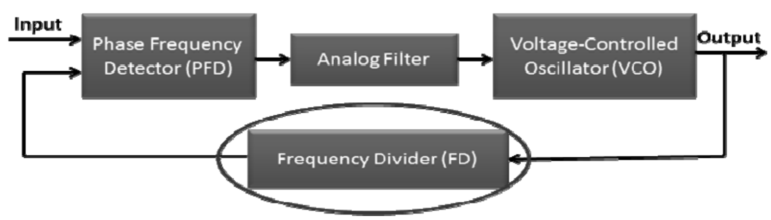

Fig. 1: Basic phase-lock loop (PLL) block diagram

For a typical PLL, prescaler is used to generate a frequency that is a multiple of the reference frequency. In PLL loop as in Figure 1, the output of VCO is divided down by the FD. Then, the divided signal and TCXO are applied to the phase detector for comparison (Cheema *et al*, 2010). FD approach makes it easier to implement low power and offer smaller phase imbalance. FD can be categorized into three parts which are digital, analog and hybrid or combination of both. The digital part can be divided into static and dynamic FDs whereas the analog part consists of regenerative divider and injection locked FD. Hybrid of digital and analog divider only consists of travelling wave FD. True single-phase clock (TSPC) is under the dynamic sub-category of FD.

The advantage of dynamic dividers over the others is reduced power consumption and less number of transistors. As in (Yu *et al*., 2006; Akter *et al*., 2008), the low power of 2/3 prescaler is proposed using a 0.18 μm CMOS technology. Compared with the existing design during that time, a 25% reduction of power consumption is achieved and maximum operating frequency up to 4 GHz. These shows that TSPC can be achieve the low power consumption. However, the operating frequency still not wide band and need to be improve. Zhiming Deng *et al*. as in (Deng and Niknejad, 2010) has improve this disadvantage by using 65 nm LP CMOS technology shows that the maximal input frequencies can be 19 GHz and 16 GHz for divide-by2 and divide-by-2/3 prescaler respectively, and the power consumption is less than 0.5 mW.

The TSPC technique for the frequency divider also can be improved in term of speed of to operate the frequencies. In (Chen *et al*., 2011), Wu-Hsin Chen *et al*. has implemented in a 130 nm technology and at same process condition, the maximum speed of the 2/3 prescaler reaches 88% of the maximum operating frequency of a single TSPC flip-flop. The maximum operating range that achieved is 3.4 – 5 GHz. However, the power

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consumption still high for achieved the maximum operating frequency which around 1 – 1.2 mW. In addition, V. Krishna Manthena *et al*. as in (Manthena *et al*., 2012) has proposed the multiband flexible divider using 0.18 μm CMOS technology that consumes power of 0.96 mW and 2.2 mW in 2.4 GHz and 5 GHz bands, respectively, when operated at 1.8 V power supply. All previous researchers have shown that TSPC can achieve the low power consumption with the wide band operating frequency that very important in frequency divider for PLL.

Extensive research is going on throughout the world on clock frequency divider to improve its performance for different applications (Manthena *et al*., 2012; Reaz *et al*., 2005; Akter *et al*., 2008; Mazzanti *et al*., 2007; Reaz *et al*., 2007; Zhang *et al*., 2011). In this paper, the power consumption and the operating frequency in the E-TPSC logic style is simulated and analyzed. There are two sources of power consumption in the proposed E-TSPC which is divide-by-2 and divide-by-3 is analyzed. Based on this analysis, the proposed E-TSPC is achieved the low power consumption by optimizing the transistor size in each divider stage. By optimize the size of transistor, the output waveform also smoother and the noise at the waveform is reduced. Finally, the proposed E-TSPC are achieved in the wide band frequency, low power consumption and reducing the noise at the output waveform.

True Single-Phase Clock (Tspc) And Extended True Single-Phase Clock (E-Tspc):

Prescaler is the most challenging part in the high-speed frequency divider design. It is usually a dual-modulus prescaler that consist of a divide-by-2/3 unit followed by several asynchronous divide-by-2 units (Guo *et al*., 2010). In each stage, TSPC flip-flop uses three transistors while an E-TSPC flip-flop uses only two transistors as shown in Figure 2.

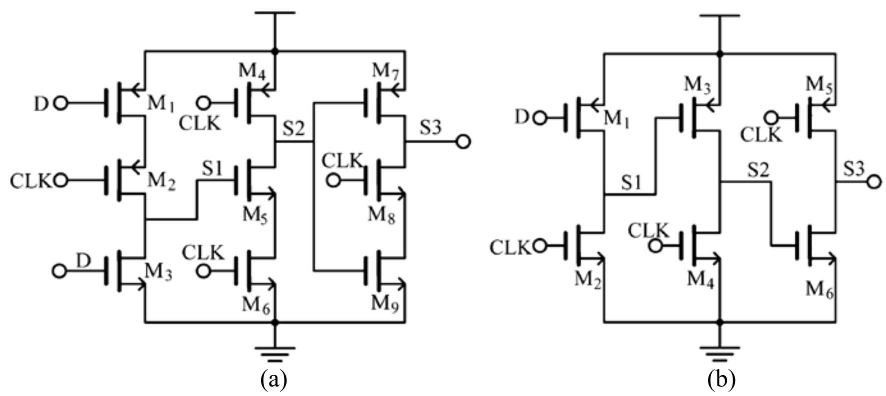


Fig. 2: Dynamic (a) TSPC and (b) E-TSPC flip-flop

In TSPC dynamic CMOS circuit, only one clock signal is operated to avoid the clock skew problems. The load capacitance of the TSPC flip-flop is higher than that of the E-TSPC flip-flop resulting in higher switching power for the TSPC flip-flop since it is directly depends on the output load capacitance. It is well known that in a 2/3 prescaler, the E-TSPC flip-flop uses lesser switching power, but significantly more short circuit power (Krishna *et al*., 2010; Ikebe *et al*, 2008).

Proposed Low Power And Wide Band 2/3 Prescaler:

The proposed wide band 2/3 prescaler consists of two D flip-flops and two NOR gates embedded in to the flip-flops as shown in Figure 3. The first NOR gate is embedded in the last stage of DFF1 and second NOR gate is embedded in the first stage of DFF2. Here, additional transistors *M*2, *M*25 and *M*4 are added in DFF1 to eliminate the short-circuit power during the divide-by-2 operation. The switching of division ratios between 2 and 3 is controlled by logic signal *MC*.

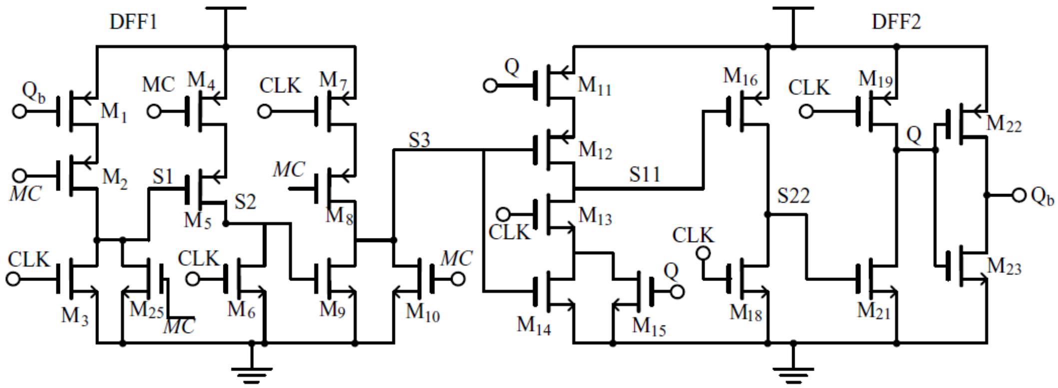


Fig. 3: Proposed low power and wideband 2/3 frequency divider

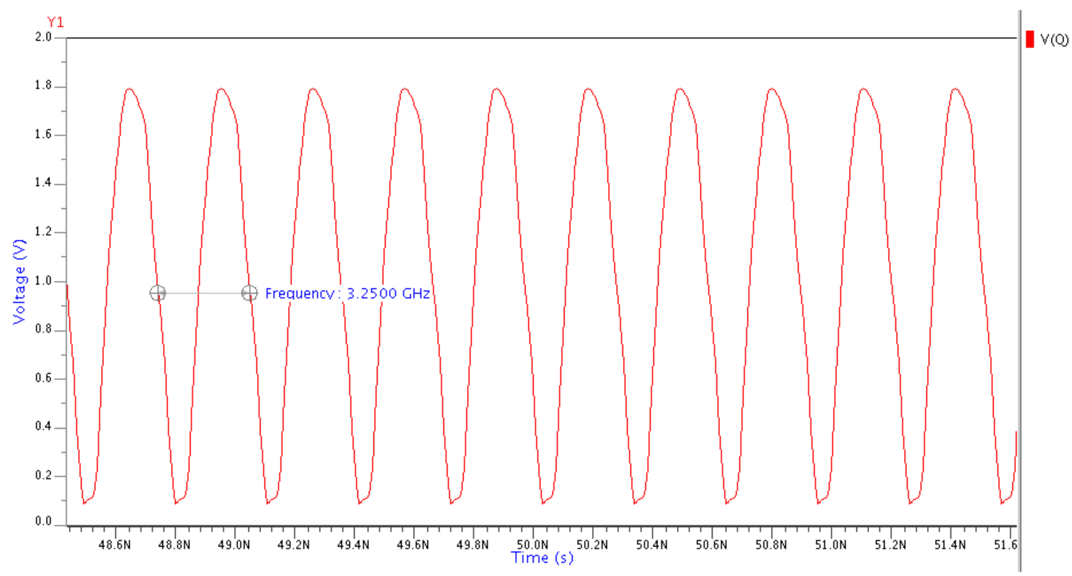
RESULTS AND DISCUSSIONS

The proposed low power and wide band 2/3 prescaler E-TSPC is designed and simulated in CEDEC 0.18 μm CMOS process. Simulations are executed to evaluate the circuit performance of the transistor sizing of the proposed 2/3 prescaler in (Krishna *et al*, 2010). The transistors and parameters involved in the 2/3 prescaler are shown as in Table I.

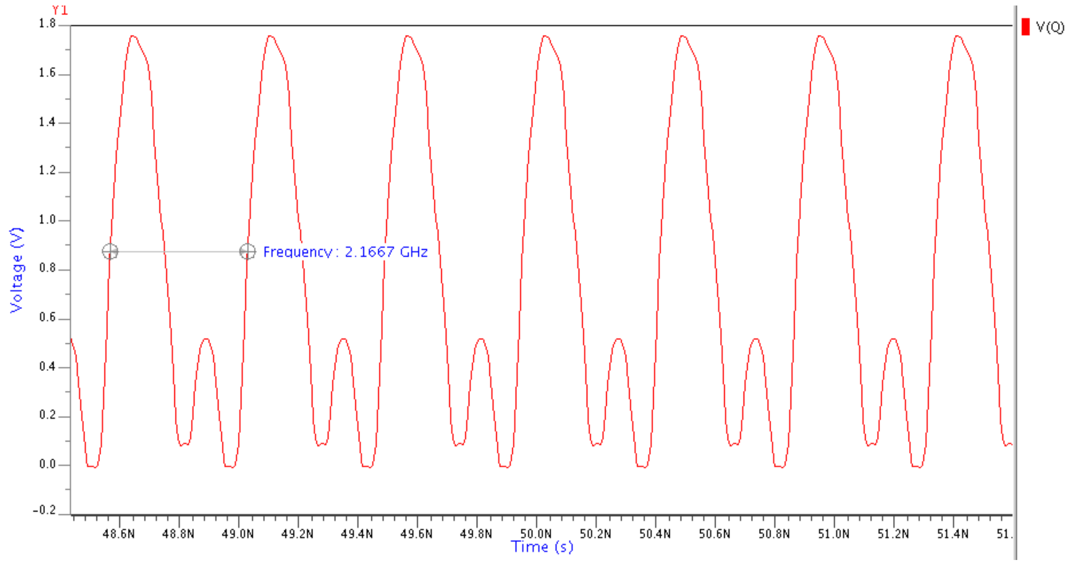
Table 1: Main Design Parameters

VDD (V)	Frequency Range (GHz)	MC Value (V)	Width for M(1,2,4,5,7,8,11,12) (μm)	Width for M(3,4,6,9,10,13,14,15,16,18,19,21,25)(μm)	Width for M22/M23(μm)
1.8	4-8	0 and 5	1.4	0.9	2/1

By using the design parameters listed in Table I, the output waveform is shown in Figure 4 under 1.8 V supply voltage. As shown in Figure 4 the transistor sizing for 2/3 prescaler give the smoother output waveform for divide-by-2 better than in (Krishna *et al*, 2010). At 6.5 GHz and 1.8 V for input frequency and supply voltage, the 2/3 prescaler gives an output waveform with 3.25 GHz and 2.1667 GHz frequency during the divide-by-2 and divide-by-3 modes respectively. For divide-by-2 mode, MC value is 5 V and 0 V for divide-by-3 mode.



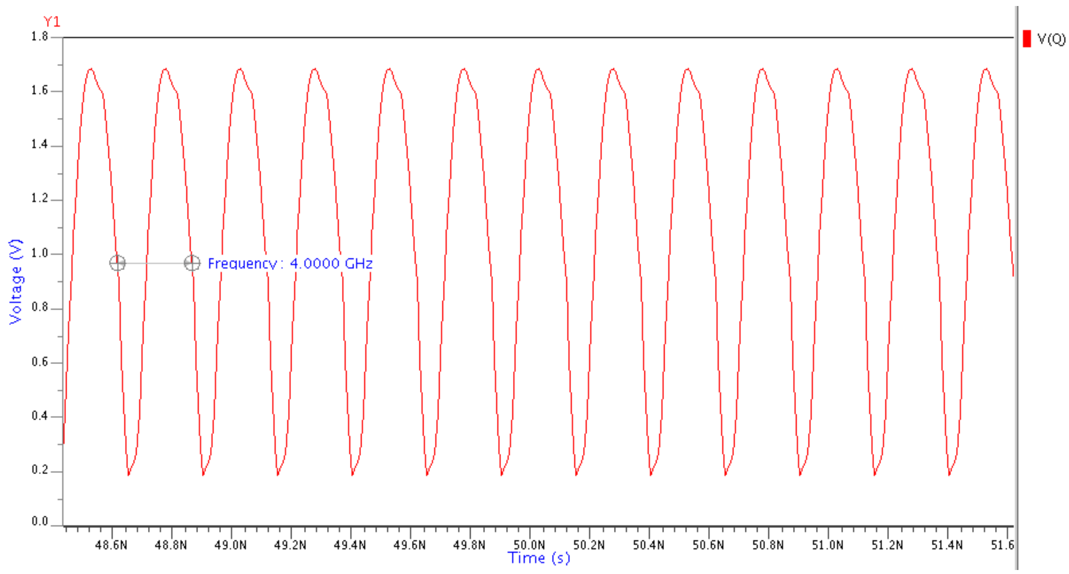
(a)



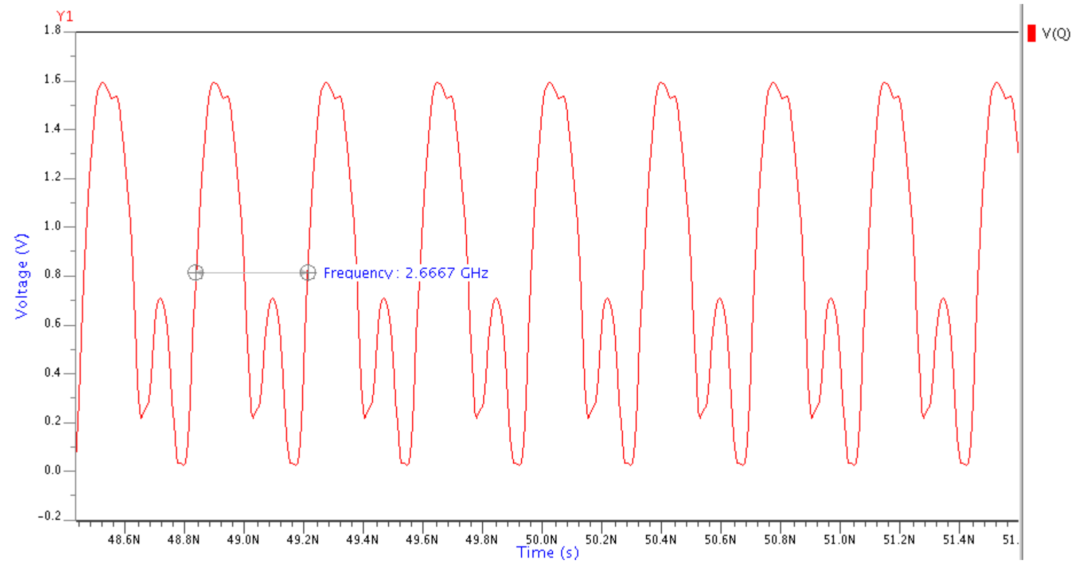
(b)

Fig. 4: Simulation result of (a) Divide-by-2 (b) Divide-by-3 at an input frequency 6.5 GHz

The simulation results shows that the proposed 2/3 prescaler has the maximum operating frequency of 8 GHz as shown in Figure 5 with a power consumption of 0.05 mW during divide-by-2 mode and 0.68 mW during divide-by-3 mode as shown in Figure 6.



(a)



(b)

Fig. 5: Simulation result of (a) Divide-by-2 (b) Divide-by-3 at an input frequency 8 GHz

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Notepad - /home/kkkc4024/azfar/schem/fd14_tb/eldonet/fd14_tb_eldonet.chi (R)
X_FD141.N$27     14.7331N
X_FD141.N$4     342.1239M
X_FD141.N$6     1.8000
X_FD141.N$8     1.2777N


 VOLTAGE SOURCE CURRENT

NAME     CURRENT     VOLTAGE     POWER
V3       0.0000      0.0000      0.0000
V2      -28.9679U    1.8000     -52.1422U
V1       0.0000      5.0000      0.0000

 TOTAL POWER DISSIPATION:  52.1422U    WATTS
```

(a)

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Notepad - /home/kkkc4024/azfar/schem/fd14_tb/eldonet/fd14_tb_eldonet.chi (R)
X_FD141.N$11     132.5313M
X_FD141.N$14     1.8000
X_FD141.N$16     1.8000
X_FD141.N$17     1.8001
X_FD141.N$2     377.7227M
X_FD141.N$27     486.8412U
X_FD141.N$4     1.8000
X_FD141.N$6     1.4141
X_FD141.N$8     75.1123M


 VOLTAGE SOURCE CURRENT

NAME     CURRENT     VOLTAGE     POWER
V3       0.0000      0.0000      0.0000
V2      -378.4011U   1.8000     -681.1219U

 TOTAL POWER DISSIPATION:  681.1219U   WATTS
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(b)

Fig. 6: Power consumption (a) divide-by-2 and (b) divide-by-3 at an input frequency 8 GHz

The 2/3 prescaler in (Krishna *et al*, 2010) has the same maximum operating frequency of 8 GHz with a power consumption of 0.92 mW and 1.73 mW during divide-by-2 and divide-by-3 modes respectively. Table II compare the performance of the 2/3 prescaler reported in (Krishna *et al*, 2010) and this simulation.

Table 2: Comparison Study Of Performances

Design Parameter	Prescaler in [9]	This Work
Process (μm)	0.18	0.18
Supply Voltage (V)	1.8	1.8
Maximum Frequency (GHz)	8	8
Power Divide-by-2 (mW)	0.92	0.05
Power Divide-by-3 (mW)	1.73	0.68

The modified 2/3 prescaler circuit layout is designed in CEDEC 0.18-µm CMOS process. In Figure 7, the completed chip layout of the modified 2/3 prescaler is presented. The overall chip layout for this 2/3 prescaler is about (14.26 × 23.05) μm^2. The transistor size is optimized according to table 1 to meet the target for the lower power consumption and smoother output waveform.

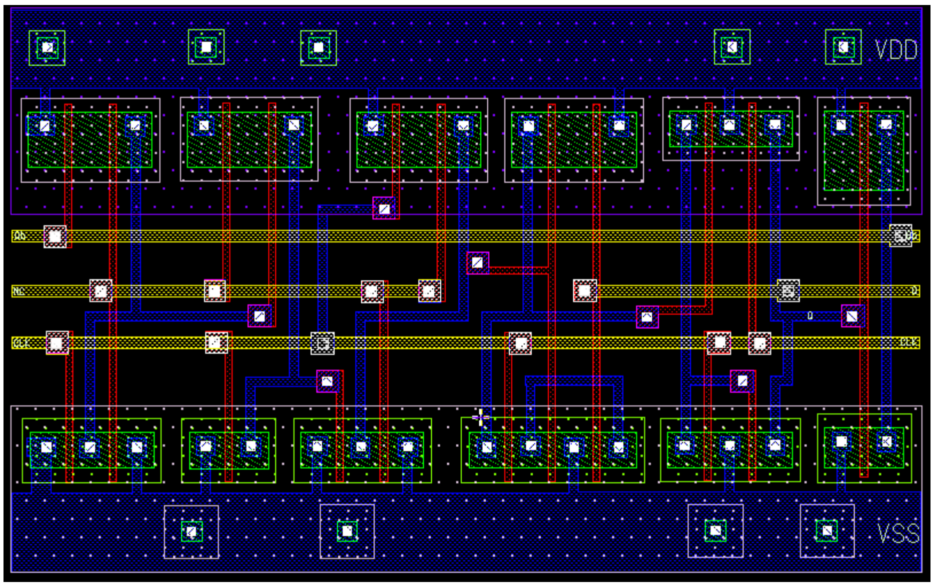

Fig. 7: A layout design of low power and wideband E-TSPC frequency divider

Conclusion:

The frequency divider is an important building block for high speed integrated circuits. After analysis of the 2/3 prescaler in (Krishna *et al*, 2010) a modified 8 GHz low power single-phase clock 2/3 prescaler is proposed. The modified 2/3 prescaler consumes a power of 0.05 mW and 0.68 mW at 8 GHz during divide-by-2 and divide-by-3 modes respectively and therefore, can save more than 50 % power in both modes. The output waveform is also smoother than the 2/3 prescaler in (Krishna *et al*, 2010) for divide-by-2 mode.

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