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Design and Optimization of 22nm NMOS Transistor

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Abstract: In this paper, we investigate the effects of four process parameters and two process noise parameters on the threshold voltage (V_{th}) of a 22nm NMOS transistor. We used TiO_2 as the high-k material to replace the SiO_2 dielectric. The NMOS transistor was simulated using the fabrication tool ATHENA and electrical characterization was simulated using ATLAS. Taguchi's experimental design strategy was implemented with the L9 orthogonal array for conducting 36 simulation runs. The simulators were used for computing V_{th} values for each row of the L9 array with 4 combinations of the 2 noise factors. The objective function for minimizing the variance in V_{th} is achieved using Taguchi's nominal-the-best signal-to-noise ratio (SNR). Analysis of Mean (ANOM) was used to determine the best settings for the process parameters whereas. Analysis of variance (ANOVA) was used to reduce the variability of V_{th}. The best settings were used for verification experiments and the results show V_{th} values with the least variance and that the mean value can be adjusted to 0.306V ±0.027 for the 22nm NMOS, which is well within the ITRS2011 specifications.

Key words: *22nm NMOS, Threshold voltage, orthogonal array, ANOVA, Taguchi Method*

INTRODUCTION

For a few decades, the scaling down on MOSFETs has been achieved according to Moore's law and also as dictated by the International Technology Road Map for Semiconductors (ITRS). A major problem is the use of a very thin oxide layer, below 3 nm which becomes a serious concern in terms of tunnelling current and oxide breakdown causing low device performance and high-gate leakage current (Shashank N *et al*., 2010).

Silicon dioxide (SiO_2) has been used as the gate dielectric material over decades, and the current device scaling trend requires the film thickness to be as thin as t_{ox} = 1.2nm. In this case, the tunnelling current will increase exponentially leading to increased power dissipation. The increase in power dissipation would be a critical problem because of the thermal management issues in submicron device structures. Moreover, the use of thin oxide films is not reliable (H.A. Elgomati *et al*., 2011).

To overcome this problem many new high-k dielectric materials have been recently introduced as a replacement for SiO_2 gate dielectric film. Many metal oxides (e.g., Al_2O_3, ZrO_2, HfO_2, TiO_2, etc.) and ferroelectric materials (e.g., PZT, BST, etc.) are being investigated as candidates to replace SiO_2 (Kyeongjae Cho, 2002). Furthermore, many researchers are implementing new CMOS technology using a combination of metal and high-k gates. However, this paper provides proof that the combination of polysilicon (poly-Si) and high-k gate material is still relevant and can still be used in NMOS transistors.

There have been many experiments demonstrating how poly-Si/high-k gate stacks address gate leakage requirements for low power applications. However, there are issues such as channel mobility and reliability degradations, as well as Fermi level pinning of the effective gate work function. These issues were found when poly-Si gate electrodes on high-k materials were created. Therefore, self-aligned silicide (SALICIDE) technology has been widely used to reduce the sheet resistance (R_s) of poly-Si gates (F.Salehuddin *et al*., 2010) The purpose of this paper is to provide a comprehensive design and optimization of high-k/poly-Si/SALICIDE as gate dielectric materials in a 22nm NMOS transistor.

The device design was developed using an industrial-based simulator which consist of both the fabrication process and device characterization methods. Optimization was executed using the Taguchi orthogonal array method. The Taguchi parameter design method is an important tool for robust design that involves an analysis of the most effective factors. The technique systematically chose certain combinations of variables while allowing analysis of their individual effects and also employs a generic signal to noise ratio (S/N) to quantify the present variation. These S/N ratios are meant to be used as a measure of the effect of noise factors on the performance characteristics (H.A. Elgomati *et al*., 2011)

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MATERIALS AND METHODS

The 22nm NMOS transistor was fabricated virtually. The substrate used for the experiment was p- type silicon, with a <100> orientation. It is then modified by growing an oxide layer at the top of the silicon bulk, using dry oxygen, at a temperature of 970ºC for 20 minutes. The p-well implantation process was done using this oxide layer as a mask. This was achieved using boron as the dopant with a dose of $3.75x10^{12}$ ions/cm^2 with implantation energy of 100KeV. The silicon wafer then underwent the annealing process at 900°C for 30 minutes in a Nitrogen environment, and this was followed by dry oxygen in order to ensure that boron atoms were spread properly in the wafer. The masking oxide was then etched. The next step was to produce a Shallow Trench Isolator (STI) of 130 Å thickness, (J W Sleight *et al*., 2006). In order to form the STI layer, the wafer was oxidized in dry oxygen for 25 minutes at 900ºC. Then, a 1000Å nitride layer was deposited on top of the oxide layer by applying the low pressure chemical vapour deposition process (LPCVD), followed by a photo resist deposit with a thickness of 1.0µm. Then, the photo resist and the nitride were etched using the reactive ion etching process (RIE) at the top of STI area. The trench depth of 3200 Å was achieved in a 25 second process. Thereafter, a sacrificial oxide layer was grown and then etched followed by a sacrificial nitride layer and so the trench was completed. Then the high-k material, TiO_2 (ε_{opt} = 5.4) was deposited to a thickness of 2nm (Davinder Rathee, *et al*., 2011; M.K. Bera and C.K. Maiti, 2006) and followed by etching to get the desired thickness and finally adjusted to produce a 22nm gate length. The next step was to implant boron difluoride (BF_2) into the N well active area in order to adjust the threshold voltage (V_{th}) value. The dosage for boron was $1.75x10^{11}$ ions/cm^2. Poly-Si was then deposited on the top of the bulk with a thickness of 7nm and etched accordingly to produce the gate contact point as desired (L. Pereira *et al*., 2008). Halo implantation then took place in order to get an optimum performance for the NMOS device. Indium with a dose of $14.75x10^{12}$ ions/cm^2, was implanted. The dosage was varied in order to get the optimum value. A Nitride layer will then be deposited on top of the poly-Si gate and immediately etched to expose the top surface of the silicon layer. Then spacers were formed at each of the poly-Si sides, the source and drain regions respectively. A silicon nitride layer of 0.0320µm was added. Then it was etched away at the same thickness. Due to the nature of the substrate surface at the gate, side wall spacers were created of 0.0867 µm thickness at the gate sides. Side wall spacers are used as a mask for source and drain implantation (J. Laeng *et al*., 2006). The source-drain implantations began with an arsenic dose of $5.4x10^{13}$ions/cm^2, and were followed by a phosphorous dose of $1.5x10^{12}$ions/cm^2 to ensure the smooth current flow in the device. The next process was to diffuse the dopants at 900°C for 10 minutes. Thereafter, the process continued by depositing an oxide mask on top of polysilicon gate in order to form a silicide structure. A cobalt silicide layer of 0.0590 µm was then deposited on top of the substrate and was annealed by the rapid thermal annealing process in a nitrogen environment. Afterwards, the residual area of cobalt was etched away. In the next step, the structure is annealed at a temperature of 900ºC in a nitrogen environment of 1 a.t.m. This particular annealing process was to deepen the spread of cobalt atoms into the polysilicon. The next process was the development of a 0.5 µm Borophosphosilicate Glass (BPSG) layer (Sarcona G.T. *et al*., 1999). This layer is acts as a pre metal dielectric (PMD). PMD contains silicon dioxide that is doped with boron and phosphorus. After the Borophosphosilicate Glass (BPSG) deposit, the wafer undergoes 15 minutes annealing at a temperature of 950°C (Sarcona G.T. *et al*., 1999). The next process was the compensation implantations using phosphorous, with a dose of $1.39x10^{13}$ions/cm^2 (Hashim, U., 2009). Then followed the deposit of an aluminium contact. The wafer was then annealed for 20 seconds at 850ºC. Then an aluminium layer was deposited on top of the structure and then etched accordingly to form the metal contact for source and drain. At this stage the design of the transistor is complete. Then, the transistor underwent electrical characteristic measurement in order to find the threshold voltage (V_{th}) by referring to the ITRS 2011 table (ITRS, 2011). Figure 1 & Figure 2 show the completed NMOS device and its doping profile. Figure 3 shows the complete process flow in developing the 22 nm NMOS transistor.

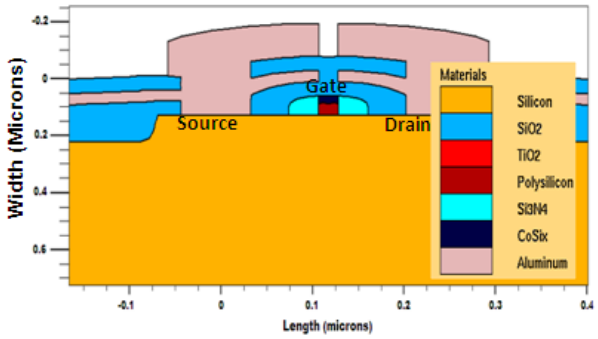

Fig. 1: Completed NMOS transistor

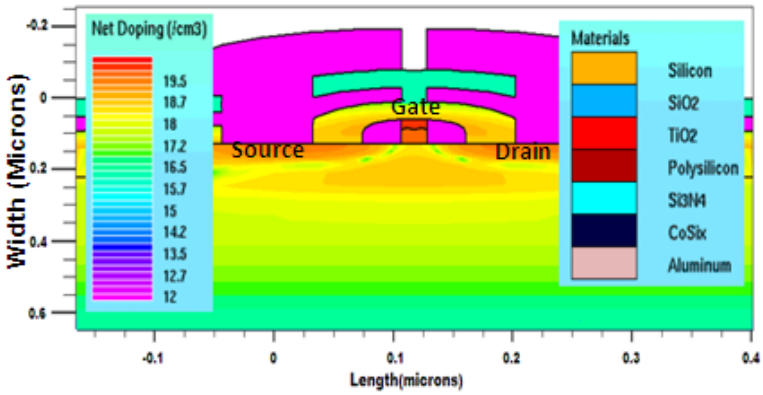

Fig. 2: The doping profile of the NMOS transistor

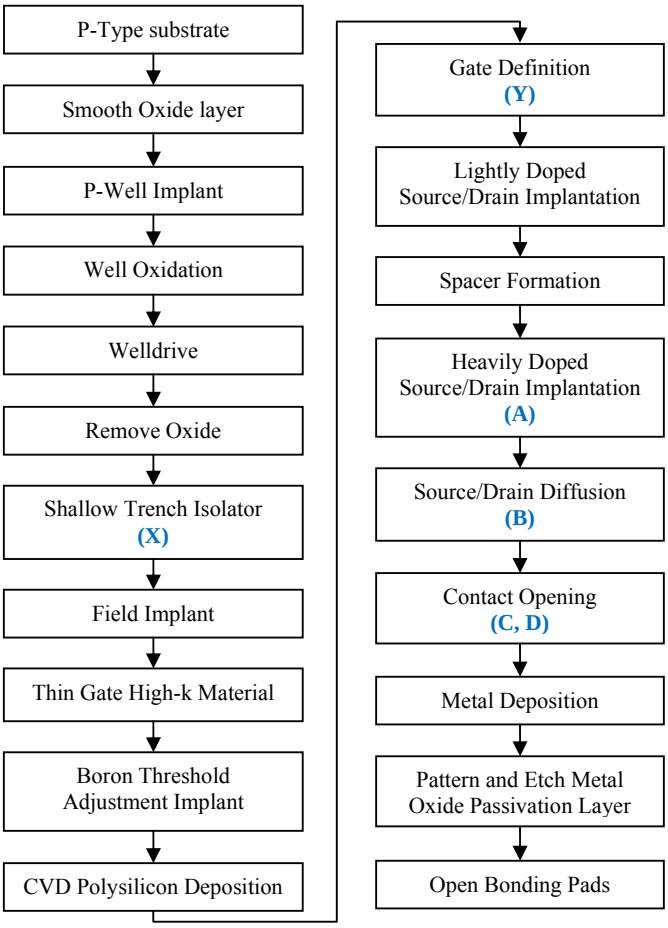

Fig. 3: Complete fabrication process flow. The selection of control and noise factors can then be referred to this figure.

A. Taguchi Orthogonal L9 Array Method:

Four control factors and two noise factors with three levels were chosen to form the L9 Taguchi orthogonal array. The control factors are Halo implantation, Source/Drain (S/D) Implantation, Compensation Implantation and Silicide Anneal Temperature and the noise factors are Sacrificial Oxide Layer and Cobalt Annealing Temperature. The values of the process parameters and noise factors at the different levels are listed in Table 1 and Table 2 respectively.

Table 1: Process Parameters and their Levels

	Process Parameter	Unit	Level 1	Level 2	Level 3
A	Halo Implant	atom/cm^3	14.25e^{12}	14.50e^{12}	14.75e^{12}
B	S/D Implant	atom/cm^3	5.4e^{13}	5.5e^{13}	5.6e^{13}
C	Compensation Implant	atom/cm^3	1.0e^{13}	1.2e^{13}	1.4e^{13}
D	Silicide Anneal Temp	^{o}C	900	910	920

Table 2: Noise Factors and their Levels

Symbol	Noise Factor	Unit	Level 1	Level 2
X	Sacrificial Oxide layer	°C	900 (X1)	902 (X2)
Y	Cobalt annealing	°C	900 (Y1)	898 (Y2)

In this research, an L9 orthogonal array which has 9 experiments was used and the experimental layout for the process parameters is shown in Table 3.

Table 3: Experimental Layout Using L9 Orthogonal Array

	Control Factors			
Expt. No.	A	B	C	D
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

RESULT AND DISCUSSION

By using the combinations of the Taguchi Orthogonal Array Method, the results of the device's threshold voltage (V_{th}) were analyzed and processed to get the optimal design. The optimized results from the Taguchi Method were then simulated again in order to verify the predicted optimal design.

A. Analysis for 22nm NMOS Device:

There were nine experiments for the NMOS device and these were performed using the design parameter combinations in the orthogonal array table. Four specimens were simulated for each of the noise parameter combinations. The completed results for V_{th} data are shown in Table 4.

Table 4: V_{th} Values for NMOS Device

Exp.	Threshold Voltage (Volts)			
No	X1Y1	X1Y2	X2Y1	X2Y2
1	0.333424	0.376840	0.362164	0.378377
2	0.298050	0.298133	0.298730	0.298740
3	0.248467	0.248213	0.249666	0.249680
4	0.334987	0.335230	0.332673	0.332710
5	0.289860	0.289960	0.288936	0.288951
6	0.371810	0.372110	0.369778	0.369812
7	0.302850	0.302930	0.303047	0.303058
8	0.397696	0.397891	0.398183	0.398200
9	0.331443	0.337180	0.337553	0.337593

After implementing the nine experiments of the L9 array, the next step was to determine the significant control factors. A control factor is the factor that gives more effectiveness to the device characteristics. Therefore the Signal-to-noise (S/N) ratio was used to find out the optimal process parameters in the experiment and analyze the experimental data. The S/N ratio for each level of the process parameters is computed on the basis of the S/N analysis. Regardless of the category of the performance characteristic, the larger the S/N ratio, the better is the performance characteristics. Therefore, the optimal level of the process parameters is the level with the highest S/N ratio (Phadke, Madhav S., 1998).

In this research, the threshold voltage of the 22 nm devices belongs to the nominal-the-best quality characteristics. The S/N ratio is selected to get a threshold voltage value that can be as close as possible to the given target value (0.306V), which is also known as the nominal value from ITRS (G.P.Syros, 2003). The S/N Ratio (Nominal-the-best), η can be expressed as (Phadke and Madhav S., 1998):

$$\eta = 10\mathrm{Log}_{10}\left[\frac{\mu^2}{\sigma^2}\right] \quad (1)$$

Where:

$$\mu = \frac{Y_i + ... + Y_n}{n} \quad (2)$$

$$\sigma^2 = \frac{\sum_{i=1}^{n}(Y_i - \mu)^2}{n-1} \quad (3)$$

While n is the number of tests and Y_i the experimental value of the threshold voltage, μ is the mean and σ is the variance. In nominal-the-best S/N ratio, there are two types of factors; the dominant and the adjustment factor. By applying equations (1)-(3), the η for each device was calculated and given in Table 5 (Joseph and VR, 2007).

Table 5: Mean, Variance and S/N Ratios for NMOS Device

Exp. No.	Mean	Variance	S/N Ratio (Mean)	S/N Ratio (Nominal-the-Best)
1	0.363	4.34E-04	-8.81	24.81
2	0.298	1.39E-07	-10.50	58.06
3	0.249	6.03E-07	-12.08	50.12
4	0.334	1.96E-06	-9.53	47.56
5	0.289	3.13E-07	-10.77	54.27
6	0.371	1.58E-06	-8.62	49.40
7	0.303	9.89E-09	-10.37	69.68
8	0.398	5.92E-08	-8.00	64.28
9	0.336	9.03E-06	-9.47	40.97

By referring to Table 5, we can see that the S/N Ratios for rows 2, 7, 8 have values of 58.06 dB, 69.68 dB and 64.24 dB respectively. This result implies that the process parameter combinations give the best resistance to the response characteristic. The effect of each process parameter on the S/N ratio at different levels can be distinguished because the experimental design is orthogonal. The S/N ratio for each level of the process parameters and the total mean of the S/N ratio for the experiments are summarized in Table 6.

Table 6: S/N Ratio for the Threshold Voltage

Symbol	Process Parameter	S/N Ratio (Nominal-the-Best)			Total Mean S/N	Max Min
		Level 1	Level 2	Level 3		
A	Halo Implantation	44.33	50.41	58.31	51.02	13.98
B	S/D Implantation	47.35	58.87	46.83		12.04
C	Compensation implantation	46.16	48.86	58.02		11.86
D	Silicide Anneal Temperature	40.02	59.05	53.98		19.03

Figure 3 shows the factor effect plotted for the S/N Ratio. The dashed line represents the values of the overall- mean of the S/N ratio and Mean respectively. Theoretically, the larger value of the S/N ratio means it's the better quality characteristic for the threshold voltage.

B. Analysis of Variance (ANOVA):

The priority of the process parameters with respect to the V_{th} was investigated to determine more accurately the optimum combinations of the process parameters. The result of ANOVA for the NMOS device is presented in Table 7. The percentage factor effect on the S/N ratio indicates the priority of a factor (process parameter) to reduce variation. The factor with higher percent contribution will have a greater influence on the stability of V_{th} with respect to the noise parameters.

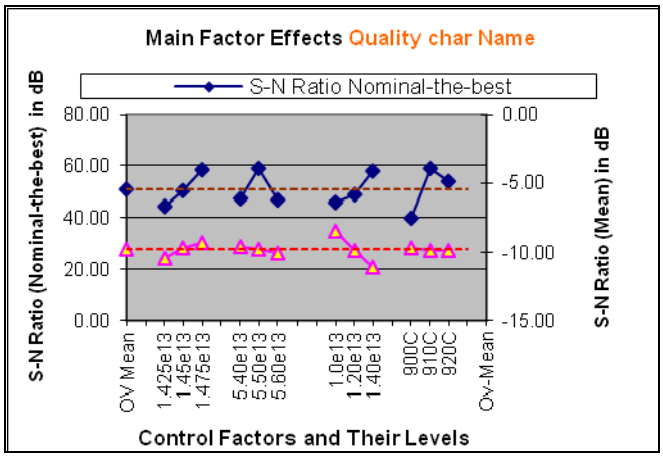

Fig. 3: S/N graph for threshold voltage in NMOS Device

Table 7: Result of ANOVA for PMOS Device

Symbol	Process Parameter	Degree of Freedom	Sum of Square	Mean square	Factor Effect on S/N Ratio (%)	Factor Effect on Mean (%)
A	Halo Implantation	2	295	147	21	17.26
B	S/D Implantation	2	278	139	20	2.82
C	Compensation implantation	2	232	116	17	79.47
D	Silicide Anneal Temperature	2	583	291	42	0.45

The results obviously show that Compensation implantation (79.47%) has the most dominant impact on the resulting threshold voltage in an NMOS device, whereas Halo implantation was the second ranking factor (17.26%). The effects on the S/N ratio for S/D Implantation and silicide annealing temperature are much lower, being (2.82%) and (0.45%) respectively. The optimal factors for the NMOS device suggested by the Taguchi method are shown in Table 8.

C. Confirmation of Optimum Factor:

With all this information, it can be clearly said that for the optimal design, either Compensation implantation or oxide thickness can be defined as an adjustment factor because it has a small effect on the S/N Ratio (variance) and large effect on the mean. In the NMOS device, the value of Compensation implantation or oxide thickness can be adjusted. The adjustment value has to be done to get the threshold voltage as close as possible to the nominal or target value. The Taguchi method suggested the best setting of the process parameters for the device and it shown in Table 8.

Table 8: Best Setting of the Process Parameters

Symbol	Process Parameter	Unit	Level	Best Value
A	Halo Implantation	atom/cm^3	3	1.475e13
B	S/D Implantation	atom/cm^3	1	5.4e13
C	Compensation implantation	atom/cm^3	-	Sweep (1.2e13 to 1.4e13)
D	Silicide Anneal Temperature	^{o}C	2	910 °C

Using the parameters in Table 8, the final experiment was performed to verify the accuracy of the Taguchi Method prediction. The value of Compensation Implantation was adjusted within 1.2 x 10^{13} to 1.4 x 10^{13} until the value of threshold voltage (V_{th}) was closer to 0.306 V as required in ITRS 2011 (ITRS, 2011). By doing the value sweep, the Compensation Implantation doping for the optimum solution in fabricating a 22 nm NMOS transistor is 1.39 x 10^{13} atom/cm^3. Then the last step was to get the best value of the V_{th} by adding noise factors to the experiment. Table 9 show the end results of the experiment when adding the noise factor.

From the above results for the NMOS device, the mean is 0.3054 V and the S/N ratio 69.7 dB. The values are well within the target set by ITRS (ITRS, 2011). Lastly, from the optimized result, the device characteristic is shown in Figure 4 and Figure 5 where the plot of I_{drain} versus V_{drain} and I_{drain} versus V_{gate} is portrayed respectively.

Table 9: Results of Further Runs of Confirmation, Experiment with Added Noises

V_{th} (n1,n1)	V_{th} (n1,n2)	V_{th} (n2,n1)	V_{th} (n2,n2)	SNR (Mean)	SNR (Nominal-the-best)
0.30521	0.30523	0.30564	0.30568	0.3054	69.7

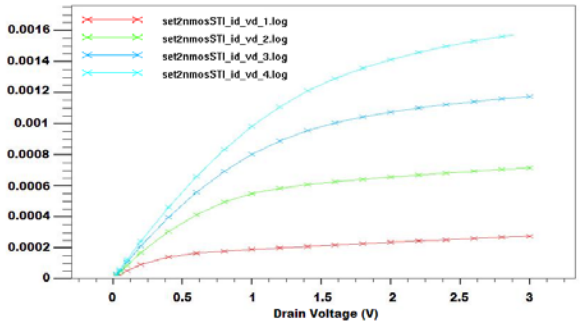

Fig. 4: I_D versus V_D Relationships

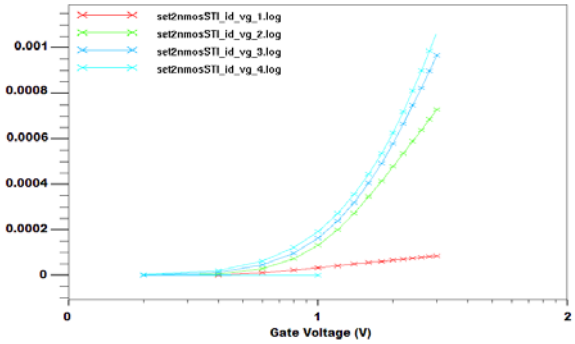

Fig. 5: I_D versus V_G Relationships

Conclusion:

In conclusion, the optimum solution in achieving the desired transistor was successfully predicted by using the Taguchi Method. Threshold voltage (V_{th}) is the main factor in determining whether the device is working or not. Leakage current was kept as low as possible to increase the speed of the device and minimising the time for the transistor to function for a transistor to turn on. In this research, the Compensation implant dose has been identified as the prime adjustment parameter for the threshold voltage; it has the strongest effect on the leakage current for this device. The best process parameter value that gives the best V_{th} for Halo Implantation, S/D Implantation, Compensation Implantation and Silicide Anneal Temperature are 1.475 x 10^{13} atom/cm^3, 5.4 x 10^{13} atom/cm^3 and 1.39 x 10^{13} atom/cm^3 and 910 °C respectively. While the noise parameter value for Sacrificial Oxide Layer and Cobalt annealing temperature are 902 °C and 898 °C respectively. Therefore it has been proven that by using a combination of high-k/poly-Si/SILICIDE gate, a working 22nm NMOS transistor can be produced and the V_{th} value is well within the ITRS 2011 requirements of 0.306 V. To the author's knowledge, this is the first time that such work has been reported in the literature.

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REFERENCES

Davinder Rathee, Sandeep K. Arya and Mukesh Kumar, 2011. Preparation and Characterization of TiO2 and SiO2 Thin Films. *World Journal of Nano Science and Engineering*, pp: 84-88.

Salehuddin, F., I. Ahmad, F.A. Hamid and A. Zaharim, 2010. Characterization and Optimizations of Silicide Thickness in 45nm pMOS Device, ICEDSA.

Syros, G.P., 2003. Die casting process optimization using Taguchi Methods. Journal of Materials Processing Technology, 135: 68-74.

Elgomati, H.A., B.Y. Majlis, I. Ahmad, F. Salehuddin, F.A. Hamid, A. Zaharim, T. Ziad Mohamad and P.R.Apte, 2011. Investigation Of The Effect for 32nm PMOS Transistor and Optimizing Using Taguchi Method. Asian Journal of Applied Sciences.

Elgomati, H.A., B.Y. Majlis, I. Ahmad, F. Salehuddin, F.A. Hamid, A. Zaharim and P.R. Apte, 2011. Application of Taguchi Method in The Optimization of Process Variation for 32nm CMOS Technology. Australian Journal of Basic and Applied Sciences, 5(7): 346-355.

Hashim, U., 2009. "Statistical Design of Ultra-Thin SiO2 for Nanodevices", Sains Malaysiana, 38(4): 553-557.

ITRS, 2011. *www.ITRS2011.net*

Laeng, J., Zahid A. Khan and S.Y. Khu, 2006. Optimizing Flexible Behaviour of Bow Prototype Using Taguchi Approach. Journal of Applied Sciences, 6(3): 622-630.

Joseph, V.R., 2007. Taguchi's Approach to Robust Parameter Design: A new Perspective. IEEE Transactions.

Sleight, J.W., I. Lauer, O. Dokumaci, D.M. Fried, D. Guo, B. Haran, S. Narasimha, C. Sheraw, D. Singh, M. Steigerwalt, X. Wang, P. Oldiges, D. Sadana, C.Y. Sung, W. Haensch, M. Khare, 2006. Challenges and Opportunities for High Performance 32nm CMOS Technology. IEDM Tech Digital.

Kyeongjae Cho, 2002. First-principles Modeling of High-k Gate Dielectric Materials. Computational Materials Science, 23: 43–47.

Pereira, L., P. Barquinha, E. Fortunato and R. Martins, 2008. Low Temperature High K Dielectric on Poly-Si Tfts. Journal of Non-Crystalline Solids., 354: 2534-2537.

Bera, M.K. and C.K. Maiti, 2006. Electrical Properties of Sio2/Tio2 High-K Gate Dielectric Stack. Materials Science in Semiconductor Processing, pp: 909-917.

Phadke, Madhav S., 1998. Quality Engineering Using Robust Design. Pearson Education, Inc. and Dorling Kindersley Publishing, Inc.

Sarcona, G.T., M. Stewart, and M.K Hatalis, 1999. Polysilicon Thin Film Transistor Using Self_Aligned Cobalt and Nickel Silicide Source and Drain Contacts. IEEE Electron Device Letters, vol.20.

Shashank, N., S. Basak and R.K. Nahar, 2010. Design and Simulation of Nano Scale High-k Based MOSFETs with Ploy Silicon and Metal Gate Electrodes. International Journal of Advancements in Technology, pp: 252-261.