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High Speed Low Power 1D DTCWT Accelerator for 3D DTCWT Architecture Design for Plant Pheno typing Video Encoding

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Abstract

Video data acquired for plant phenotyping applications need to be compressed for data storage and data transmission. Video data comprising multiple frames are decomposed into wavelet sub bands using 3D Discrete Wavelet Transform (DWT). Computation complexity of 3D DWT for hardware implementation is addressed by use of lifting scheme. With limitations of DWT in terms of shift variance and directional selectivity, Dual Tree Complex Wavelet Transform (DTCWT) is replacing DWT for image compression and image processing applications. Computation complexities of DTCWT processing need to be addressed with use of improved methods for data processing. In this work, novel algorithm for 1D DTCWT computation is designed with reduced hardware complexity that accelerates data computation and hence is used in design of 3D DTCWT computation. The 3D DTCWT architecture design reduces arithmetic unit and memory unit for 3D DWT computation. VLSI implementation of the proposed architecture achieves 38% improvement in power and operates at a maximum frequency of 328 MHz and is suitable for real time video compression. The proposed algorithm is suitable for real time plant phenotyping compression applications.

Key words: Image Compression, Hardware Accelerators, 3D Data Processing, FPGA, Low Power, Plant Phenotyping.

INTRODUCTION

Plant phenotyping is identification of plant appearance and performance with genotype changes and environmental changes the plant is subjected to. Plant phenotyping provides information on using water, land and fertilizer based on environmental changes and climate conditions. R. T. Furbank and M. Tester (2011) proposed Phenomics - technologies to relieve the phenotyping bottleneck. Image based phenotyping techniques have gained importance as they provide adequate information for high end commercial applications, low cost approaches, with high throughput phenotyping of plant structure and function. Plant phenotyping involves 3D images that are obtained from 2D image data set, plant also has growth pattern which is time dependent. Compression of 3D data sets imposes challenges in terms of computational time and compression loss. Li Hui Fang, Xu HouJie and Miao Guo Feng (2011) have proposed an Images Compression Using Dual Tree Complex. Use of transformational techniques such as wavelets for compression suffers from time shift loss and directionality. As 3D data with time information are directional sensitive, dual tree wavelets are suitable for 3D image compression. Nowadays, most of the applications require real-time 3D DTCWT engines with large computing potentiality for which a fast and dedicated very-large-scale integration (VLSI) architecture appears to be the best possible solution. While it ensures high resource utilization, that too in cost effective platforms like field programmable gate array (FPGA) and ASIC, designing such architecture does offer some flexibilities like speeding up the computation by adopting more pipelined structures and parallel processing, possibilities of reduced memory consumptions through better task scheduling or low-power and portability features. The lifting based architecture has advantages over traditional architectures in terms of number of multipliers and adders required for data path operation. Literature studies report on various schemes for optimizing hardware utilization on VLSI platform for DWT implementation, very few studies have been reported on DTCWT implementation. This is the first paper that discusses suitable architecture design for DTCWT. A brief review on DWT hardware implementation is presented in this work. 3D discrete wavelet transforms (3D-DWT) have been proposed by various researchers. Karlsson and Vetterli (1990) first advocated the use of a separable 3D-DWT for video compression. Taubman and Zakhor (1994) proposed an approach based on spatially aligning video frames on a high-resolution grid, prior to the application of

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a separable 3D-DWT. More generally, the spatial alignment of video frames prior to separable transformation may be achieved through arbitrary frame warping operations. Invertibility of the transform, however, depends upon that of the frame warping operations. A second class of approaches can be described as local block warping or block displacement methods, as proposed by Ohm and Woods and Choi (1994). In this class of approaches, video frames are divided into blocks, where each block undergoes rigid motion (usually translation). Again, the 3D-DWT is essentially applied in a separable fashion to the displaced blocks, but the effects of expansion and contraction in the motion field are observed in the appearance of "disconnected pixels" between the blocks. Malay Ranjan Tripathy, Kapil Sachdeva, and Rachid Talhi (2009) have proposed an improved version of lifting based 3D Discrete Wavelet Transform (DWT) VLSI architecture which uses bi-orthogonal 9/7 filter processing. This is implemented in FPGA by using VHDL codes. Aroutchelvame, S.M. and K. Raahemifar (2005) where architecture performs both forward and inverse lifting-based discrete wavelet transform. The proposed architecture reduces the hardware requirement by exploiting the redundancy in the arithmetic operation involved in DWT computation. Anirban Das, Anindya Hazra, and Swapna Banerjee (2010) have proposed the architecture of the lifting based running 3-D discrete wavelet transform (DWT), which is a powerful image and video compression algorithm. Most of the work reported in literature based on 3D DWT architectures on FPGA platforms, and there are very few literature studies on 3D DTCWT implementation. In this paper, we propose a hardware efficient, low power 3D DTCWT architecture based and the proposed design is implemented in VLSI platform. Section 2 discusses 3D DTCWT algorithm design. Section 3 discusses the proposed 3D DTCWT architecture design. Section 4 discusses the FPGA implementation and Section 5 concludes the results obtained.

D-DTCWT algorithm

Computation of DTCWT is as similar to DWT computation with two major differences: one is the selection filter coefficients and second is the complex structure. DTCWT is based on Kingsbury (1998) filters and in this work 10-tap filter is selected. The DTCWT structure comprises of real (F_h = {H_{0a}, H_{0b}}) and imaginary (F_g = {H_{1a}, H_{1b}}) filter banks that compute the real and imaginary wavelet coefficients or also termed as dual tree complex wavelet coefficients by I. W. Selesnick and R.G. Baraniuk, (2005) that satisfy the conditions $H_{1x} = H_{0x}(n-1)$. The DTCWT filter outputs that are generated from four filters are denoted as approximation and detail coefficients {C, D} and is represented as in Eq. (1).

$$C^{j}_{a/b}(Z_1, Z_2) = (2^{J}\downarrow)\left((A^{j}_{a}(Z_1) \pm j(A^{j}_{b}(Z_1))(A^{j}_{a}(Z_2) + j(A^{j}_{b}(Z_2))\, S(Z_1, Z_2)\right) \quad \textbf{(1a)}$$

$$D^{j}_{1a/b}(Z_1, Z_2) = (2^{J}\downarrow)\left((A^{j}_{a}(Z_1) \pm j(A^{j}_{b}(Z_1))(B^{j}_{a}(Z_2) + j(B^{j}_{b}(Z_2))\, S(Z_1, Z_2)\right) \quad \textbf{(1b)}$$

$$D^{j}_{2a/b}(Z_1, Z_2) = (2^{J}\downarrow)\left((B^{j}_{a}(Z_1) \pm j(B^{j}_{b}(Z_1))(A^{j}_{a}(Z_2) + j(A^{j}_{b}(Z_2))\, S(Z_1, Z_2)\right) \quad \textbf{(1c)}$$

$$D^{j}_{3a/b}(Z_1, Z_2) = (2^{J}\downarrow)\left((B^{j}_{a}(Z_1) \pm j(B^{j}_{b}(Z_1))(B^{j}_{a}(Z_2) + j(B^{j}_{b}(Z_2))\, S(Z_1, Z_2)\right) \quad \textbf{(1d)}$$

The input signal is represented as S, which is decomposed into C and D coefficients. The terms a and b represents the real and imaginary terms respectively. The terms 1, 2, 3 represent the directional information of input image extracted by complex wavelets in $\pm 15^0$, $\pm 75^0$, $\pm 45^0$. Level-1 DTCWT computation for input image is carried out as shown in Figure 1. The four filters in the first stage process data along the rows, the second stage filter processes the data along the column. The last stage of data processing computes the sum and difference of wavelet coefficients to generate the eight sub bands of real and imaginary components. 2D DTCWT computation requires 20 filters for level-1 computation.

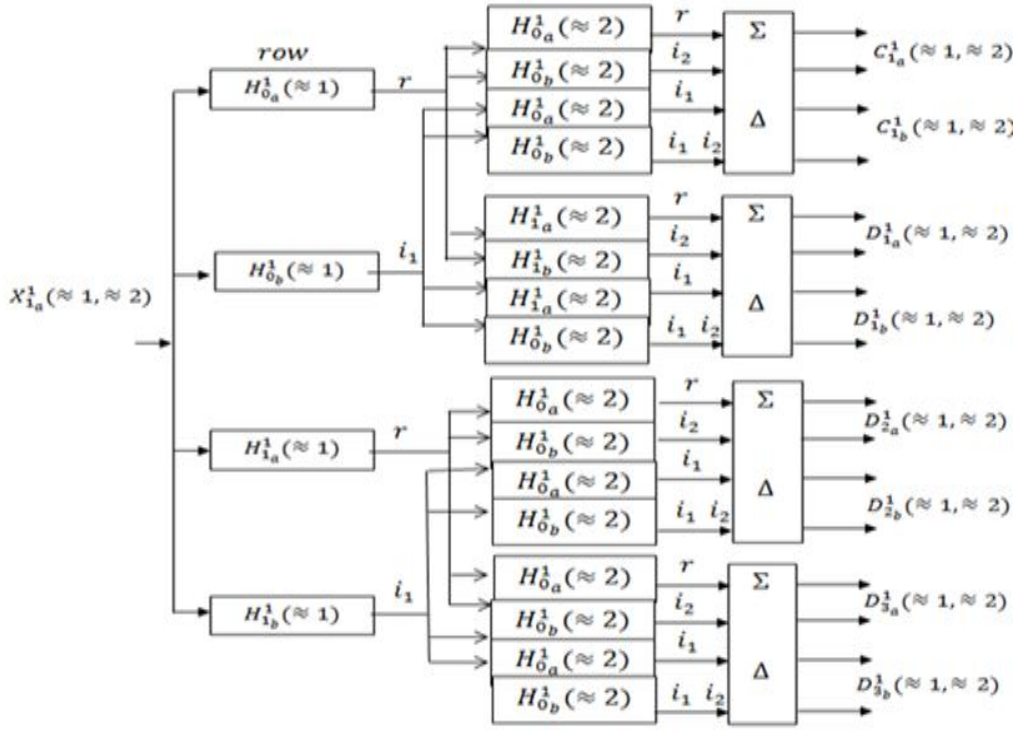

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Figure 1 Single Stage Dual Trees CWT

Table 1 shows the filter coefficients for the first stage decomposition the coefficients for higher stages of decomposition are presented by Jingyu Yang, Yao Wang, Wenli Xu, and Qionghai Dai, (2008).

Table 1 DTCWT filters for level-1

Tree a		Tree b	
H_{0a}	H_{1a}	H_{0b}	H_{1b}
0	0	0.01122679	0
-0.08838834	-0.01122679	0.01122679	0
0.08838834	0.01122679	-0.08838834	-0.08838834
0.69587998	0.08838834	0.08838834	-0.08838834
0.69587998	0.08838834	0.69587998	0.69587998
0.08838834	-0.69587998	0.69587998	-0.69587998
-0.08838834	0.69587998	0.08838834	0.08838834
0.01122679	-0.08838834	-0.08838834	0.08838834
0.01122679	-0.08838834	0	0.01122679
0	0	0	-0.01122679

Computation complexity of DTCWT

Computing 8 sub bands of real and imaginary components of 2D DTCWT requires two stages of data processing. If the input image is of size N x N, the first stage processes N rows by four filters and each row comprises of N elements. Computing one output at every filter requires 10 multiplications and 9 additions. Hence the first stage requires 40 multipliers and 36 adders for computing one output. As there are N elements in every row, the total number of multiplications and adders are 40N and 36N respectively. Considering N rows the number of multiplication and adders are $40N^2$ and $36N^2$ respectively. The second stage consists of 16 filters and hence the number of multipliers and adders required are $160N^2$ and $144N^2$ respectively. Computing level-1 2D DTCWT computation requires $200N^2$ and $180N^2$ multipliers and adders respectively. Computing 3D DTCWT requires $40N^3/4$ and $36N^3/4$ multipliers and adders for one band. As there are 8 sub bands the total number of multipliers and adders required are 320 $N^3/4$ and 288 $N^3/4$ respectively. With large number of arithmetic unit and memory unit required for DTCWT computation, there is a need for suitable architecture design that can optimize area, timing and power requirements for DTCWT implementation on VLSI platform. In this work, modified and improved architectures for DTCWT computation are designed and implemented on FPGA platform.

DTCWT Architecture

In order to reduce computation complexity in hardware implementation of DTCWT structure, similarities between filter coefficients are considered. Considering symmetry and common filter coefficients the reduced filter structure for stage 1 {h0, h1, h2, h3} and stage 2 {g0, g1, g2, g3, g4, g5, g6} are presented in Table 2.

Table 2 Reduced filter coefficients with common terms

Tap	Stage 1				Stage 2			
	LP	HP	LP	HP	LP	HP	LP	HP
0	h_0	h_0	h_3	h_0	g_0	g_1	g_1	$-g_0$
1	$-h_1$	$-h_3$	h_3	h_0	g_1	g_1	g_1	g_1
2	h_1	h_3	$-h_1$	$-h_1$	$-g_2$	$-g_6$	$-g_6$	g_2
3	h_2	h_1	h_1	$-h_1$	g_3	g_1	g_1	g_3
4	h_2	h_1	h_2	h_2	g_4	g_5	g_5	$-g_4$
5	h_1	$-h_2$	h_2	$-h_2$	g_5	$-g_4$	g_4	g_5
6	$-h_1$	h_2	h_1	h_1	g_1	g_3	g_3	g_1
7	h_3	$-h_1$	$-h_1$	h_1	$-g_6$	g_2	$-g_2$	$-g_6$
8	h_3	$-h_1$	h_0	h_3	g_1	g_1	g_1	g_1
9	h_0	h_0	h_0	-h3	g_1	$-g_0$	g_0	g_1

The responses of four filters denoted as $\{Y_{LR}, Y_{HR}, Y_{LI}, Y_{HI}\}$ for row processing are represented as in Eq. (4), the responses are obtained by considering the similarities in filter coefficients, and xi represents the input samples. From the output terms $\{Y_{LR}, Y_{HR}\}$ there are common terms such as $\{(x_{i+2} - x_{i+1}), (x_{i+3} + x_{i+4}), (x_{i+5} - x_{i+6})$ & $(x_{i+7} + x_{i+8})\}$, thus the number of arithmetic operations can be reduced. The reduced filter structure for computation of $\{Y_{LR}, Y_{HR}\}$ is shown in Figure 2.

$$\boldsymbol{Y_{LR} = h_1 (X_{i+2} - X_{i+1}) + h_2 (X_{i+3} + X_{i+4}) + h_1 (X_{i+5} - X_{i+6}) + h_3 (X_{i+7} + X_{i+8})} \quad \textbf{(4)}$$

$$\boldsymbol{Y_{HR} = h_3 (X_{i+2} - X_{i+1}) + h_1 (X_{i+3} + X_{i+4}) + h_2 (X_{i+5} - X_{i+6}) - h_1 (X_{i+7} + X_{i+8})} \quad \textbf{(5)}$$

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$$Y_{LI} = h_3 (X_i + X_{i+1}) + h_1 (X_{i+3} - X_{i+2}) + h_2 (X_{i+4} + X_{i+5}) + h_1 (X_{i+6} - X_{i+7}) \quad (6)$$

$$Y_{HI} = -h_1 (X_{i+2} + X_{i+3}) + h_2 (X_{i+5} - X_{i+4}) + h_1 (X_{i+6} + X_{i+7}) + h_3 (X_{i+8} - X_{i+9}) \quad (7)$$

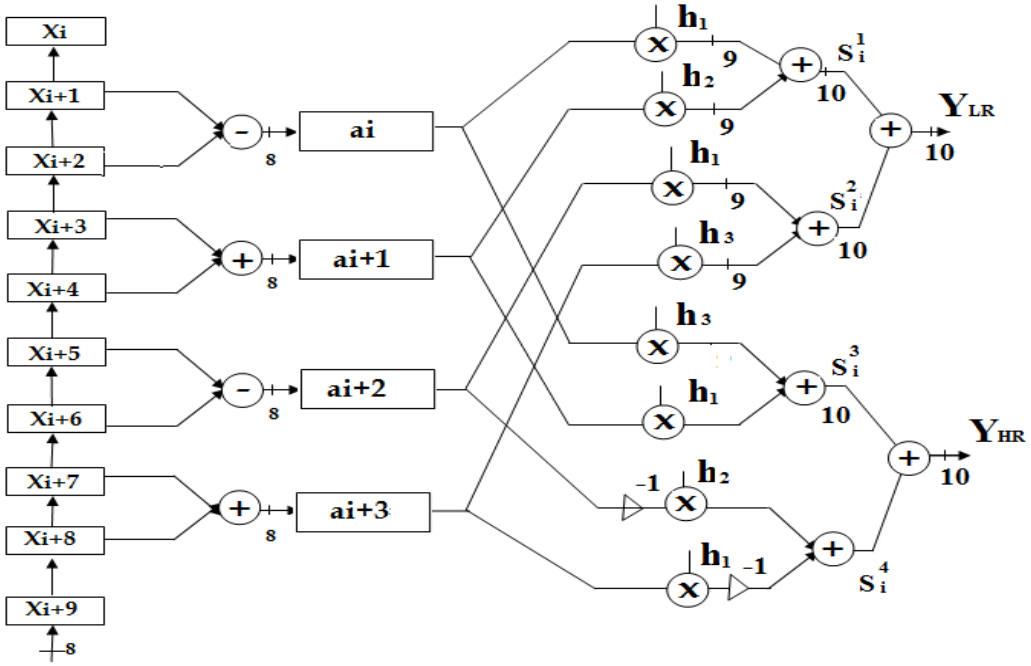

Figure 2 Reordered filter architecture (Real)

1D DTCWT computation is carried out by first loading 10 input data vectors into the input register that requires 10T clock cycles. At the start of 11th clock cycle the content of input registers are added and the intermediate data is stored in the second stage register array denoted as {a}. At the start of 12th clock cycle the content of intermediate registers are multiplied by the filter coefficients {h}. The last two stage of addition requires additional two clock cycles for computing the Y_{LR} and Y_{HR} outputs. Hence for computing one output of two filters it requires 14 clock cycles. Consecutive output computation requires 5 clock cycles, as one clock cycle is required for data loading and four clocks is required for arithmetic operations. The latency is found to be 14 clock cycles and throughput is found to be 5 clock cycles. The architecture shown in Figure 2 is designed with pipeline approach with four stages of pipeline. The pipeline stage has a latency of 14T and throughput of 1T. The pipeline architecture requires 10 input registers, 14 intermediate registers and 2 output registers as there are 4 adders, 8 multipliers and four adders in the intermediate stages. Similarly for computation of {Y_{LI}, Y_{HI}} output terms (shown in Eq. (6) and Eq. (7)) in the stage 1 filter, the common terms in filter coefficients are reorganized to minimize the number of arithmetic operations is shown in Figure 3.

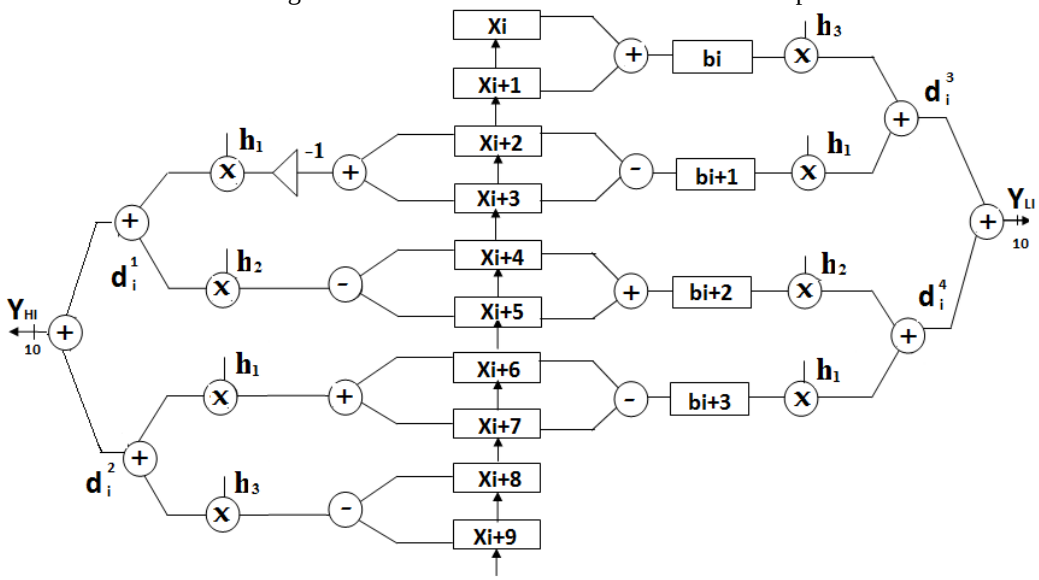

Figure 2 Reordered filter architecture (Imaginary)

Pipelined DTCWT architecture

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Considering Eq. (4) and Eq. (5) the Y_{LR} and Y_{HR} term comprises of four terms which can be represented as in Eq. (8). These addition operations are carried out in the first stage. The first two terms require h1 and h2 coefficients and next two terms require h1 and h3 coefficients for multiplication. These operations are computed in two stages.

$$\mathbf{a_{i+n} = X_{i+1+n} + X_{i+2+n} \quad n = 0, 1, 2, 3} \tag{8}$$

During the second stage the terms S_i^1 and S_i^3 (shown in Eq. (9) and Eq. (11)) are computed, and during third stage the terms S_i^2 and S_i^4 (shown in Eq. (10) and Eq. (12)) are computed simultaneously.

$$\mathbf{S_i^1 = h_1\ a_{i+n} + h_2\ a_{i+n+1}} \tag{9}$$

$$\mathbf{S_i^2 = h_1\ a_{i+n} + h_3\ a_{i+n+1}} \tag{10}$$

$$\mathbf{S_i^3 = h_3\ a_{i+n} + h_1\ a_{i+n+1}} \tag{11}$$

$$\mathbf{S_i^4 = h_2\ a_{i+n} + h_1\ a_{i+n+1}} \tag{12}$$

In the fourth stage, Eq. (13) and Eq. (14) are computed. Similarly, the Y_{LI} and Y_{HI} terms for DTCWT are computed as presented in Table 4.

$$\mathbf{Y_{LR} = S_i^1 + S_i^2} \tag{13}$$

$$\mathbf{Y_{HR} = S_i^3 + S_i^4} \tag{14}$$

Table 4. Computation of imaginary terms of DTCWT

DTCWT Terms	$Y_{LI} = h_3 (X_i + X_{i+1}) + h_1 (X_{i+3} - X_{i+2}) + h_2 (X_{i+4} + X_{i+5}) + h_1 (X_{i+6} - X_{i+7})$	
	$Y_{HI} = -h_1 (X_{i+2} + X_{i+3}) + h_2 (X_{i+5} - X_{i+4}) + h_1 (X_{i+6} + X_{i+7}) + h_3 (X_{i+8} - X_{i+9})$	
1st stage	$b_{i+n} = X_{i+1+n.} + X_{i+2+n.}\ \ n = 0, 1, 2, 3$	
2nd stage	$d_i^1 = h_1\ b_{i+n} + h_2\ b_{i+n+1}, n = 0$	$d_i^3 = h_3\ b_{i+n} + h_1\ b_{i+n+1},\ n = 0$
3rd stage	$d_i^2 = h_1\ b_{i+n} + h_3\ b_{i+n+1}, n = 2$	$d_i^4 = h_2\ b_{i+n} + h_1\ b_{i+n+1},\ n = 2$
4th stage	$Y_{LI} = d_i^3 + d_i^4$	$Y_{HI} = d_i^1 + d_i^2$

The reduced architecture consists of four stage pipeline scheme. The latency is 14T and throughput is 1T. For level-1 row filtering the number of arithmetic operations and timing parameters are summarized in Table 3.

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Table 5 Comparison of hardware requirements

Parameter	1st Stage Row Processing (1st Stage Column Processing)	
	Modified architecture with pipeline	Generic DTCWT architecture
Multipliers	16 (64)	40 (160)
Adders	24 (96)	36 (144)
Throughput	1T (1T)	4T (4T)
Latency	14T (24T+2N)	24T (48T+2N)
Pipeline stage	4	Nil
Intermediate memory	36 (144)	20 (80)

Level-2 DTCWT computation

The level-2 processing is performed on the four low pass sub bands (approximation coefficients), each of size N/2 x N/2. The level-2 comprises of stage 1 row processing and stage 2 column processing, which are realized using the pipelined structure as shown in Figure 3. The common terms in filter coefficients are simplified into coefficients represented as {g0, g1, g2, g3, g4, g5, g6}. The reduced output expressions are given in as in Eq. (15), and the corresponding reduced architecture is shown in Figure 3.

$$Y_{LPR} = X_i\ g_0 - X_{i+2}\ g_2 + X_{i+4}\ g_4 + X_{i+3}\ g_3 + X_{i+5}\ g_5 - X_{i+7}\ g_6 \quad (15a)$$

$$Y_{HPI} = -(X_i\ g_0 - X_{i+2}\ g_2 + X_{i+4}\ g_4) + X_{i+3}\ g_3 + X_{i+5}\ g_5 - X_{i+7}\ g_6 \quad (15b)$$

$$Y_{HPR} = -X_{i+2}\ g_6 + X_{i+4}\ g_5 + X_{i+6}\ g_3 - (X_{i+5}\ g_4 - X_{i+7}\ g_2 + X_{i+9}\ g_0) \quad (15c)$$

$$Y_{LPI} = -X_{i+2}\ g_6 + X_{i+4}\ g_5 + X_{i+6}\ g_3 + X_{i+5}\ g_4 - X_{i+7}\ g_2 + X_{i+9}\ g_0 \quad (15d)$$

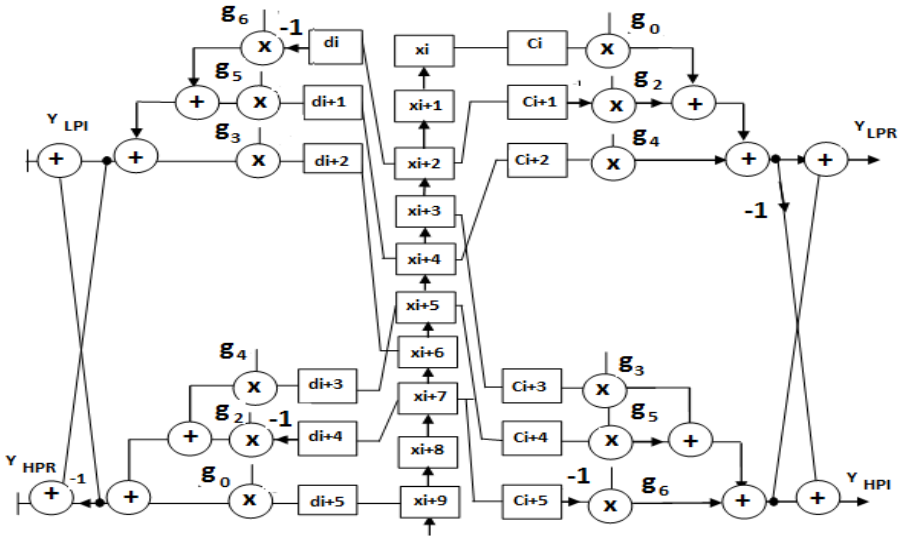

Figure 3 Optimal Pipelined Filter Architecture

The reduced architecture for row processing comprises of 10 input registers, into which the input data is first loaded. The data path control unit reads corresponding elements into another register array represented by c and d that are on the right and left side of the register array. The contents of registers c and d are correspondingly multiplied by the filter coefficients and accumulated in two stage adder array. A last stage accumulator unit designed as butterfly structure generates the real and imaginary components. The total number of multiplier and adder units is designed to be 12 and 12 respectively.

VLSI Implementation

Figure 4 shows the block diagram of the top level architecture for 2D DTCWT processor. The basic 2D DWT architecture for image decomposition as presented by Yun-Nan Chang and Yan-Sheng Li, (2001).

B. K. Mohanty and P. K. Meher, (2013) derived modified 2D DTCWT architecture. The 2D DWT architecture consists of input memory, intermediate memory, output memory and DTCWT processor. The memory controller reads the individual frame that are stored in the input memory and the processed data is further stored in the output memory. The memory controller controls the address generation logic to read corresponding data from the input memory and store data in the corresponding location in the output memory.

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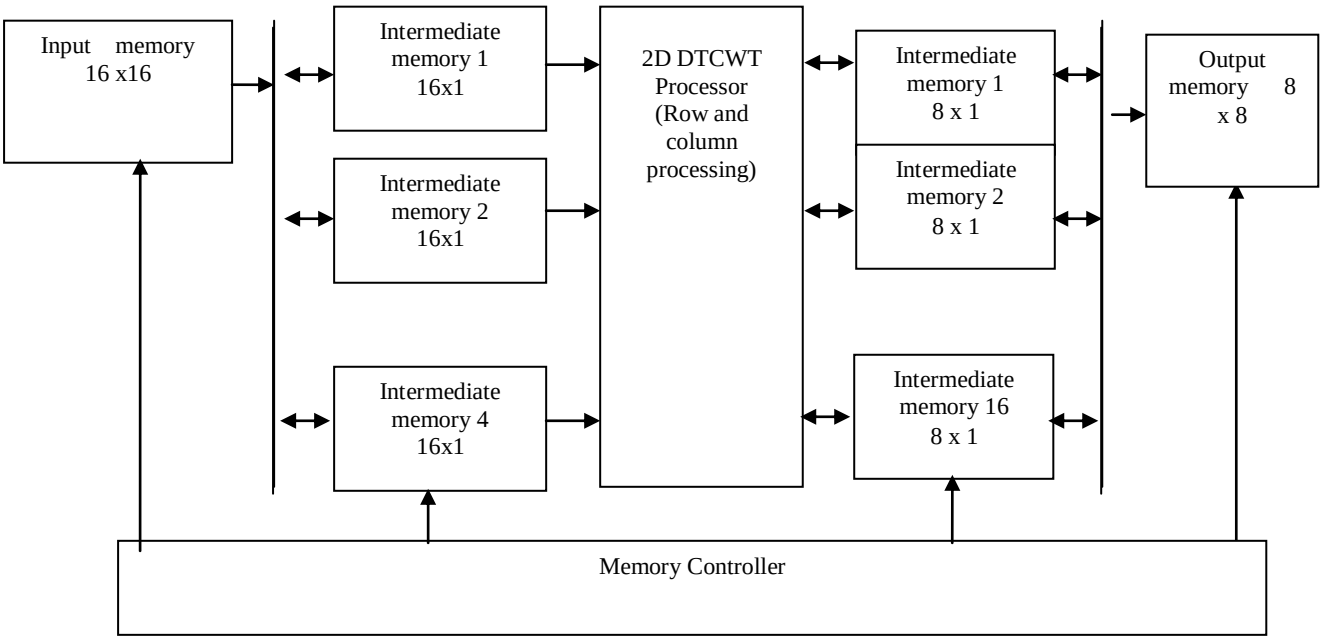

Figure 4 Top level architecture of 2D DTCWT processor

3D DTCWT Architecture

For the computation of 3D-DTCWT, 1D-DTCWT has been performed first on 16 frames each of size (16 x 16). The 16 frames are decomposed into four sub bands each of size (8 x 8) by performing 2D DTCWT computation as shown in Figure 4. There will be four real and four imaginary sub bands. In 3D DTCWT computation, the real and imaginary sub bands are processed further in the temporal domain considering all the four sub bands obtained after 2D DTCWT computation. The top level block diagram of 3D DTCWT architecture is shown in Figure 5.

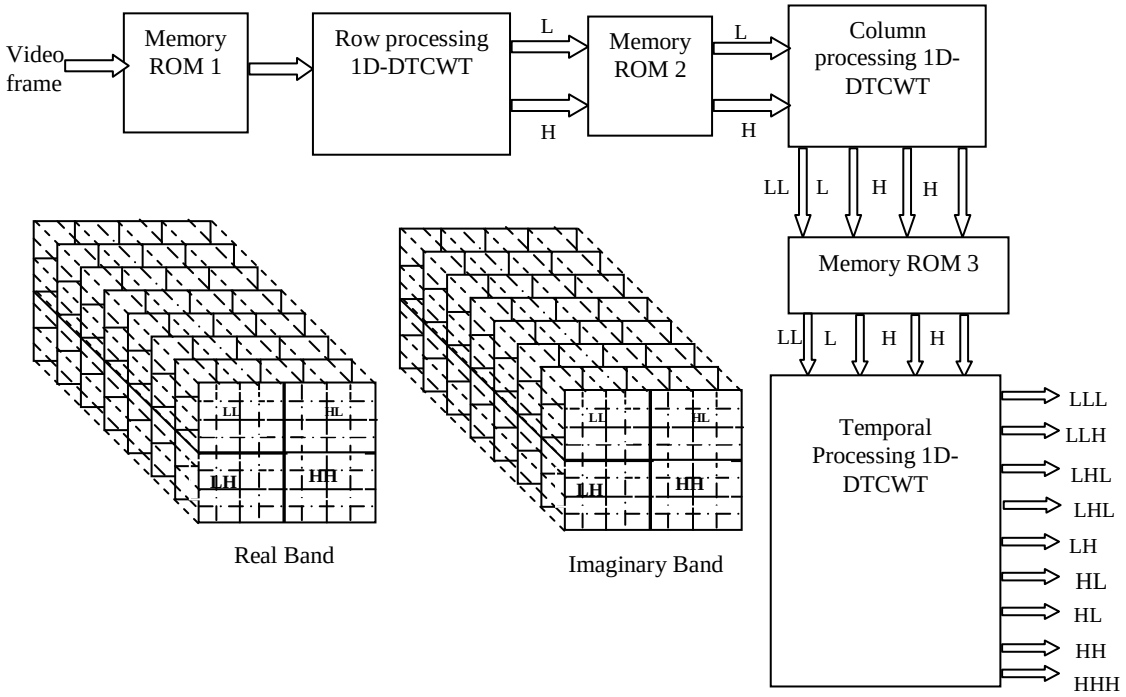

Figure 5 3D DTCWT architecture

For a 16 x 16 x 16 data size, row processing is carried out on 16 rows of each frame and hence the total number of row processing for all 16 frames is 256. Similarly, the number of times column processing is carried out to obtain 2D DTCWT computation is 256. After 2D DTCWT computation, there will be 16 frames each of size (8 x 8). Considering both real and imaginary sub bands there will be 16 frames of real and 16 frames of imaginary sub bands, with each frame comprising of four sub images of size (8 x 8). The 3D DTCWT is computed along the temporal direction considering all the four sub bands and requires 256 rows to be processed in temporal direction for real and another 256 rows to be processed for the imaginary sub band. The total number of 1D

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DTCWT processing required for computing 3D DTCWT is 1024. Each of the 1D DTCWT is designed considering the pipelined structure designed and presented in section 3.1.

RESULTS & DISCUSSION

The designed 3D DTCWT architecture is modeled in Verilog HDL and is verified for its functional correctness considering input data of size 16 x 16 x 16. The simulated results were compared with theoretical results and were found to be matching demonstrating logic correctness of the proposed architecture. The functionally correct HDL model is synthesized in the Xilinx ISE targeting Virtex-5 device. The synthesized net list for 1D DTCWT is shown in the Figure 6a and the RTL net list is shown in Figure 6b. The design is optimized for power, area and timing. RTL synthesized block diagram of DTCWT is obtained using Xilinx ISE and the synthesis report is analyzed for estimation the performances of the proposed design in terms of area, speed and power.

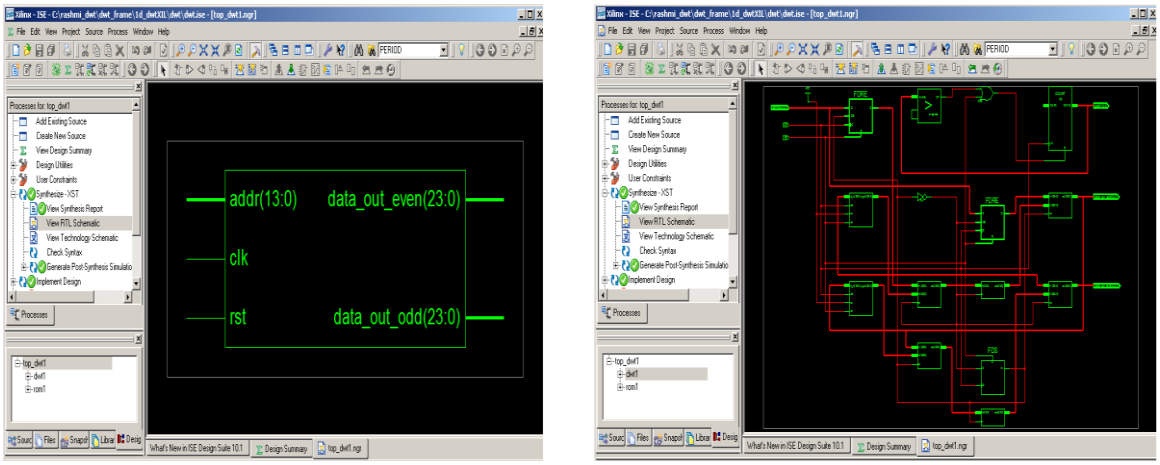

Figure 6 1D DTCWT implementation (a) top level net list (b) RTL net list

Figure 7 presents the top level net list of 2D DTCWT structure and Figure 8 presents the top level net list of 3D DTCWT structure.

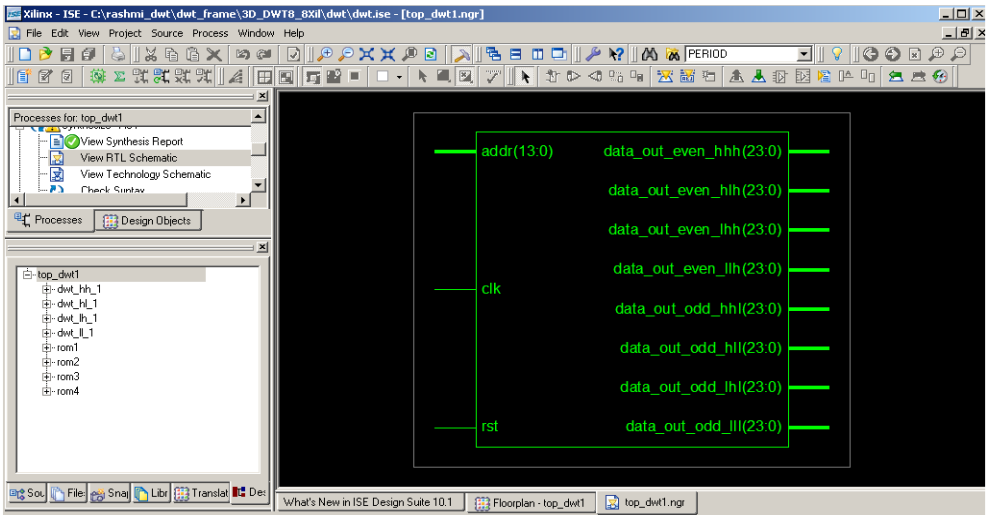

Figure 7 2D DTCWT

Citation: Yashavantha kumar ,T. R, *et al.*, High Speed Low Power 1D DTCWT Accelerator for 3D DTCWT Architecture Design for Plant Pheno typing Video Encoding. Australian Journal of Basic and Applied Sciences, 13(2): 36-45. DOI: 10.22587/ajbas.2019.13.2.5

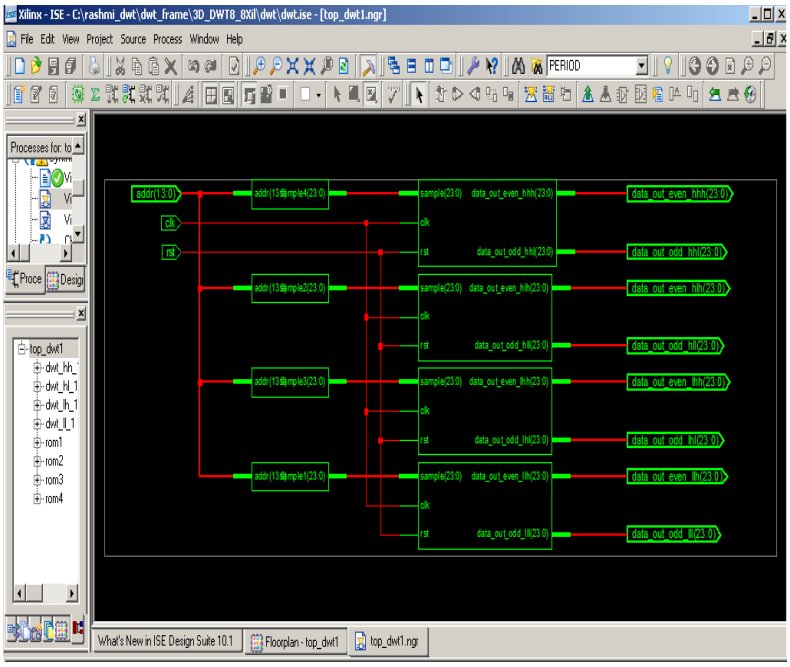

Figure 8 3D DTCWT RTL net list

Table 6 summarizes the FPGA implementation results of designed 2D DTCWT architecture comparing area utilization in terms of LUTs, total power dissipation and maximum frequency of operation.

Table 4 Implementation results of 2D DTCWT

	Direct DTCWT	Reduced DTCWT	Pipelined DTCWT	Venkateshappa and Cyril Prasanna Raj P. (2017)
LUT utilization	8134	3894	3992	4091
Frequency of operation	182 MHz	298 MHz	328 MHz	268 MHz
Memory utilization	36	42	48	-
Total power dissipation	2.81 W	2.32 W	1.8 W	2.10 W

As far as the work on DTCWT FPGA implementation is observed there are no or very few papers reported in literature. In order to evaluate and validate the proposed architecture design, Verilog HDL model is developed for DTCWT implementation based on convolution algorithm and the results are compared with reduce architecture design and pipelined architecture design. The results are also compared with the work reported in literature [14]. From the results it is found that the proposed 2D DTCWT design is faster than existing architecture by 1.2x times, power dissipation is reduced by 1.16x times and area resources in terms of LUT utilization is reduced by 1.02x times. Conventional DTCWT architecture occupies large area and also operates ta frequencies less than 200 MHz and hence the proposed design is suitable for high speed data processing. Table 5 presents the hardware performance metrics for 3D DTCWT implementation comparing direct implementation and pipelined architecture.

Table 5 Implementation results of 3D DTCWT

	Direct DTCWT	Pipelined DTCWT
LUT utilization	10224	5322
Frequency of operation	152 MHz	298 MHz
Memory utilization	44	58
Total power dissipation	3.11 W	2.3 W

From the comparison results presented in Table 5, 3D DTCWT performance metrics evaluated considering Virtex-5 FPGA is better as compared with direct implementation. The memory resources can be reduced by considering proper design of data movement operation and memory reuse operations. The computation speed of 3D DTCWT will reduce further if multiple level decompositions are considered. In order to further improve computation speed systolic array structures can be designed that work on data reuse logic.

6. Conclusion

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In this paper, 3D DTCWT that is one of the major building blocks in video compression is designed using pipelined architecture that utilizes the symmetry property of filter coefficients. The reduced architecture and pipelined architecture is designed that computes two outputs and four outputs respectively. The reduced architecture reduces the number of multiplication operation and the pipelined architecture is designed that overcomes the limitation of reduced architecture by considering common terms among all the four filters. The designed architecture is implemented on FPGA and is found to operate at frequency greater than 250 MHz consuming less than 2.5 W of power. The architecture designed in this work is suitable for real time data compression on FPGA platform. The computation complexity in data compression of plat phenotyping data can be addressed by use of the 3D DTCWT processor designed in this work.

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