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Autogated Flip Flop Based Low Power Clock Distribution

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ABSTRACT

The Clock distribution uses current than voltage, to distribute a global clock signal with reduced power consumption. While current-mode (CM) signalling has been used in one-to-one signals, this is the first usage in a one-to-many clock distribution network. To achieve this, we want to create a new high-performance current-mode pulsed flip-flop with enable (CMPFFE) .One of the major dynamic power consumers in computing and consumer electronics products is the system's clock signal, generally responsible for 35% to 75% of the total dynamic (switching) power consumption. Several techniques to minimize the dynamic power have been developed, of which clock gating is predominant. Clock gating is very useful for decreasing the power consumed by digital systems. Three gating methods are known, the most popular is synthesis-based, determining clock enabling signals based on the logic of the underlying system. It unfortunately leaves the majority of the clock pulses drive the flip-flops (FFs) redundant. A data-driven method stops most of those and yields higher power savings, but its implementation is complicate and application dependent. A third method called Auto-Gated FFs (AGFF) is simple but yields relatively small power savings. Look-Ahead Clock Gating (LACG).

INTRODUCTION

Overview:

Portable electronic devices require great battery lifetimes which can only be obtained by utilizing low-power components. Recently, the low-power design has become quite critical in synchronous application specific integrated circuits (ASICs) and system-on-chips (SOCs) because an interconnect in scaled technologies is consuming an increasingly significant amount of power. Researchers have demonstrated the major consumers of this power are global buses, clock distribution networks (CDNs), signals in general. The CDN in the POWER microprocessor, for example, dissipates 72% of total chip power. In addition to the power and interconnect delay poses a major obstacle to high-frequency operation. Technology scaling reduces the transistor and local interconnect delay while increasing the global interconnect delay. Moreover, conventional CDN structures are becoming difficult for multi-GHz ICs because skew, jitter, and variability are often proportional to large latencies .Prior to and in early the CMOS technologies, current-mode (CM) logic was an high-speed signaling scheme .CM logic, however, consumes significant static power to offer these high speeds. Because of this,

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standard CMOS voltage-mode (VM) signalling has been the factor standard logic family for the several decades.

Low-swing and current-mode signalling, however, are highly attractive solutions to help address the interconnect power and variability problems. Traditionally, the static power dominates and dynamic power consumption in a CM signaling scheme. However, the static power is often significantly less than VM dynamic power and latency is significantly improved over VM in global CM interconnect.

Instead, the power savings is maximized by create a high-fanout physically or electrically symmetric distribution that feeds many CM flip-flop (FF) receivers. Logic signals on the FF receivers from VM compatibility with low-power CMOS logic in the remainder of the chip. In this paper, we present the first true CM CDN and a new CM pulsed D-type FF where the clock (CLK) input is a CM receiver and data input (D), an active low enable, and output (Q) are VM. In particular, the key contributions of this paper are:

- The first demonstration of the CM clocked FF
- The effective integration of the CM FF to VM CMOS logic
- Power consumption comparison of CM CDN and VM CDN at different frequencies
- Noise and variability analysis of the CM and VM CDN.

Clock signals are important in synchronous circuits to the synchronize different data signals arriving.

1.2 Clock Distribution Network:

From different parts of the integrated circuit, such that the correct data is available for computation. Due to impedance that present in interconnects there are mismatches in the clock arrival time due to spatial distances between two clocks. These mismatches time are known as clock skews. Due noises caused by other interconnect lines running in parallel with the clock signals, clock signals arriving at two different registers with the same clock input experience a phase noise, commonly known as clock jitter .

Different methods are employed to satisfy the clock conditions given above. Such techniques involve a tree like structure that has the main “trunk” supplying the global clock which branches at various points in the circuit based on the loads. Such the clock distribution networks include buffered clock distribution network, X-tree distribution network, H-tree distribution network, and mesh type clock distribution network. To ensure that clock load is balanced at each branch of the clock tree in an X-tree or H-tree network, interconnect that carries these clock signal are scaled by 1/3 at each branch

1.3 Flip Flop:

In electronics, a flip-flop or latch is a circuit that has two stable states can be used to store state information. A flip-flop is the bistable multivibrator. The circuit can be made to change state by the signals applied to one or more control inputs, will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are the fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

Although the term flip-flop has historically referred generically to both simple and clocked circuits, in modern usage it is common to reserve the term flip-flop exclusively for discussing clocked circuits; the simple ones are commonly called latches. Using this methodology, a latch is level-sensitive, whereas a flip-flop is edge-sensitive. That is, when a latch is enabled it becomes transparent, while a flip flop's output only changes on a single type (negative going or positive going) of clock edge.

Since the elementary amplifying stages are inverting, two stages can be connected in the succession (as a cascade) to form the required non-inverting amplifier. In this configuration, each amplifier may be considered as a active inverting feedback network for the other inverting amplifier. Thus the two stages are connected in a non-inverting loop although the circuit diagram is usually drawn as symmetric cross-coupled pair (both the drawings are initially to introduced in the Eccles–Jordan patent).

D Flip Flop:

This latch exploits the fact that, in the two the active input combinations (01 and 10) of a gated SR latch, R is the complement of S. The input NAND stage converts the two D input states (0 and 1) to these two input combinations for next SR latch by inverting data input signal. The low state of the enable signal produces the inactive "11" combination. Thus a gated D-latch may be considered as a one-input synchronous SR latch. This configuration prevents application of the restricted input combination. It is also known as data latch, transparent latch or simply gated latch. It has the data input and an enable signal (sometimes named clock, or control). The word transparent comes from the fact that, when the enable input is on, the signal propagates directly through the circuit, from the input D to the output Transparent latches are typically used to I/O ports or in asynchronous systems or synchronous two-phase systems (the synchronous systems that use a two-phase clock), where two latches operating on different clock phases the prevent data transparency as in a master–slave flip-flop.

1. Low-Power Dual Dynamic Node Pulsed Hybrid Flip-Flop Featuring Efficient Embedded Logic:

In this paper, a new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFF-ELM) based on DDFF is proposed. The designs eliminate the large capacitance present in the precharge nodefollowing a split dynamic node structure to separately drive the output pull-up and pulldown transistors. The conditional data mapping flip-flop (CDMFF) is one of the most efficient among them. It uses an output feedback structure to conditionally feed the data to the flip-flop. This reduces overall power dissipation by eliminating unwanted transitions when a redundant event is predicted. Since there are no added transistors in the pull-down nMOS stack, the speed performance is not greatly affected. But the presence of three stacked nMOS transistors at the output node, similar to HLFF, and the presence of conditional structures in the critical path increase the hold time requirement and D-Q delay of the flip-flop.

2. *Proposed Method:*

2.1 Look Ahead Clock Gating:

Look-Ahead Clock Gating (LACG), which combines synthesis based clock gating, data driven clock gating. LACG computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. It avoids the tight timing constraints of AGFF and data-driven by allotting a full clock cycle for the computation of the enabling signals and their propagation. A closed-form model characterizing the power saving per FF is presented. It is based on data to-clock toggling probabilities, capacitance parameters and FFs' fan-in. Furthermore, unlike data-driven gating whose optimization requires the knowledge of FFs' data toggling vectors, LACG is independent of those. The embedding of LACG logic in the RTL functional code is uniquely defined and easily derived from the underlying logic, independently of the target application. This simplification is advantageous as it significantly simplifies the gating implementation.

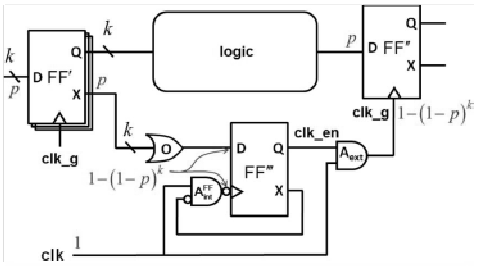

Fig. 2.1: Look Ahead Clock Gated Flip FLOP.

The FF's master latch becomes transparent on the falling edge of the clock, where its output must stabilize no later than a setup time prior to the arrival of the clock's rising edge, when the master latch becomes opaque and the XOR gate indicates whether or not the slave latch should change its state. If it does not, its clock pulse is stopped and otherwise it is passed. A significant power reduction was reported for register-based small circuits, such as counters, where the input of each FF depends on the output of its predecessor in the register. AGFF can also be used for general logic, but with two major drawbacks. Firstly, only the slave latches are gated, leaving half of the clock load not gated. Secondly, serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating.

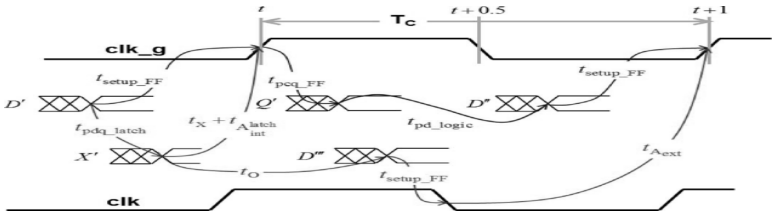

Fig. 2.2: Timing sequencing of LACG clock gating.

Look-Ahead Clock Gating (LACG) computes the clock sanction native signals of each FF one cycle previous time, supported this cycle info of those FFs on it depends. Uniformly to data-driven gating, it's capable of stopping the majority of redundant clock pulses. It has an enormous advantage of avoiding the tight temporal arrangement constraints of AGFF and data-driven, by allotting a full clock cycle for the facultative signals to be computed and propagate to their gater. Furthermore, unlike data-driven gating whose optimization requires the flip-flops toggling vectors, LACG is independent of those. LACG logic in the RTL functional code is uniquely defined and easily derived from the underlying logic, independently of the target application. This

simplification is advantageous as it significantly simplifies the gating implementation. Theoptimization plays an important role in the process of clock gating. The most probably used techniques for optimization are ACO, PSO, GA and ANFIS.

2.1.2 Power Consumption:

Dynamic power management could be a powerful methodology for reducing power consumption in electronic systems. It encompasses a collection of techniques that achieves energy-efficient computation by selection, reducing the performance of the system parts after they are idle. During a power-managed system, the state of operation of assorted parts is dynamically custom-made to the specified performance level, in an attempt to reduce the facility wasted by idle or underutilized parts. For many system parts, state transitions have non negligible power and performance prices. Thus, the matter of planning power management policies that minimize power underneath performance constraints could be a difficult one. It has been with used with success in several real-life systems, a lot of work is needed for achieving a deep understanding on the way to style systems that may be optimally power managed.

Optimization for power is usually one in all the foremost vital style, objectives in fashionable nm microcircuit style. Their paper presents: (I) a completely unique style methodology of applying multi-bit flip-flops at the post-placement stage, which may be seamlessly integrated in fashionable style flow; (ii) a replacement drawback formulation for post-placement improvement with multi-bit flip-flops; (iii) flip-flop agglomeration and placement algorithms to at the same time minimize flip-flop power consumption and interconnecting wire-length; and (iv) a progressive window-based improvement technique to cut back placement deviation and improve run-time potency of our algorithms. During a projected system conferred a replacement drawback formulation of post-placement improvement with MBFFs to optimize the facility consumption of the clock network, supported the matter formulation, tend to projected flip-flop grouping and MBFF placement algorithms to at the same time minimize flip-flop power consumption and interconnecting wire-length specified each placement density and temporal arrangement slack constraints are happy. To scale back placement deviation and improve run-time potency of our algorithms, the progressive window-based improvement technique has been introduced. This approach is extremely effective in reducing not solely flip-flop power consumption, however additionally clock tree and signal web wire-length once applying MBFFs to a style at the post-placement stage.

Clock power is that the major contributor to dynamic power in contemporary computer circuit style. A standard single-bit flip-flop cell uses associate electrical converter chain with high drive strength to drive the clock signal. While not enumerating all attainable mixtures, determine only partial sequences that are necessary to cluster flip-flops, therefore resulting in an associate economical clump theme. Moreover, our quick coordinate transformation additionally makes the execution of our rule terribly economical. A quick multi bit flip-flop bunch rule has been planned for clock power saving. To resolve the time and area deficiencies encountered by recent works, assume coordinate transformation and expressed the possible regions by 2 interval graphs. The probabilistic model of the clock gating network that enables us to enumerate the expected power savings and therefore the inexplicit overhead. Expressions for the ability savings in an exceedingly gated clock tree are given and therefore the optimum gated fan-out springs. The derivation is predicated on the toggling likelihood of the FFs comprising the circuit, the relative capacitance factors of the method technology and cell library in hand, and therefore the filler factors utilized in the clock tree construction. The ensuing clock gating methodology achieves 100% savings of the overall clock tree shift power. The temporal arrangement implications of the planned gating theme area unit mentioned. The grouping of FFs for a joint clocked gating is additionally mentioned. The analysis and therefore the results match the experimental information obtained for a three-D graphics processor and a 16-bit micro-controller, each designed at 65-nanometer technology.

2.1.3 Data transition look ahead flip-flop:

Flip-flops, have their content change to only either at the rising edge or falling edge of enable signal. But, after the rising or falling edge of the enable signal, the flip-flop's content remains to constant even if the input changes. In a conventional D Flip Flop, to the clock signal always flows into the D flip-flop irrespective of whether to the input changes or not. Part of the clock energy is the consumed by the internal clock buffer to control in transmission gates unnecessarily. Hence, if input of the flip-flop is identical to its output, the switching of clock can be suppressed to conserve power

2.1.3.1 Logic gating:

The transmission gates TG4 and TG5 in data look ahead block the data transition look ahead. It compares hold data at output with the respective input data and enables flip flop to write the data, accordingly. The DL block act as XNOR gate. For example, when Q = D= 1, the clock is inactive and transmission of data is not required. But, when Q = 1, D = 0, the clock is enabled and data gets transmitted.

2.1.3.2 Clock gating:

The Clock control block consists of transmission gate TG6 followed by NMOS transistor. The clock control signal depends on DL's output. The input to the clock control is given by external clock CSP and divides into CK and CKN

2.1.3.3 Operation:

A DLDFF is triggered by positive edge of the clock (CSP). When an input data D is the same as the hold output data Q, the DL circuit makes P1 to low. This turns the TG in the clock gating circuit to off. Because of that, CK and CKN do not transmit. CK and CKN transmit only when D and Q are different. When D changes to a value different from Q, P1 1st changes to 1. Next, when CSP rises, CK also rises and changes. Then, P1 again changes back to 0 since D and Q are the same again. This immediately makes CK low. Therefore, a DLDFF consumes less power of than a conventional one, because CK is inactive when there are no data transitions.

Result And Observation:

Clock enabling signals are to very well understood at the system level and thus can effectively be defined and capture the periods where functional blocks and modules do not need to be clocked. Those are later being automatically synthesized into clock enabling signals at the gate level. In many cases, clock enabling signals are manually to added for every FF as a part of a design methodology.

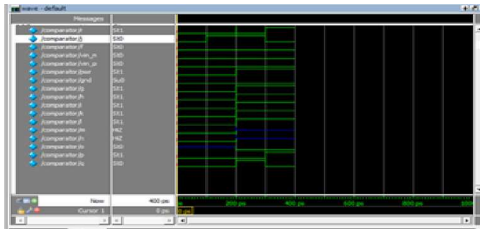

Fig. 3.1: Proposed data look ahead flip-flop.

The wave form shows the power consumption using look ahead flip flop The clock control signal depends on DL's output. The input to the clock control is given by the external clock CSP and divides into CK and CKN

Conclusion:

The presented gating scheme is first verified by a formal verification EDA tool and it was found equivalent to original circuit before the gate logic was introduced. Though not surprising, it is must in an industrial environment where the method was experimented. It is important to the introduction of LACG made most of the gate-level clock gating techniques employed by the design redundant. Those were therefore dropped, which somewhat compensated the LACG power and area overhead.

The Data look ahead D Flip-Flop will be best suited for large circuits since it can drive very large loads efficiently. It consumes only 40% of total power with around 75% reduction in delay. The clock gated conditional capture flip-flop will work efficiently under high frequency applications provide around 75% power reductions. It is also proved that it has very less delay for high frequencies provided that only minimum amount of load connected to it.

Look-ahead clock gating has been shown to be very useful in reducing clock switching power. The computation of clock enabling signals one cycle ahead of time to avoids the tight timing constraints existing in other gating methods. A closed model characterizing the power saving was presented and used in the implementation of gating logic. The gating logic can be further optimized by matching the target FFs for joint gating which may significantly reduce the hardware overheads

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