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Circuit Design and CNTFET Implementation of Ultra-fast Reversible Fast Adder

[1]R.M.Bommi and [2]Dr.S Selvakumar Raja

[1]*Research Scholar*: Dept of ECE Sathyabama University Chennai, India
[2]*Associate Professor*: Dept of ECE University of Gondar Ethiopia

Address For Correspondence:
R.M. Bommi, Research Scholar: Dept of ECE Sathyabama University Chennai, India.
E-mail: rmbommi@gmail.com

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ABSTRACT

VLSI concentrates on two major areas in logic circuit design, they are low power logic design and reduction in size of the circuit. This paper is focused on the reduction of the power consumed and heat dissipation by the logic circuit. The proposed system is developed with the basic of reversibility which is an eight bit reversible Carry Select Adder implemented with Carbon Nano Tube as the channel material for the transistors. The design is efficient in not only in terms of power but also makes its architecture simple. Simulation is carried out in HSPICE environment and the results shows that the proposed adder is faster and consumed less power when implemented in CNTFET as compared to CMOS.

INTRODUCTION

Reversibility is the basic concept behind the design of the proposed system which offers to be an information lossless addition. Reversible logic also has inevitable applications in nano-computing and Quantum computing, which are power efficient [5], [6]. The main advantage of this technology is that the input stages can be retrieved back, by which erasure of data gets eliminated resulting in a lesser power consuming logic. The lateral scaling follows Moore's law shrinking and reducing the area of devices in an IC (Moore, G., 1975). Moreover, for improving the carrier transport in the channel region of the transistor, several researches are being progressed. (Datta, S., 2005). One best solution to the problem is to realize the devices having high channel mobility is to use CNTs (Carbon Nano Tubes).

Reversible Logic:

According to Landauer research, for every irreversible bit Operation the amount of energy dissipated is at least *KTln2* of energy in joules, where K is the Boltzmann's constant and T is the temperature during active mode (Landauer, R., 1961). Increasing the device density and scaling down, high failure rate and power consumption are serious challenges for digital circuits.In 1973, according to Bennett in another experimental research, proved that the observed outputs will not dissipate heat energy as long as the device allows the recovery of inputs (Bennett, C.H., 1973).

Quantum cost, garbage output and constant inputs are the basic requirements to be considered while designing any circuit in reversible logic. The quantum modular exponentiation when performed in a reversible logic way increases proportional with the size of the number to be factorised. So the Auxiliary memory also grows linearly with the reversible way (Artur Ekert, 1995).This information lossless logic finds extensive application in nano computing, optical computing, nano technology, and DNA technology and quantum computers. A quantum

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network composed of quantum logic gates is a quantum computer. Each quantum logic gate performs unitary operation on qubits and the Quantum cost is the total number of gates used primarily in the circuit.

The CNTFET:

CNTFETs possess honeycomb tubular shape on a molecular level and uses Carbon Nano tube as channel material inplace of Silicon in conventional MOSFETS. Carbon nanotubes find remarkable applications in various fields like interconnects, memory and logic devices, sensors and as an electron source in field emission devices (Martel, R., 2001). CMOS transistors suffer limitations like leakage current, electron tunneling, doping and variation in device structure when scaled below 22nm range. In order to overcome the above said limitations, CNTFETs can be used for implementing the proposed system since they are not subjected to the scaling problems as in traditional CMOS devices. In Carbon nanotube field effect transistor (CNTFETs) the channel is made up of carbon nanotube that sits above the substrate forming the gate terminal. The structure of n-channel and p-channel transistors made from nanotubes is as shown in the Fig 1.1. This structure of CNTFETs is same to that of conventional MOSFETs and their transfer characteristics an Id – Vd characteristics are also most promising alternative in near future.

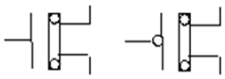

Fig 1.1: Structure of N-CNTFET and P-CNTFET.

Reversible Gates:

In the reversible logic the total number of inputs and outputs are equal i.et there is one to one correspondence between the inputs and outputs. Reversible logic is also called as charge recovery logic or adiabatic logic and exhibits zero energy dissipation. The Proposed fast adder i.e carry select adder is designed with (FTFA) Fault tolerant full adder gate and (FG) Fredkin gate as it provides a power efficient circuitry and each gate has specific function to be performed.

A. Fredkin Gate:

Fredkin gate is a reversible (3*3) three input- three output gate as shown in fig 1.2. Basic operation of the gate is to swap the inputs. This is performed when the input A=1. Since the input A is maintained constant the input B is mapped to output R and input C is mapped to output Q. Due to this operation this gate is used as a multiplexer in this design.

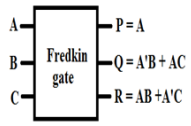

Fig 1.2: Fredkin gate.

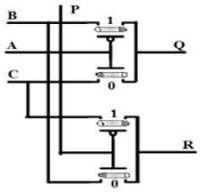

Fig 1.3: CNTFET implementation of FG gate.

The CNTFET transistor level implementation of Fredkin gate which acts as a 2 to 1 Multiplexer is as shown in the Fig 1.3 which has only 2 inputs and 1 select line.

B. Fault Tolerent Full Adder:

Islam gate is a reversible (4*4) four input four output gate as shown in fig 1.4. This gate can provide a function of parity preserving. Islam gate when combined with another islam gate can act as a full adder. Two Islam gates combined to form a full adder which is called FTFA is shown in the Fig 1.5.

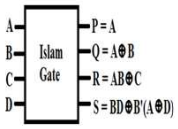

Fig. 1.4: Islam gate.

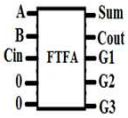

Fig. 1.5: Fault tolerent full adder.

The Fig 1.6 shows CNTFET implementation of the FTFA for performing the unitary addition operation of the input a and b with both 0 and 1 as input.

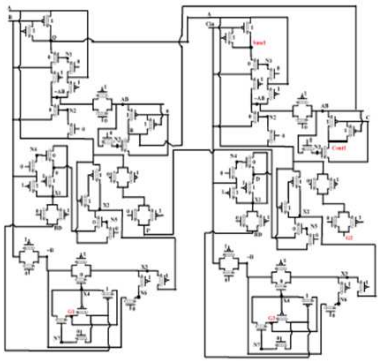

Fig. 1.6: Transistor level implementation of FTFA gate.

Reversible Carry Select Adder:

Carry select adder is one of the efficient fast adders whose computation is performed with a precomputed carry. The basic block diagram of one bit reversible carry select adder is as shown in the fig 1.7 . In this bit A and Bit b are added with the FTFA with cin to be initialized to be ZERO (0) in one full adder and ONE(1) in another full adder. The sum and carry of each of addition is obtained at the output of each FTFA gate and to select the exact computation output , FG gate act as a multiplexer.

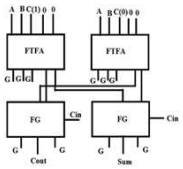

Fig 1.7: 1-bit carry select adder.

For designing a 8-bit reversible carry select adder eight such stages are combined toghether as shown in the Fig 1.8 The output carry of first stage is taken to the next stage and is fed as input carry to theFTFA and FG gates, so that the sum and carry of that is computed and the same process is repeated . The block shown in the Fig 1.8 consists of 32 gates with 80 garbage outputs and 32 constant inputs.+

RESULTS AND DISCUSSION

The carry select adder with Inputsa[8:1], b[8:1], cin & outputs sum_1[8:1], cout_8 ,designed with the reversible logic is simulated to obtain its output characteristics in HSPICE environment. The tool used for obtainnig the characteristics output is Hspice analog circuit simulator with the help of cosmos scope viewer.

Cosmos scope is verification tool used to view the waveform generated by the HSPICE.. This is an efficient nodal analysis tool which helps to implement the transistor level netlist of the circuit easily. The circuit is simulated with CNT FET and CMOS libraries which are readily available in Spice.The fig 1.9 shows the simulation result of 8-bit carry select adder implemented using CNTFET.

The fig 1.9 shows the simulation result of 8-bit reversible carry select adder implemented using conventional CMOS.

The power Comparison of reversible 8-bit carry select adder implemented in CNTFETs and CMOS transistors with two different supply voltages are tabulated in Table 1.1.It is observed that there is a drastic change in the power consumption of the order of milliwatt to microwatt.

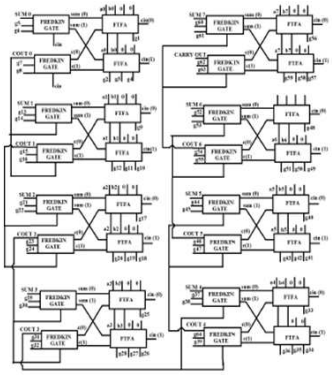

Fig. 1.8: 8-bit carry select adder.

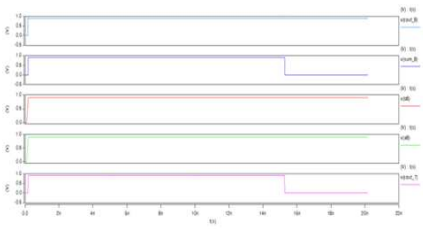

Fig 1.9: Simulation result using CNTFET.

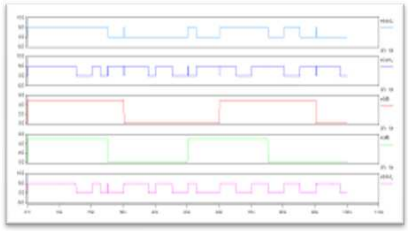

Fig 1.10: Simulation result using CMOS.

Table 1.1: Comparison table to show the power reduction.

Design	Supply voltage	Avg_power (w)
Rev CSA using	5v	6.02E-05
CNTFETs	3v	1.73E-06
Rev CSA using	5v	1.70E-03
CMOS	3v	1.66E-03

The comparison of reversible carry select adder with the existing adders in terms of total number of garbage outputs, number of gates used in the logic circuit, delay and ancilla inputs are tabulated in the Table 1.2 . It is observed that the designed carry select adder showed better performance in terms of gate count, ancilla inputs and delay but the garbage output is more compared to the existing circuit (Susan Christina, X., 2010).

Table 1.2: Comparison of reversible carry select adders.

Adder	Reversible Gates	Ancilla inputs	Garbage outputs	Delay
Proposed 4-bit CSA	8 FG+8 FTFA=16	16	40	2.83 ps
Proposed 8-bit CSA	16FG+16 FTFA=32	32	80	5.66 ps
Existing 4-bit CSA (Susan Christina, X., 2010)	4FG+8TSG+8F = 20	20	24	476.223ns

Conclusion:

In prior to the existing work carried so far, this paper proposed the design of an eight bit carry select adder and implemented both in CNTFETS and CMOS. This proves that the CNT FETS can over come the draw back of CMOS in micron scaling. The power reduction is possible since the average carrier velocity is double in CNTFET as compared to conventional CMOS. The carry select adder designed is used in arithmatic calculations such as multiplication. This reversible design is very useful in designing quantum computers, low power logic circuits and high speed multipliers.

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