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Design of Multiplexer Based 64-Bit SRAM using QCA

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ABSTRACT

Quantum-dot Cellular Automata is a new trend in nanotechnology and investigated as an alternative to the current CMOS technology. QCA provides an attractive computational paradigm to design digital system architecture. This work proposes a novel multiplexer-based 64-bit SRAM architecture in which the area and clock delay are optimized. The loop-based memory in motion paradigm is accomplished in each QCA memory cell and clocking zones are shared between memory cells. The read/write operations are implemented by simplified control circuitry with less area for the higher order memory array. The Proposed QCA memory cell with control circuit uses 104-QCA cells and reduced area. The advantages of the proposed work is sharing the clock zones in a column reduces the number of clock delay. For 8x8 memory utilizes only 5-clock cycles to complete read/write operations.

INTRODUCTION

Advancement in CMOS fabrication technology in the last few decades reduces the feature size of the transistor and scales down the supply voltage. Due to the decreasing supply voltage, the power consumption from leakage current is a big challenge for transistor circuits (Rairigh, D., 2005). As the device size is reduced, power dissipation, leakage current, interconnect wiring and capacitances become a potential bottlenecks to the circuit performance. The International Technology Roadmap for Semiconductors (ITRS) predicts that the size limit for CMOS technology to be 5 to 10 nm by 2016 (Lent, C., 1994) and summarizes several possible technology solutions ((IRTS), 2007) Nanotechnology is an alternative to these problems and the Quantum-Dot cellular automata is one of the attractive alternatives. QCA technology has been introduced in 1993 (Amlani, I., 1999) and the experimental devices for semiconductor, molecular, and magnetic approaches have been developed. The molecular QCA devices can achieve high density of 10^3 per cm^2 and clock speed could be from 1 to 10THz at room temperature (Cowburn, R. and M. Welland, 2000) and (Frost, S., 2002). In terms of feature size, it is claimed that the size of the basic QCA cell can be implemented by few nanometres molecular fabrication at room temperature (Lent, C., 2003). The power dissipation of a QCA device with 10^{11} cells is approximately 100mW at 10THz (Timler, J. and C.S. Lent, 2002; Kummamuru, K., 2002).

QCA cell is arranged as a square pattern with four aluminum metal islands connected via tunnel junctions made of Al/AlO_x as shown in Fig. 1. Thermal fluctuation is avoided by keeping quantum – dot charging energy is much higher than thermal energy. Though the four dots are located at the corners of the cell and only two electrons are injected into a cell and makes two possible configurations of polarization which is encoded as binary '0' and '1'.

The QCA clock is used to control the signal propagation among QCA cells. QCA clocking has been operated using quasi-adiabatic switching, which allows recycling of energy by returning stored energy back to

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the supply and reduces the total energy drawn from the power supply. The computation process has been enabled by quantum-mechanical tunneling and columbic interaction between QCA cells.

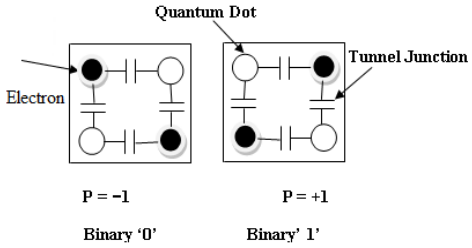

Fig. 1: QCA cell.

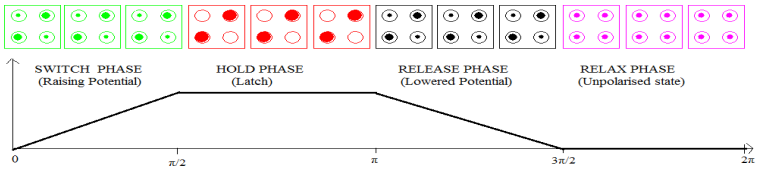

Fig. 2: Polarization of QCA Cells for different Clocking zones.

There are four-different clocking zones such as Switch, Hold, Release and Relax. The Polarization of QCA clocking is shown in Fig. 2. During Switch phase, the inter-dot barriers are slowly raised and the computation is performed. During the phase of Hold, the inter-dot barriers are kept high and the QCA cells retain their states and in the next phase of Release, the barriers are lowered and the cells are relaxed to an unpolarized state. During relax, the barriers are kept low and the cells remain in unpolarized state.

A set of equally sized tiles together forms complex circuits in the square formalism. The QCA memory can be designed using square formalism (Berzon, D. and T. Fountain, 1999). The main advantage of this technique is simple geometric layout and disadvantage of this methodology is lower density and spatial redundancy and additional control circuit.

The H-memory architecture has been introduced by researchers from Notre Dame University (Frost, S., 2002), it uses a squared shaped spiral structure that loops back itself for storing data and the sections of each layer of the spiral can be in the same clocking zone. It is a complete binary tree structure and the additional control circuit is provided at each node to perform read/write operation. Though the word size of each memory cell is increased by adding extra layers, the number of clocking zones is not increased. The architecture achieves high density and uniform access time but requires complex control logic circuit and the memory size is not linear with cell count.

The parallel memory architecture was proposed in (Walus, K., 2003). In this architecture, one-bit information can be stored at each memory cell which is designed using 158 QCA cells with simple read/write circuit. The limitation of this approach is the requirement of the large number of clocking zones.

The design of parallel QCA memory was introduced in (Vankamamidi, M., 2005), the number of clocking zones was independent of the memory size and shared among all memory cells in a column. Also, the read/write control circuit was very simple and requires two additional clock signals. In the line-based architecture, the storage was achieved by moving data back and forth in QCA line. This line-based memory architecture design needs additional three zones for storage and the four-step process whose timing was different from the adiabatic switching.

Tile-based memory architecture has been discussed in (Vankamamidi, M., 2008) contains three tiles and placed in the order of input tile, output tile and memory tile to store one-bit information. The number of memory tiles can be extended between input and output tiles according to the storage of N-bit information in which the input tile is used to multiplex new input values into the memory loop. The memory tile is designed using 74 QCA cells, whereas 24 and 54 QCA cells are utilized for the input and output tiles.

The synchronization of line-based memory architecture has been improved in (Taskin, B. and B. Hong, 2006) using dual phase clocking signal and the clock zone required for data storage was reduced to two. The dual phase clocking signal was excited using single clock generator.

Multiplexer-Based Memory Architecture:

This work proposes a novel multiplexer-based 64-bit SRAM architecture in which the area and clock delay are optimized. The one-bit memory cell is designed using a 2 to 1 multiplexer with control circuit. The circuit

diagram of the memory cell and its QCA layout are shown in Fig. 3 & Fig. 4 respectively. The address decoder circuit selects the entire row of the memory cells and the additional control is provided for read/write operations.

The input control circuit is designed using two majority gates and the output control circuit consists of one majority gate and both functions efficiently to perform read/write operations. In QCA-based memory logic, memory must be kept in motion, i.e., the memory state has to be continually moved through a set of QCA cells. These cells are connected in a loop and are partitioned into four clocking zones. At any point of time, one of the zones must be in hold phase to retain the information. The Proposed QCA memory cell with control circuit uses 104-QCA cells and has reduced area.

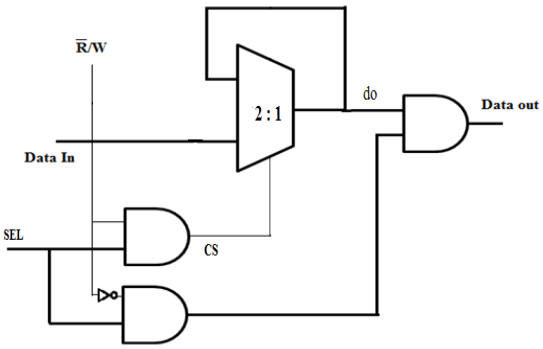

Fig. 3: Circuit diagram of one-bit memory cell.

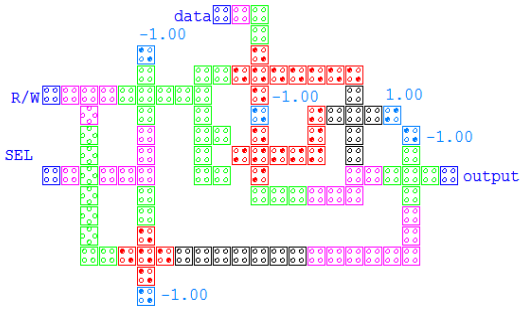

Fig. 4: QCA layout of memory cell.

Table I: One-Bit Memory Cell.

SEL	R/W	Operation	Data out
High	High	Write	Low
High	Low	Read	Data In
Low	High or Low	Holding	Low

Table I shows the operation of one-bit memory cell. When the R/W and row select signals are logically high, the new input state is written into memory cell and hold it until it receives the next control signal. If R/W goes low and the row select remains high, the memory state is read out by the data out pin. When row select signal goes low, data will be held in the memory loop. The Read/Write control circuit is implemented using majority gates which is defined mathematically in Equation - (1) and (2). The equation – (3) describes the funtion of Multiplexer-based memory loop which is aquiring control signal CS from control circuit.

$$\text{data out} = M[\, d0, M[\, \overline{\overline{R}/W}, SEL, 0\,], 0\,] \quad (1)$$

$$CS = M[\, SEL, \overline{R}/W, 0\,] \quad (2)$$

$$d0 = M[\, M[\, d0, CS, 0\,], M[\, \text{data in}, CS, 0\,], 1] \quad (3)$$

CMOS based SRAM is designed using parallel architectures, in which the all the bits of information are read-out simultaneously. But in QCA-based memory design, data read and write in the memory cell is performed in different clock zones which makes it impossible to read the data simultaneously. Introducing delay in memory cells will synchronize the read operation. In CMOS SRAM, wire delay is not considered, but in QCA SRAM, wire is designed using QCA cells which will increase the latency and size. Area of QCA circuits can be determined using QCA designer tool. The size of the one-bit memory cell, including the control

circuit is 0.17 μm^2 and the size of 64-bit memory array including the control circuit is 13.6 μm^2.The QCA layout of 64-bit SRAM is shown in Fig. 5. Table III lists the performance of the proposed one-bit memory cell, 4X4 and 8X8 memory arrays. It has been observed that the higher order memory arrays occupies less area and complete the process in less number of clock cycles because of sharing the control circuit. The performance of the one-bit cell is compared with the best published works and is listed in Table IV. The proposed one-bit memory cell occupies less area, realized by less number of cell count and reduced clock cycles to complete the operation than the existing works. Table IV shows the comparison of 1-bit QCA SRAM with 6T SRAM using CMOS technology.

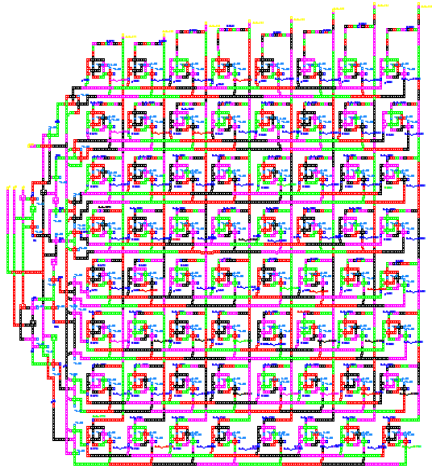

Fig. 5: QCA Layout of 64-bit SRAM.

The inverted and non inverted signals are obtained using coplanar wire crossing option which is shown in Table II and its QCA layout is displayed in Fig. 6.

Table II: Coplanar Wire Crossing.

Data in	Data out
X1	X1
Y1	~Y1
X2	X2
Y2	Y2

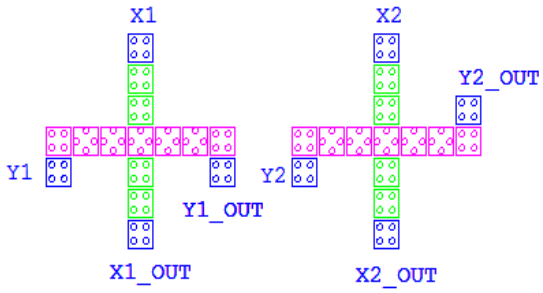

Fig. 6: QCA Coplanar wire crossing.

Table III: Performance Of The Proposed Work.

Size	Performance metrics				
	Architecture	*Complexity*	*Cell count*	*Area (μm^2)*	*Clock cycle*
Proposed work one-bit (dia=18nm)	Multiplexer-based parallel memory	Simple read/write operations	104	0.17	1.5 (6 clock zones)
Proposed work (4x4 Par) (dia=18)	Multiplexer-based parallel memory	Simple read/write operations	2862	6.31	3 (11 clock zones)
Proposed work (8x8 Par) (dia=18)	Multiplexer-based parallel memory	Simple read/write operations	9264	13.6	5 (21 clock zones)

Simulation Results:

Fig. 7(a) shows the number of memory bits Vs QCA cells. It has been observed that the QCA cell count including control circuits is linearly varies with respect to number of memory bits. Fig. 7(b) shows plot of memory Vs Clock delay. The clock delay is specified in terms of clock zones i.e one clock delay is equal to four clock zones. It reveals that the clock delay is almost varies linearly for higher order bits and it is a sharp curve slightly for the lower order memory bits which is obtained due to area of the control circuit. Fig. 7(c) shows the memory bits Vs area. It has been observed that the area of the arrays including control circuits varies linearly with respect to number of memory bits. For bistable approximation and coherence vector engine, the clock low and clock high is defined $9.800000e^{-22}$s and $3.800000e^{-23}$s respectively.

Table IV: comparison of proposed work with best published works.

Comparisons	Performance metrics				
	Architecture	Complexity	Cell count	Area (μm^2)	Clock cycle
K. Walus (one– bit) [11]	Parallel memory	Complex circuitry	181	0.29	8
Vankamamidi (one-bit) [12]	Line-Based parallel memory	Complex read/write circuitry	158	unknown	unknown
Vankamamidi (one - bit) [16]	Tile-based serial memory	Complex input-output tiles	152	unknown	unknown
Moein Kianpour (one-bit)(dia=10nm) [17]	Loop-based parallel memory	Simplified control circuit	140	0.25	2
Proposed work one-bit (dia=18nm)	Multiplexer-based parallel memory	Simple read/write operations	104	0.17	1.5 (6 clock zones)

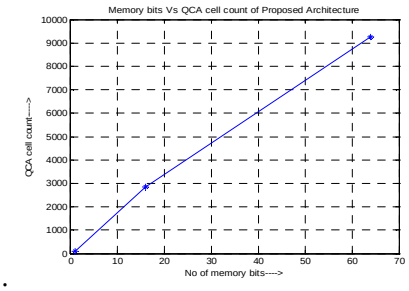

Fig. 7: (a) Number of memory bits Vs cell count.

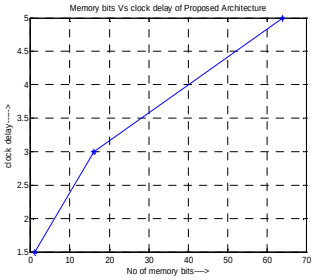

Fig. 7: (b). Number of memory bits Vs delay.

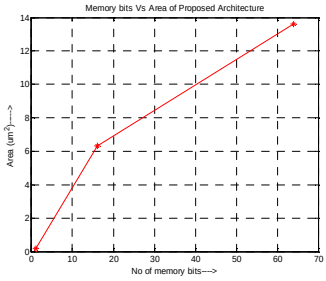

Fig. 7: (c) Number of memory bits Vs area.

The simulation result of 1-bit memory is displayed in Fig. 8. It can be inferred from Table-V that the proposed QCA memory cell occupies much lesser area than other Conventional SRAM designs. The speed of QCA is high compared to the conventional SRAMs. The Simulation result of coplanar wire crossing is shown in Fig. 9. In the Fig. 6, there is no change in electron flow direction hence the out coming signal is not inverted. If the QCA cell is placed in such a way that the electron flow direction gets changed then the signal is inverted.

Conclusion:

The 64-bit Parallel memory architecture is designed efficiently using multiplexer-based memory loop. It reduces the cell count, and area considerably. The speed has been increased due to reduced clock cyle in mulplexer-based memory loop. A simple control algorithm is developed to synchnonize read write memory operations. The higher oder 64x64 bit SRAM will be developed in future using different methods of cross over options by increasing temperature stabilty.

Table V: Comparison Of 1-Bit Qca Sram With 6t Sram Using Cmos Technology.

Parameters	Proposed 1-bit QCA memory cell (including R/W control circuit)	6T SRAM using CMOS Technology				
		0.25 um [18]	0.18 um [19]	65 nm [20]	40 nm [20]	32nm [20]
Area	0.17um^2	2.4x4.1 um^2	5.59 um^2	0.4 um^2	0.33 um^2	0.124 um^2
Clock delay	1.5 clock cycle	1.8 ns	1.8ns	-	-	-

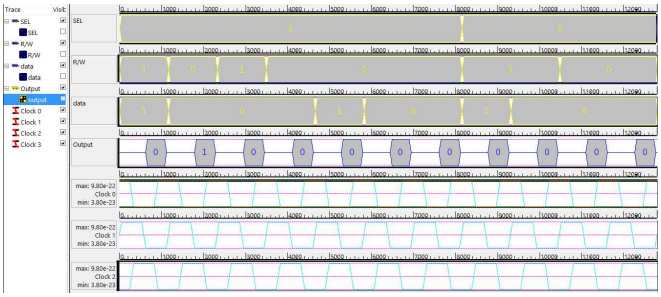

Fig. 8: Simulation results of 1-bit memory cell.

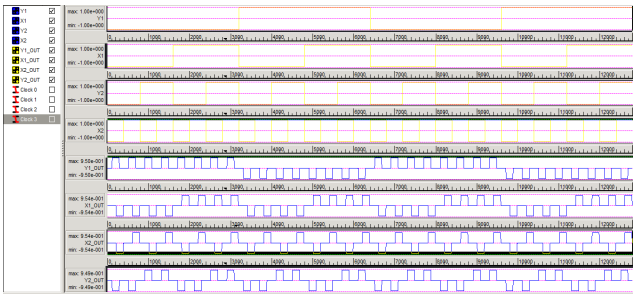

Fig. 9: Simulation results of coplanar wire crossing.

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