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All Digital Phase Locked Loop Architecture Design Using Vernier Delay Time-to-Digital Converter

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ABSTRACT

In this paper, we propose a low power All Digital Phase Locked Loop with a wide input range. The Three Step TDC consumes more power which cannot be used in many applications. Hence a method has been proposed which replaces Three Step TDC by Vernier Delay TDC which consumes less power. The blocks were implemented using Tanner EDA Tool under 130nm technology which drives the entire architecture to consume a power of 8.68mW which is 1.7799 times smaller than the original value with the power supply of 1.8V and the output frequency is 10MHz.

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INTRODUCTION

An All-Digital Phase Locked Loop (ADPLL) is a Phase locked loop implemented only by digital blocks. The signal are digital (binary) and the signal may be either in single or combination of parallel digital signals. The phase locked loop is used in many applications such as digital communications for FSK decoder, wideband frequency tracking, and mobile phone applications for frequency matching.

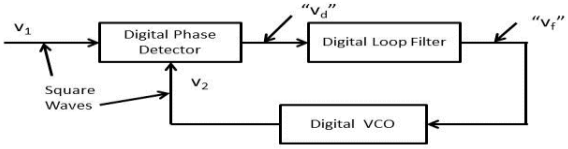

Fig.1: General Block diagram for All Digital Phase Locked Loop.

The block diagram for All digital Phase Locked Loop (ADPLL) is shown in Figure.1 consist of digital phase detector, digital loop filter and digital VCO. The Digital phase detector compares the square waves of input signal 'V_1' and output from Digital VCO as 'V_2'. The output from digital phase detector is given to digital loop filter which is used to reduce the noise of the compared signal. Finally the values are passed to Digital VCO which is the combination of both Voltage controlled Oscillator and the Digital-to-Analog Converter for wide frequency range and it is flexible (KUSUM LATA AND MANOJ KUMAR, 2013).

In the existing system, the Three step Time-to-Digital Converter (TDC) was used. Generally the Time-to-Digital Converter (TDC) refers to translating the time interval into voltage and voltage to digital values. The Three step (TDC) consist of 1st coarse TDC, the 2nd coarse TDC, and the fine TDC with a phase interpolator and a Time Amplifier (YOUNG GUN PU, 2011). The fine TDC uses thermometer-to-binary for accurate resolution. This Three step TDC alone consumes more power which is 11.0509mW. So the overall power consumption for entire architecture will be 15.449mW by using the power formula.

$$Power\ Consumption = V_{DD} \times \int_0^T I_{DD}\, dx \qquad (1)$$

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If Three step TDC is replaced by Vernier Delay TDC, the power consumption will be less will be shown below. The paper is divided in the several sections as follows: Section II shows the architecture of ADPLL and operation of proposed Vernier Delay TDC Section III shows the Experimental works. Section IV provides the conclusion and finally the last section V describes the References.

2, *Proposed System:*

The block diagram for proposed system has been shown in Figure.2. It consist of Phase Frequency detector, Ex-OR Gate, Vernier Delay TDC, TDC Control, Digital Loop Filter, Sigma Delta Modulator, Digitally Controlled Oscillator, Frequency divider. The proposed Vernier Delay TDC is possible for loop structure (JOVANOVIC, G.S. AND M.K. STOJCEV, 2009). The block diagram for individual blocks was explained below.

2.1 Phase Frequency Detector:

The Phase Frequency Detector (PFD) which is also known as Phase Comparator. The structure of PFD is shown in Figure.3. It consist of two edge-triggered D Flip-Flop, AND and OR Gates. If REF value is high, the signal UP goes high making DOWN to fall. When reset is given both UP and DOWN value falls to zero. When OR Gate is inserted into the reset path, Reset_div is set high, both the D Flip-Flops are reset (XIN CHEN, 2011).

2.2 EX-OR gate:

The symbol for XOR gate is shown in Figure 4. The operation for EX-OR gate is, when both the input values either low or high, the output becomes low and if any of the input values either low or high, the output becomes high.

2.3 Vernier Delay TDC:

The Vernier delay line TDC consists of start and stop signal delay lines [3]. The start signal is given as the input to the D Flip-Flop and the stop signal is sent as synchronous clock which determines the propagation timing delay between the adjacent stages. The Vernier Delay TDC is considered to improve the resolution and area and power [5]. The circuit diagram for Vernier Delay TDC is shown in Figure 5.

2.4 Digital Loop Filter:

Digital loop filter Figure 6, is similar operation like Digital inverter. Here it results with the inverted output which leads the input signal to the Digital Controlled Oscillator. RC network at the output maintains the output value at the proper range.

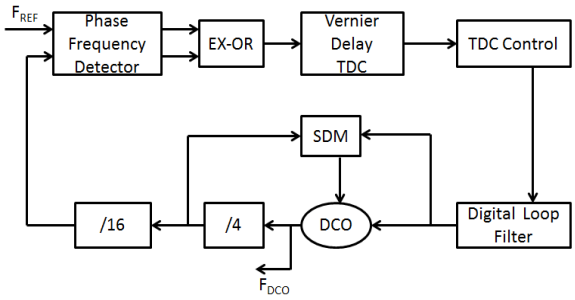

Fig. 2: Block diagram for Proposed ADPLL.

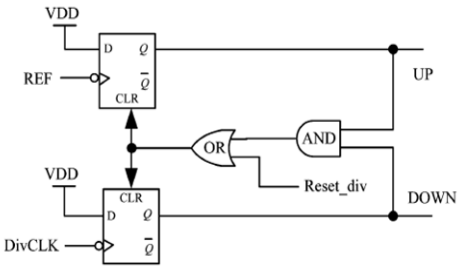

Fig. 3: Circuit Diagram for Phase Frequency Detector.

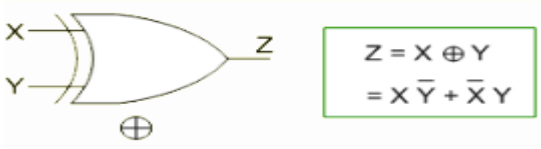

Fig. 4: Symbol for XOR Gate.

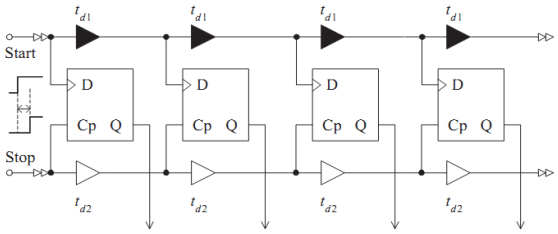

Fig. 5: Circuit Diagram for Vernier Delay TDC.

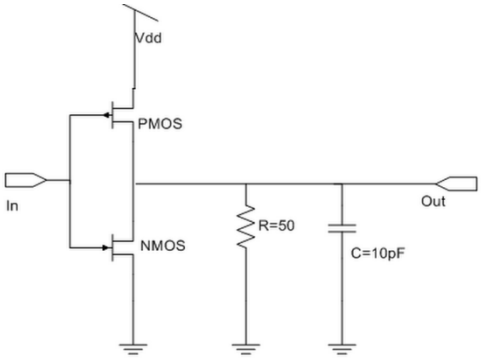

Fig. 6: Circuit Diagram for Digital Loop Filter.

2.5 Digitally Controlled Oscillator:

The digitally controlled oscillator circuit diagram is shown in Figure 7, consist of the ring-type VCO that is odd number of inverters are connected in series will generate five clocks named as CLK[0]-CLK respectively. The delay is controlled at each stage by using digital signals. The delay cells keep the output level low. Thus, the voltage will control the frequency of VCO, when the Signal Run is low level. So the current increases if the voltage increases and decreases the delay cell's delay time thus increase the VCO's frequency

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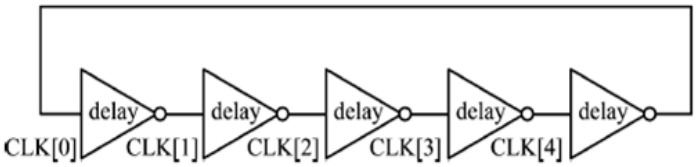

Fig. 7: Circuit Diagram for Digitally Controlled Oscillator.

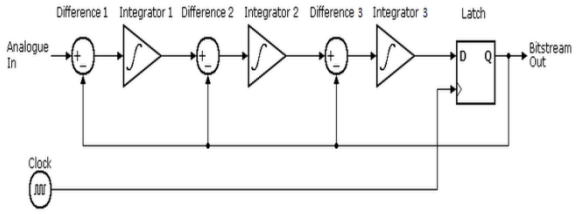

Fig. 8: Circuit Diagram for Sigma Delta Modulator.

2.6 Sigma Delta Modulator

The Sigma Delta Modulator (SDM) circuit diagram is shown in Figure 8, consist of accumulators and comparator. In this the integrator will act as a D Flip-Flop and operates by means of a digital signal.

2.7 Frequency Divider:

The frequency divider circuit diagram is shown in Figure 9, the output depends on clock signal and it gets divided based on the divider.

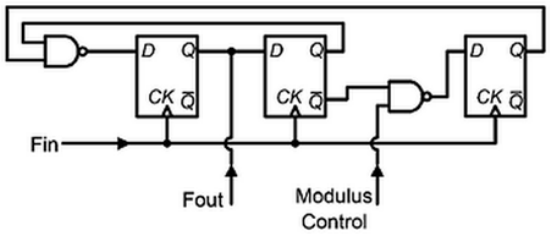

Fig. 9: Circuit Diagram for Frequency Divider.

3, *Experimental Results:*

3.1 Implementation:

In back end, Tanner Version 7 uses 180nm Technology for measuring the Power and Output Frequency. The input applied voltage is 1.8V. The power and Frequency Calculation are shown below. The Figure.10 shows the circuit diagram for Overall Block diagram and comparison chart for existing and proposed is shown in Figure 11. And the comparison result for various performances for existing and proposed is shown in table 1.

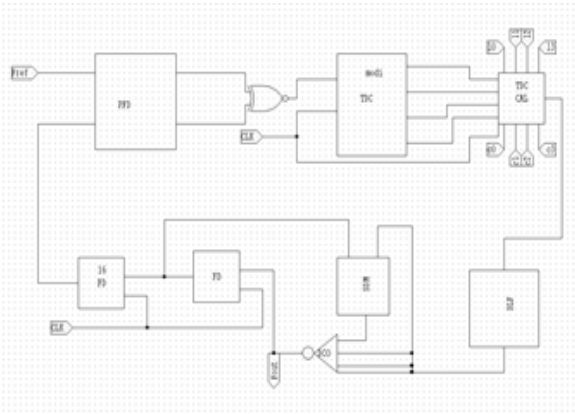

Fig. 10: Circuit Diagram for Overall Block Diagram.

3.2 Power Calculation:

$$Power\ Consumption = V_{DD} \times \int_0^T I_{DD}\, dx$$

Where T = Time
V_{DD} = Voltage Supply
I_{DD} = Current Supply
To apply
V_{DD} = 1.8V and
T = 50 Seconds
To Find I_{DD}

$$P = VI$$

$$I = \frac{P(Maximum\ Power)}{V}$$

$$I = \frac{8.68800 \times 10^{-3}}{1.8}$$

$$I = 4.822mA$$

$$Power\ Consumption = 1.8 \times \int_0^{50} 4.822 \times 10^{-3}\, dx$$

$$= 1.8 \times 4.822 \times 10^{-3}$$
$$= 8.68 \times 10^{-3} W$$
$$= 8.68mW$$

Frequency Calculation:

$$Frequency(f) = \frac{1}{T}$$

Where $T=T_{ON}+T_{OFF}$
$T_{ON} = 5\mu s$
$T_{OFF} = 5\mu s$
$T=10\ \mu s$

$$f = \frac{1}{10\mu s}$$

$$f = 10MHz$$

The Power Consumed by the overall architecture is $8.68mW$ and the Output Frequency is obtained by $10MHz$.

Conclusion:

ADPLL has been designed using Tanner EDA tool implemented with 180nm technology with the supply voltage of 1.8V. Existing ADPLL used Three Step TDC which consumes the power of 11.0509mW. The entire Architecture had driven the power consumption of 15.4499mW. The proposed ADPLL used Vernier Delay TDC which consumes the power of 2.6166mW. Hence, the overall architecture power consumption is 8.68mW. Compared with existing architecture, the proposed

architecture occupies less area because when the switching activity increases. And hence it can be used for mobile applications for frequency matching.

Table 1: Summary of measured performance.

Reference	Existing work	Proposed Work
Technology	180nm	180nm
Output Frequency	10 MHz	10 MHz
Output power	15.4499mW	8.68006mW
Minimum Power	0	4.6533mW
Maximum Power	15.44mW	8.68mW
Power Delay product (PDP)	0.6180µW	0.043452µW
Energy Delay Product(EDP)	24.704pW	0.0021701pW

In table 1, the maximum power and minimum power values are showed.

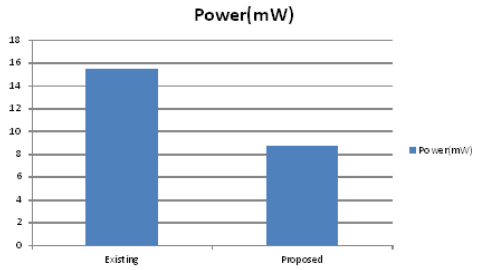

Fig. 11: Comparison Chart.

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