

Low Power CAM based on Synchronous Control Mechanism

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ABSTRACT

Content Addressable Memories (CAMs) are mainly employed for quick packet forwarding and packet classification in switches and routers when transmitting data over network. However, architecture level techniques as well as technology scaling are decreasing the dynamic power of CAMs. This enables the need for a power consumption minimization technique for Content Addressable Memories. This report presents a technique to reduce the power consumption in CAMs without affecting the speed of operation. The circuits are analyzed and the trade-offs are presented using the power reduction technique by implementing in the Tanner tool. As, a design example, CAM is implemented and evaluated by Tanner simulation under a 130nm CMOS technology. The obtained simulation results show a significant amount of reduction in the power consumption for the word circuit block operation of CAM.

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INTRODUCTION

Content-Addressable Memories (CAMs) are used in high speed search engines that are much faster than other approaches utilized for search-exhaustive applications. There are two basic types of CAM: Binary CAM (BCAM) and Ternary CAM (TCAM). Binary CAMs maintain storage and penetration of binary bits, it allows only zero or one (0,1). The

TCAMs are capable of storing and searching ternary states ('0', '1', and 'X'). The 'X' state is used as a wild card state in case of search operation. An input search word is compared with a table of stored words and the matching word is obtained at high speed through a parallel equality search.

However, the area and power of a CAM are the main factor for speedy approach at the cost of augmented silicon area, the designers are struggling to reduce these two parameters. As CAM applications widen, demanding larger CAM sizes, the power difficulty is further exacerbated. Diminishing power utilization, without sacrificing speed or area, is the most important thread of recent research in huge capacity CAMs. In this paper, a Synchronous control based power reduction scheme for increasing the throughput and reducing the energy of the CAM is introduced. In a CAM, most mismatches can be found by investigating a few

given bits with the stored word of the circuit.

CAMs often contain a few hundred to 32 K entries for network routers. Each input-search bit is compared with its CAM-cell bit and the comparison result determines whether a pass transistor in the CAM cell attached to the match line (ML) of a word circuit is in on or off states. CAM cells are classified into two types: NOR and NAND. A NAND-type word circuit operates at medium speed because pass transistors are connected serially between a ML to a ground line. Because very few matched word circuits discharge their ML capacitances, a NAND-type word circuit reduces the power dissipation of MLs compared to the NOR-type word circuit.

This paper presents a discharge processing and Pai-Sigma match line based synchronous control circuits in order to reduce the search power of CAMs. The proposed methodology can overcome from the issues such as charge sharing and short circuit current. The remainder of this paper is sorted as follows. Section 2 describes the basics and operation of Content Addressable Memory. Section 3 discusses the power reduction techniques of BCAMs based on discharge processing. Section 4 presents the architecture of the proposed Pai Sigma match line based on synchronous CAM circuits. Section 5 deals with the simulation results and inference. Finally, Section 6 concludes the paper with highlights and future scope of the work.

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Basics of content addressable memory:

Figure 1 shows the block diagram of a CAM. A search word is broadcasted onto Search Lines (SLs) to the table of stored words whose sizes are of n bits. The amount of bits in a CAM word circuit typically sorts from 36 to 144 bits. A typical CAM utilizes a table size sorting between a small amount of hundred

entries to 32 K entries. Each word block has a match line (ML) that indicates whether search and stored words are the same or different. The outputs from the word blocks are given to an encoder that produces a binary match location i.e., 0 or 1 corresponding to the ML that is in the match state.

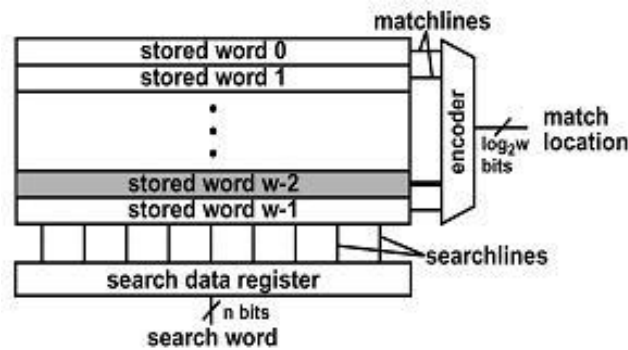


Fig.1: Block diagram of Content Addressable Memory (CAM).

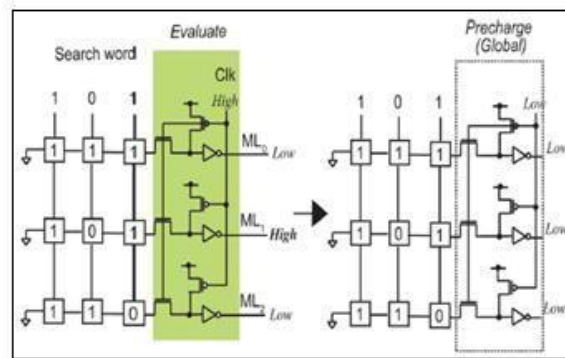


Fig. 2: Synchronous Control based CAM word circuit operations.

The storage and comparison are performed in the CAM core cells circuitry. The search lines of the CAM run vertically in the figure and transmit the search data to the CAM cells. The match lines run parallelly across the array and designate whether the explore data contest the row's word. If a match line is activated it indicates a match and if it is deactivated match line show a non-match process, called a mismatch.

The search operation in the CAM starts with precharging all match lines high, putting them all provisionally in the match state. Then, the search line constrains broadcast the search data. Next, every CAM core cell search the given data into the stored data. If the search data is matched with the stored data then the match line remains high, if it is mismatched with the data then the match line low. The entire results pulls down the match lines for any given word that has a minimum of one mismatch. The match lines of the matched data in the cell remain high, indicating a match, while the other match lines in the cell discharge the match line to ground, reporting a mismatch operation. At last, the

encoder produces the location of search address of the contesting data.

Binary cam word circuit based on synchronous control:

A CAM is a search memory that executes the lookup-table operation utilizing devoted comparison circuitry within a single clock cycle. The CAM word circuit is designed based on dynamic logic that contains evaluate and precharge phases. It is normally used in a CAM to reduce its area. Once a search word matches a stored word in an evaluate phase, the ML of the word circuit needs to be precharged before the next-word search. In a synchronous CAM, all word circuits are controlled by a global clock signal and hence they periodically operate using two phases. As each word circuit is dependently controlled using its global control signal, unused word circuits are on the evaluate phase, while the others are on the precharge phase. In combination with the word overlapped search scheme, input search words match in unused different word circuits whose MLs have already been

pre-charged. Therefore, new search words are immediately processed without wasting the precharge time.

3.1 Synchronous CAM word circuit:

The synchronous circuits operate in two phases: precharge and evaluate, based on dynamic logic. In the precharge phase, the match line in the circuit is charged through the PMOS transistor. In the evaluate phase, the given search word is matched with the stored word while all pass transistors in the CAM cells are in on states. Hence, the match line capacitance is discharged. This process is described

as a “match” operation.

3.2 Modified CAM Clock circuitry:

The block diagrams of a typical word circuit based on a synchronous control for Binary CAM is shown in Figure 3. In synchronous word circuits when controlled by a global clock, its static power dissipation is high. Hence an additional logic block is added to the existing CAM word circuit in order to minimize the static power dissipation. The logic block proposed is added to the existing clock circuitry since they are major source for power control.

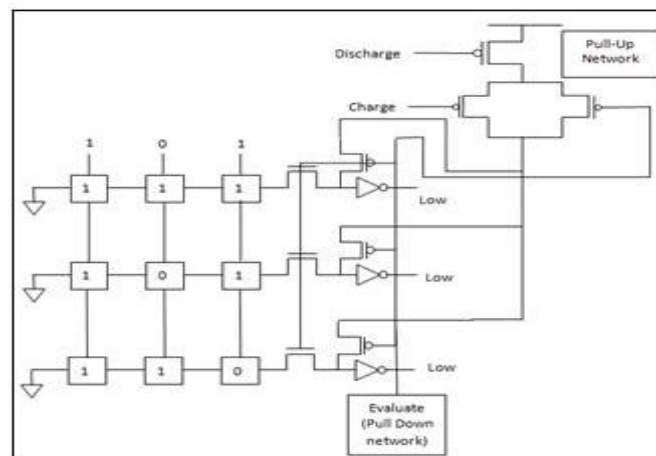


Fig. 3: CAM Word Circuit using Clock Circuitry.

This proposed circuitry has three modes of operation as charging, evaluating and discharging process. Of these, charging and discharging transistors form the pull-up network and evaluate transistors forms the pull-down network. Thus, when the circuit is in match condition, it is connected to evaluate block. Else it is connected to discharge or charging block.

Ternary cam based on synchronous control:

TCAM is used in high-speed parallel search operations leads to very high power consumption. To reduce the power consumption of the CAM word circuit, many methods on low power design of TCAM is accounted. In [8], the authors suggested a current-race match line sensing scheme, it diminish the power consumption by reducing switching activity of the search lines and the voltage swing of the match lines are shrunk. In (Anh-Tuan Do, 2013; Li, 2006), a match line is divided into two parts, the first element is an NAND-type match line and the second element is an NOR-type match line. Similarly, the comparison result of the initial part decides whether the second part is precharged or not. In a ripple-precharge match line scheme which is similar to an NAND-NOR match line scheme was recommended to diminish the power dissipation of a TCAM.

To attain the concession between the power and the delay of a match line (Anh-Tuan Do, 2013; Li, 2006; Pagiamtzis, 2006) by using the Hybrid NAND-NOR match line is one preferred design approach. If the CAM executes a Compare operation, all the NAND type match lines are activated. But, only the NOR type match lines with the corresponding NAND match lines which produces a match result is activated. Since the switching activity of the NAND match line is minimized and only a little amount of NOR type match lines is getting activated, the power required for compare operation of the CAM with NAND-NOR match lines can radically be diminished.

In addition to, the delay of the NAND-NOR match line is very much improved than that of the NAND match line. Hence the major disadvantages of the NAND/NOR match line structures 1) the match line acquires short circuit current (ie., DC current), it is due to the search results of NAND and NOR match lines are match and miss, 2) the problem of charge sharing exist in the NAND type match line process when the result of the search operation of NAND match lines are in mismatch state. The problem of charge sharing is reduced by the search lines should be precharged to V_{dd} when the NAND match line executes the precharge operation. The results of this technique increase the power

dissipation of the search lines.

4.1 Pai-Sigma match line:

Figure 4 shows the transistor-level diagram of the proposed Pai-Sigma match line scheme. The pai sigma match line reduces the problems in the NAND

and NOR type TCAM cells. The pai segment utilizes the NAND function and the sigma segment utilizes the NOR function. Then the two segments are combined with the interface logic block between the pai and sigma segment

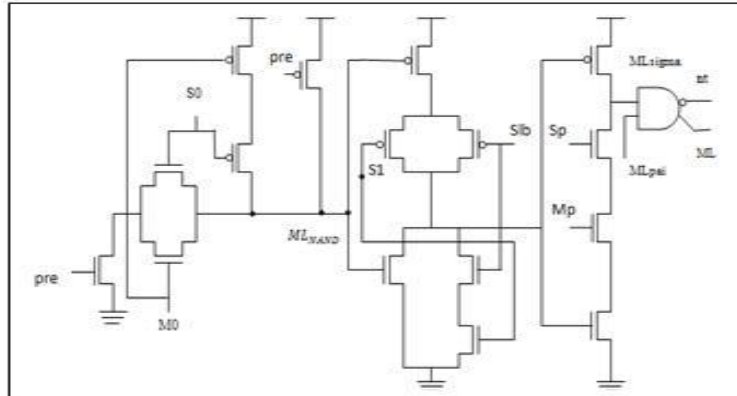


Fig. 4: Structure of Pai-Sigma Match line Scheme.

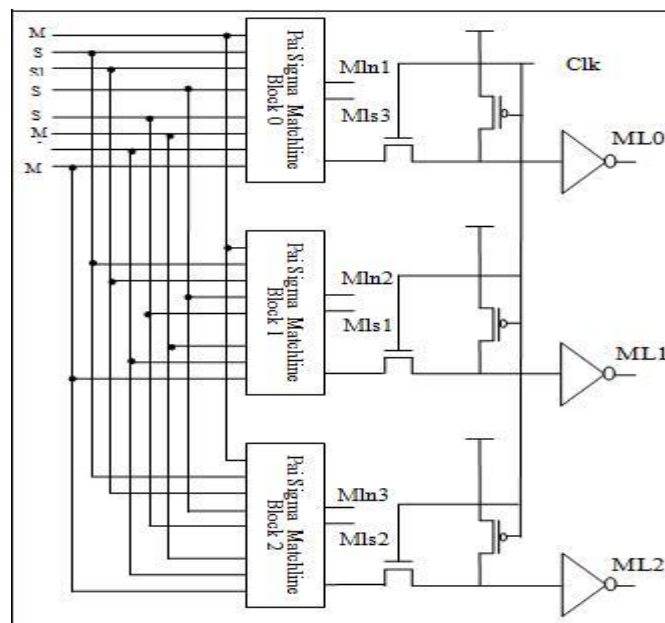


Fig. 5: Synchronous word circuit based on Pai-Sigma matchline.

In the Precharge phase, the signal pre turns out to be low (i.e., pre=0) all the internal nodes of the circuit between the logic can be charged to V_{dd} or $V_{dd}-V_t$. If $(S_i, M_i) = (1,1), (0,1), (1,0)$ then the internal nodes $I_{i+1}=I_i$. Suppose the signal $(S_i, M_i) = (0, 0)$, then the pMOS transistors controlled by S_i and M_i turn on the internal nodes and precharged to logic 1. Hence the search lines of the cells in the pai segment not need to be reset to assure the all internal nodes is precharged to logic 1 and also the ML_{NAND} is precharged to logic 1 through pMOS transistor. This can eliminate the problem of short circuit current in the interface logic and the dynamic power. In the evaluate phase (pre = 1), both S_i and M_i of the pai

segment are not logic 0. If any of the S_i and M_i goes to logic, i.e., the search result is mismatch, then the corresponding pMOS transistors are turned on and the internal nodes I_{i+1} are precharged to logic 1. Hence, it is propagated to the consecutive internal nodes through the nMOS transistor.

The interface logic uses the static CMOS gate to cascade the NAND and the NOR match line to eliminate charge sharing. The input to the static CMOS gate depends on the S_i, M_i and ML_{NAND} . Therefore, if the search result of the cell in the pai segment is in match, then the interface logic produces logic 1 at ML_{pai} node. Then, the precharged pMOS of the NOR match line will be turned off. The

short circuit path does not exist, If the search result of NOR match line is miss. The final result of the match line (ML) is active, when the ML_{pai} and the ML_{sigma} produces logic 1.

4.2 Synchronous control based on Pai-Sigma Match line:

Figure 5 illustrates the block diagram of synchronous word circuits based on the pai-sigma match line scheme. Here, the global clock signal is used to control the Synchronous word circuit.

In the precharge phase, all match lines are charged and the inverter output goes to be low. In the evaluate phase, simply a matched word circuit discharges the match line capacitance and then the output of the inverter turn out to be high. All the match lines are charged for every precharge phase.

Results and inference:

In the content addressable memory, the select line is used to select the bit according to the input given to the memory. The output will depend on the

match line. Tanner EDA is to design the memory whereas the output waveform, power, leakage current are determined using T-Spice. Table I summarizes the comparison results of the low-power CAM based on synchronous control. The low-power CAMs reported are designed for specific applications. Thus, specific low-power design techniques can be utilized to diminish the search energy.

The performance parameters are calculated in order to determine the efficiency of CAM. The average power is obtained from the total power consumed by the circuit. The static power and static current which are the power consumed and current drawn because of the switching activities in CAM. The area represents the space occupied by the transistors in CAM. Energy Delay Product (EDP) represents the product of static power and square of the time required for operation of CAM. Power Delay Product (PDP) represents the product of static power and time required for operation of CAM.

Table I: Comparison of Power results of Existing Vs Proposed methods.

Performance	Synchronous	Low power Binary CAM based on	Low power Ternary CAM based on
Parameters	Control	Synchronous Control	Synchronous Control
Average power (microwatts)	480	91	0.4
Static power (milliwatts)	4.5	0.09	7.6
Static current (milli Amps)	2.5	0.05	4.2
Area (μm^2)	712.5	730.5	487.5
EDP (picowatt (sec) ²)	0.05	0.009	0.00002
PDP (microwatt sec)	0.005	0.0009	0.1

The performance parameters are obtained from the static power and dynamic power displayed in the power results window in Tanner tool. The time considered for calculation is the time taken for the specific power consumption. Some of the parameters are maintained with the default value when tanner tool is considered. For static current calculation, the supply voltage is given as 1.8V. For area calculation, the length and width of the transistors are considered to be 2.5u.

Taken into account the synchronous control of the proposed CAM, the average power and static power consumption is minimized. From the comparison table, it can be seen that the power consumption for the proposed CAMs in combination with synchronous control dissipates less power when compared to the existing CAM in combination with synchronous control.

Conclusion and future work:

In this paper, the design of Binary and Ternary CAMs based on synchronous control is discussed. The search line power being the major source of

power dissipation is greatly minimized with the help of the pai sigma match line scheme and discharge processing scheme. Thus, the proposed low-power CAM is implemented using TSMC 130nm CMOS technology. Results show that the proposed CAM can attain a significant amount of energy reduction compared with the conventional type CAMs.

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