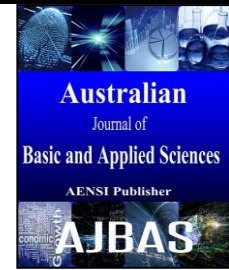




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Analysis of Multilevel Inverter for STATCOM using Fuzzy controller for Power Factor Improvement

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ABSTRACT

This paper proposes a three phase nine level multilevel inverter using reduced switch topology with pulse width modulation (PWM) control scheme. The nine level inverter is used in STATCOM by replacing the inverter in it. When a three phase source is connected to a non-linear load there will be a drop in the output voltage and output current which leads to the reduction in the power factor. Hence the STATCOM with the reduced switch multilevel inverter is used to compensate the drop in the output voltage and output current that increases the power factor. The modulating signal for the PWM inverter in STATCOM is produced from a controller and the K_p and K_i values in it are tuned with the help of fuzzy controller. The total harmonic distortion and the power factor without STATCOM and with STATCOM are discussed in this paper and the improvement in power factor is shown by using the STATCOM compensation.

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INTRODUCTION

Modern power systems are of complex networks, where hundreds of generating stations and thousands of load centres are interconnected through long power transmission and distribution networks. In distribution network sinusoidal voltage is essential, where consumer uses various non - linear, capacitive and inductive loads. Non-linear loads change the shape of the current waveform from a sine wave to some other form and creates harmonic currents in addition to the original (fundamental frequency) AC current that leads to low power factor. Poor load current phase angle is generally the result of an inductive load such as an induction motor, power transformer, welder, lighting ballasts or induction furnace. A poor power factor due to an inductive load can be improved by the addition of power factor correction. A distorted current waveform can be the result of the variable speed drive, switched mode power supply, rectifier, and discharge lighting or other electronic load. The poor power factor due to the distorted current waveform requires a change in equipment design or expensive harmonic filters to gain an appreciable improvement. In reality many inverters are quoted as having a power factor of better than 0.95, the true power factor is between 0.5 and 0.75. The power factor of 0.95 is based on the cosine of the angle between the voltage and current but it does not take

into account that the current waveform is discontinuous and therefore contributes to increased losses on

the supply. This problem can be overcome by some FACTS devices (STATCOM, SVC) that were incorporated in power system but these devices lead to the generation of harmonics due to the power semiconductor devices present in it. The FACTS devices produce output which is not purely sinusoidal and requires large filter in the power system. Multilevel inverters (MLI) produce near sinusoidal output-voltage waveforms and output current with better harmonic profile. Stress on electronic components that decreases voltage is avoided by MLI, switching losses also lower than the conventional two-level inverter, a smaller filter size is required and with lower EMI. These makes multilevel inverter cheaper, lighter, and more compact but as the levels gets increased the usage of the power electronics switches and the separate DC sources gets increased. Thus the reduced switch topology is used to reduce the switches and the DC sources. The reduced switch topology structure for seven level is described in (Nasrudin Rahin, 2011), in this paper the reduced switch topology for nine level is modeled for the STATCOM application. In this paper the STATCOM is used to improve the power factor of the system that is connected with the non-linear load. The voltage source inverter in STATCOM is replaced

by multilevel inverter with reduced switch topology structure using controller with fuzzy logic.

Static synchronous compensator:

Static Synchronous Compensator (STATCOM) is a voltage source converter based FACTS controller. It is a shunt controller mainly used to regulate the voltage by generating/ absorbing the reactive power. The STATCOM consists of a three phase inverter voltage source converter (VSC) using SCR, MOSFETs or IGBT, a D.C voltage for the inverter, a link reactor which links the inverter output to the a.c supply side, and filter components to filter

out the high frequency components due to the PWM inverter. The reactive power is controlled with the magnitude of output voltage of STATCOM and the ac voltage. The real power is controlled with the phase difference between the VSC output voltage and system voltage. The active power flow into the system can be controlled with the control of dc link voltage. The general overview structure of STATCOM is shown in Fig.1. The STATCOM in this paper is used to improve the power factor. The STATCOM is connected with the ac system at the Point of common coupling (PCC).

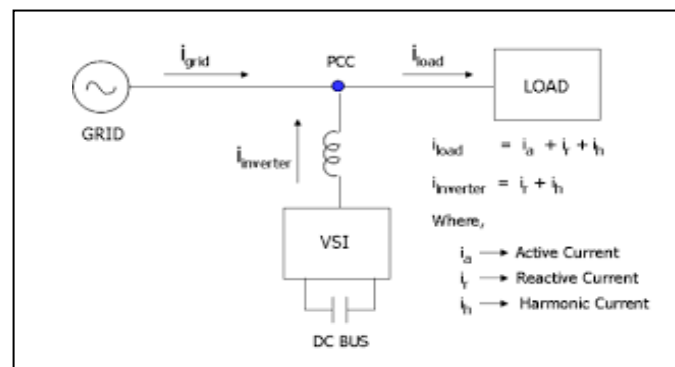


Fig. 1: General structure of STATCOM.

Multilevel inverter with reduced switch topology:

There are three different structures of multilevel inverter namely Diode Clamped MLI, Flying Capacitor MLI and Cascaded H bridge Multilevel Inverter (CHBMLI). These multilevel inverter structures do have some disadvantages. It requires greater number of power semiconductor switches and also it needs separate DC sources. There are many topologies to reduce the switches in the multilevel inverter. The bi-directional switch topology (Nasrudin Rahin, 2011) is considered in this paper

for the reduction of switches. There are three types of bi-directional switch topology such as common collector type, common emitter type and diode bridge topology. In this paper diode-bridge topology is used for the reduction of switches for a nine level inverter, which consists of four diodes that are arranged in the bridge topology in which a switch is placed at the middle of the diode bridge.

Fig.2. represents the reduced switch diode bridge topology for nine level inverter.

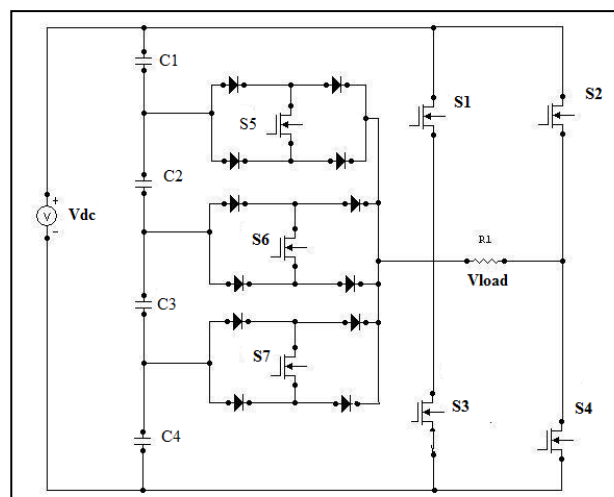


Fig. 2: Reduced switch topology for nine level inverter.

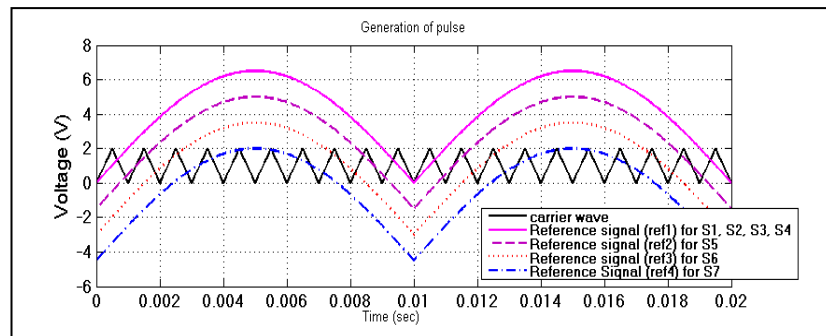


Fig. 3: Single carrier pulse width modulation technique.

The diode bridge topology comprises a conventional H-bridge inverter, bidirectional switches, and also includes a capacitor voltage divider. The number of switches required in the cascaded H Bridge nine level inverter is 16 switches for each phase so totally 48 switches are required for three phase nine level inverter in cascaded form. But the reduced switch topology requires 7 switches per phase so totally 21 switches are required for the three phase nine level inverter using reduced switch topology and also it requires single dc source for each phase compared with four separate dc sources for each phase in CHBMLI. Hence the components get decreased in using the reduced switch topology.

The switches are triggered using single carrier pulse width modulation technique as shown in Fig.3. There are four reference signal compared with one carrier signal to produce the pulse. Each reference signal is in phase with each other and equal in amplitude except with an offset value that is equal in magnitude to the carrier wave. Here ref1 interacts

with carrier signal and produce the pulse1, ref2 interacts with the carrier and produces pulse2, ref3 interacts with the carrier and produces pulse3, ref2 interacts with the carrier and produce the pulse4, and the ref4 interacts with carrier and produces pulse5. The switch S2 and S4 operates at the fundamental frequency. By comparing the pulse1 and 3 produces the pulse to the switch S1, switch S2 operates at fundamental frequency is triggered. The pulse1 and 3 is compared for next positive cycle to produce the pulse for switch S3, then S4 operates at fundamental frequency is triggered. The product of pulse 3 and NOT gated pulse5 is compared with the product of pulse4 and NOT gated pulse1 to produce the pulse for the switch S5 and S7 and the switch S6 is triggered by comparing the pulse2 and NOT gated pulse3. The gate pulses obtained from this pulse width modulation technique is shown in Fig.4. for the seven switches in per phase. The switching sequence of the output voltage is given in Table.I.

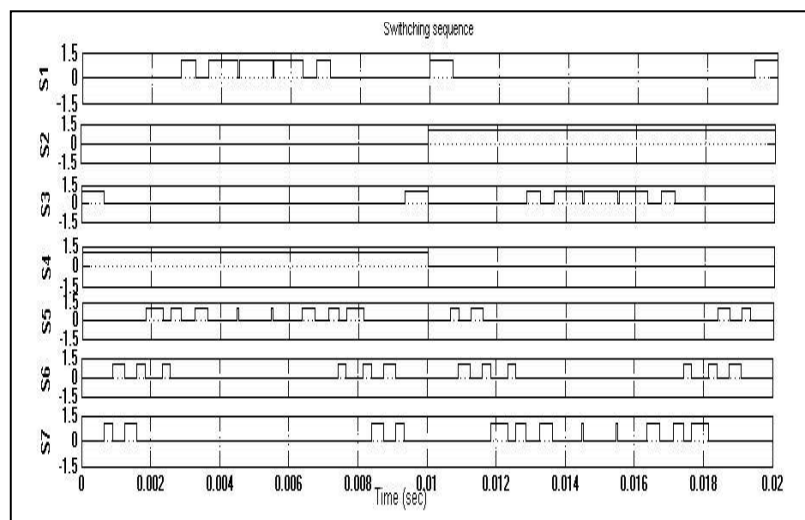
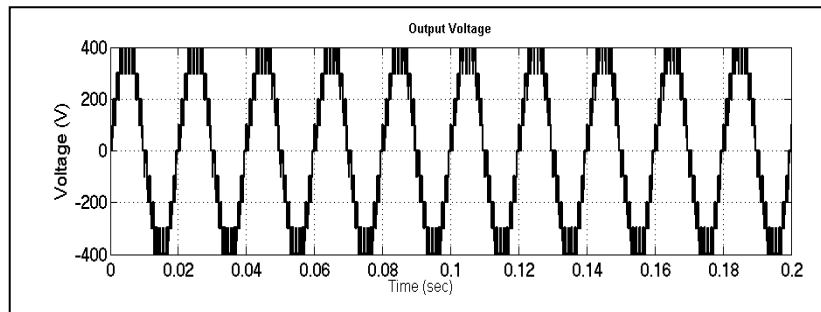
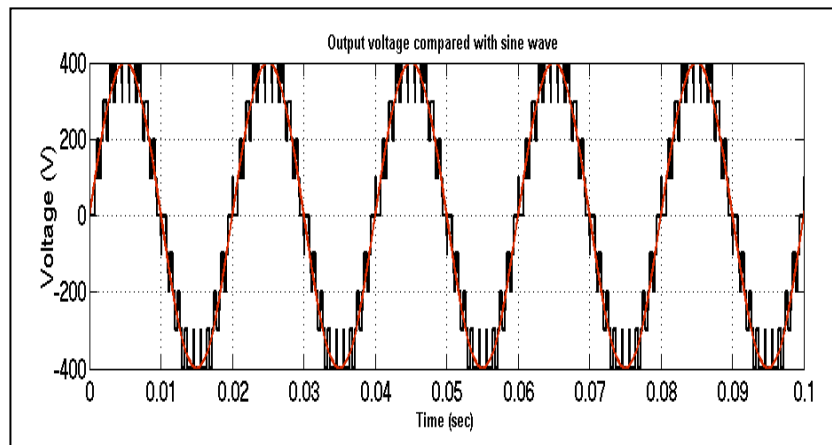


Fig. 4: Switching sequence for nine level inverter.

The output voltage waveform for the nine level inverter with reduced switch structure is shown in Fig.5 and the near sinusoidal waveform in Fig. 6.

Table 1: switching table for reduced switch nine level inverter

Voltages	S1	S2	S3	S4	S5	S6	S7
0V	0	0	1	1	0	0	0
V/4	0	0	0	1	0	0	1
2V/4	0	0	0	1	0	1	0
3V/4	0	0	0	1	1	0	0
4V/4	1	0	0	1	0	0	0
0V	1	1	0	0	0	0	0
-V/4	0	1	0	0	1	0	0
-2V/4	0	1	0	0	0	1	0
-3V/4	0	1	0	0	0	0	1
-4V/4	0	1	1	0	0	0	0

**Fig. 5:** Output voltage for reduced switch nine level inverter.**Fig. 6:** Output voltage compared with sine waveform.**Test system model:**

The simulation analysis is carried out in a system as in Fig.7. that consists of a three phase source of 230 V connected to the RL load along with the non-linear load through the transmission line impedance.

A. Simulation of the system without nonlinear load and without STATCOM

The system is simulated in normal condition

without any nonlinear load. The three phase output voltage and current waveform in this case is shown in Fig.8. There are no harmonics present in the voltage as well as current wave thus the power factor will be 0.9524 because there is no non-linear load connected to the system. When there is no non-linear load connected to the transmission line then there will not be any drop in the output voltage and the current waveform. Hence it produces pure sinusoidal output voltage and current waveform.

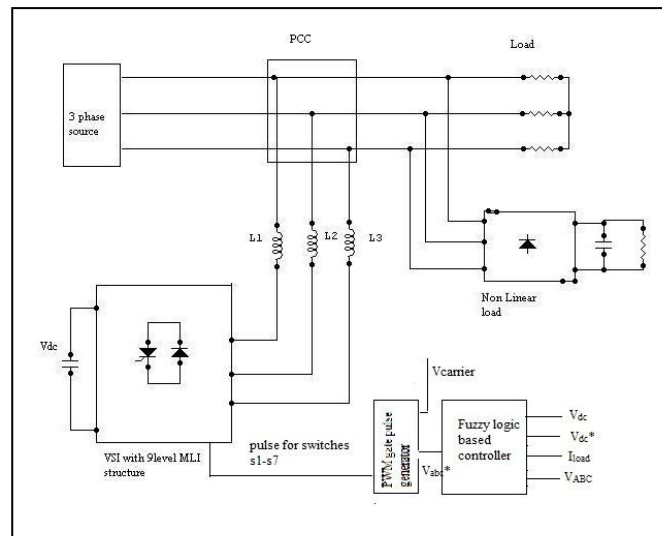


Fig. 7: Test system model.

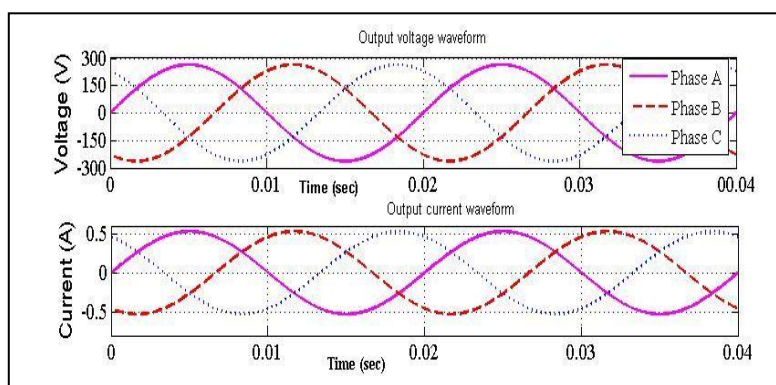


Fig. 8: Waveform for output voltage and current without nonlinear load.

B. Simulation of the system with nonlinear load and without STATCOM:

The system is simulated with the non-linear load without STATCOM compensation this leads to distorted current waveform that reduces the power factor. Here the rectifier load is used as the non-linear load.

Fig.9.shows the three phase output voltage and current waveform when the system is connected with the non-linear load. The power factor decreases due

to the usage of the non-linear load leads to discontinuous and distorted current waveform. Here the rectifier is used as a non-linear load which produces 0.7853 as power factor without the STATCOM compensation in the transmission line.

Fig.10 represents the THD analysis of the system with non-linear load without the STATCOM compensation. The THD produced for the output voltage waveform when a non-linear load connected to the source without any compensation is 6.43%.

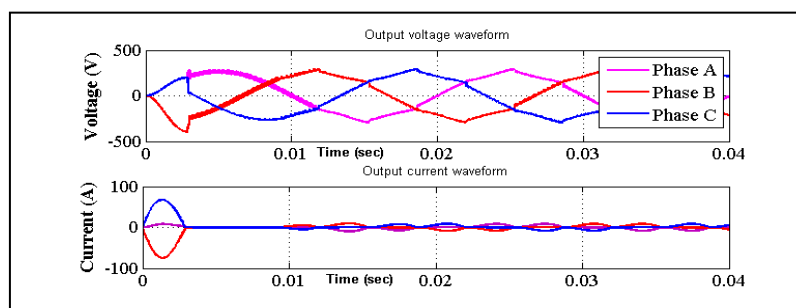


Fig. 9: Output voltage and current waveform with nonlinear load.

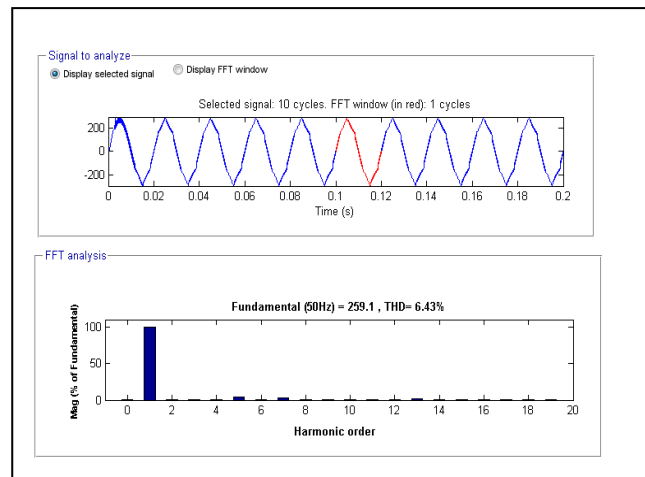


Fig. 10: THD analysis for the nonlinear load system without compensation.

Simulation of non-linear load with statcom:

Fig.11. shows the simulation block of the system compensated by the STATCOM when it is connected to the non- linear load where the STATCOM is used for improving the power factor with the help of the

controller using the fuzzy logic. Fig.12 shows the waveform for the modulating signal of the PWM modulation technique and Fig.13 shows the voltage waveform of the inverter connected to the transmission line.

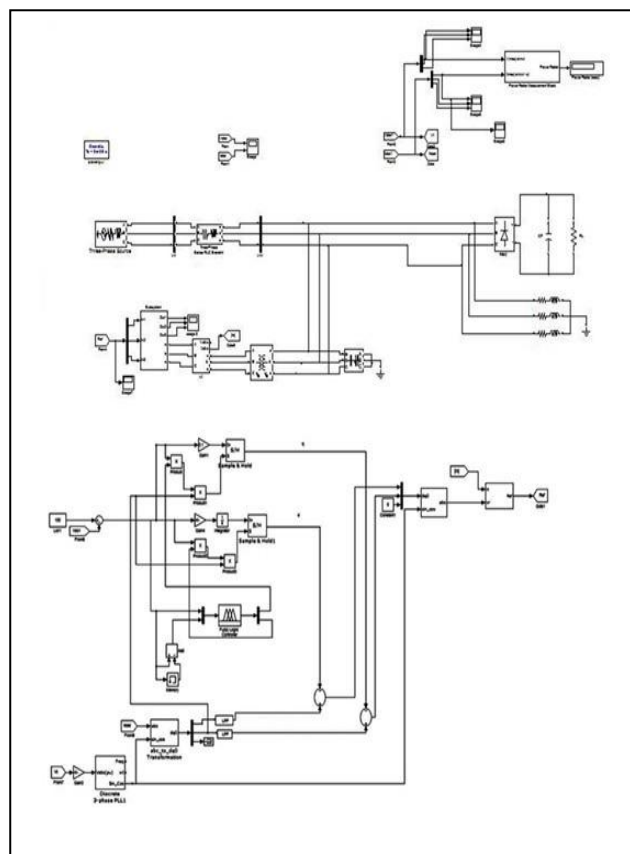


Fig. 11: Simulation block of the system with nonlinear load with STATCOM.

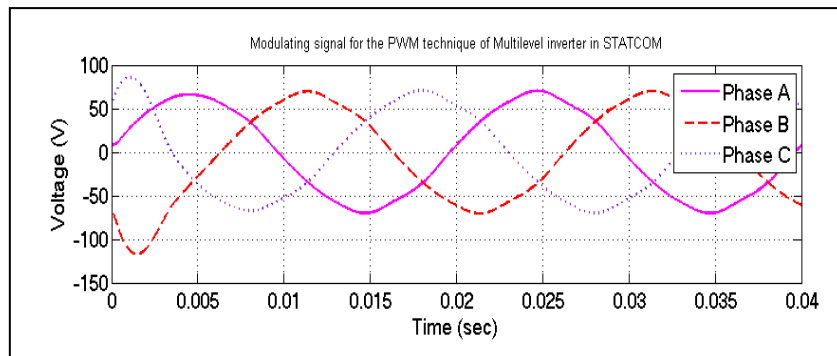


Fig. 12: Modulating signal for the PWM inverter.

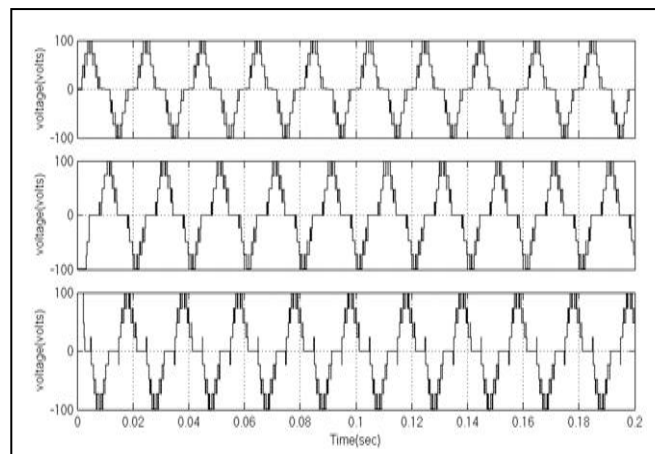


Fig. 13: Voltage waveform from the inverter connected to the transmission line.

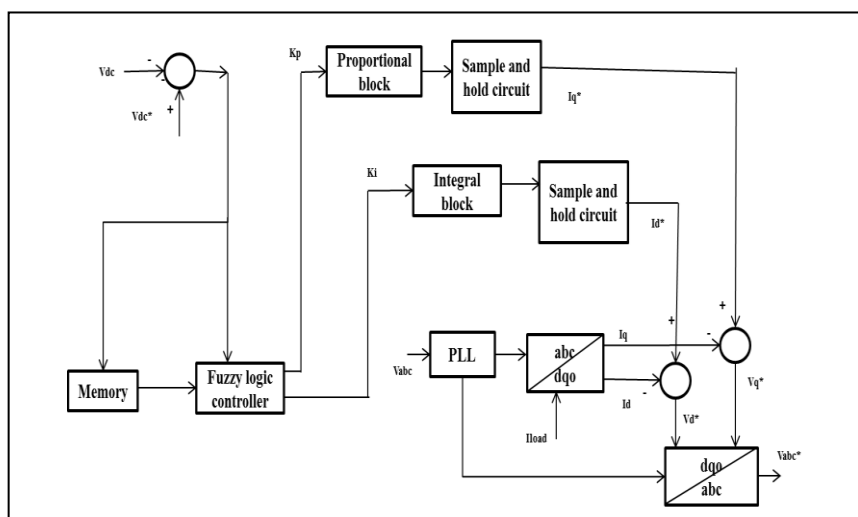


Fig. 14: Block diagram of Fuzzy controller.

Fuzzy controller:

Fig.14. shows the control block for the STATCOM. The dc voltage V_{dc} is compared with the reference voltage V_{dc}^* , produces the error signal that is given to the proportional gain K_p block and integral gain K_i block. The K_p , K_i values are given to the sample and hold circuit block which produces the I_q^* and I_d^* . The controller using fuzzy logic takes the

input from the error produced by the dc voltage and the previous error stored in the memory. The K_p , K_i values are tuned from the fuzzy controller with the help of error and the change in error of the dc voltage. It is tuned to inject the decreased amount of current when using the non-linear load to improve the power factor. The V_{ABC} is given to the phase locked loop to give the reference angle for the abc-

dq0 block; the I_{load} is transformed to I_q , I_d with the abc-dq0 transformation. The I_q^* , I_d^* and I_q , I_d compared and produces V_q^* , V_d^* . Finally the dq0-abc transformation is done to get the respective voltage V_{abc}^* is given as the modulating signal for the inverter.

The inputs of the fuzzy controller are given by

$$Err = V_{dc}^* - V_{dc}$$

$$derr = err(\text{present}) - err(\text{previous})$$

The output of fuzzy controller given by

$$K_p = K_{p,ref} + \Delta K_p$$

$$K_i = K_{i,ref} + \Delta K_i$$

Fuzzification:

The fuzzification interface modifies the inputs to a form in which they can be used by the inference mechanism. It takes in the crisp input signals and assigns a membership value to the membership

function. Typical input membership functions used here is in triangular form. Five triangular membership functions have been chosen: NB (Negative Big), NS (Negative Small), Z (Zero), PS (Positive Small), and PL (Positive Big) for both error (err) and change in error (derr). Each membership function has a membership value belonging to [0, 1]. It can be observed that for any value of error or change in error, either one or two membership functions will be active for each.

Inference Mechanism:

Fig.15 shows the fuzzy logic controller design block in MATLAB. Fig.16 and Fig.17 shows the membership function for error input and change in error. The error input is PB (positive Big); change in error is PS (positive Small).

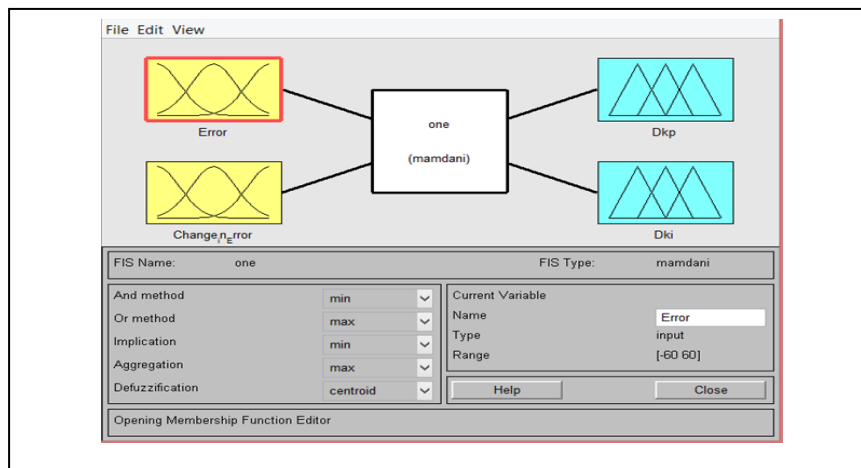


Fig. 15: MATLAB fuzzy logic controller design.

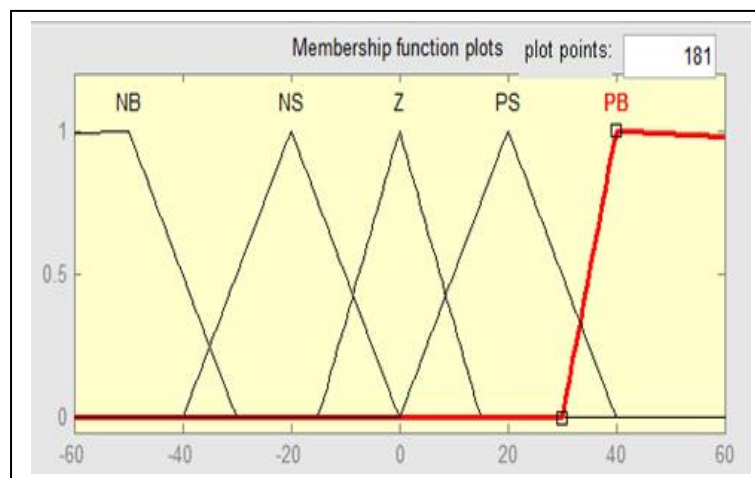


Fig. 16: Membership functions for error input.

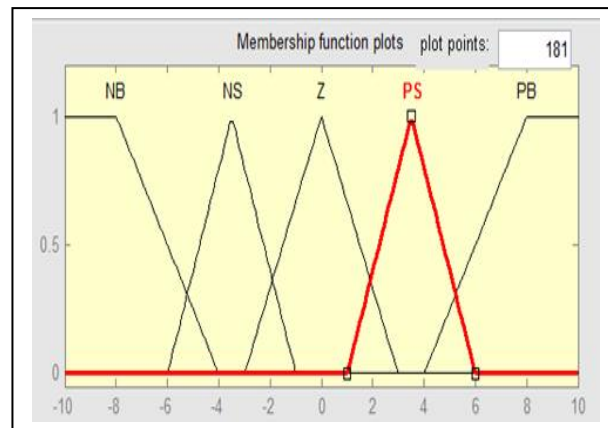


Fig. 17: Membership functions for change in error.

The rule base:

The rule based is used to set the membership function for the error and the change in error and also

to obtain the respective k_p and k_i values. The Table II and III represent the rule base for the k_p and k_i values depending on the error and the change in error.

Table 2: Rule base matrix for change in k_p .

Error(err)	NB	NS	Z	PS	PB
Change in error(derr)					
NB	NB	NS	NB	NS	PB
NS	NS	NB	Z	PB	Z
Z	NB	Z	NB	NS	NB
PS	NS	PB	PS	NB	PS
PB	PB	NS	Z	PS	NB

Table 3: Rule base matrix for change in k_i .

Error(err)	NB	NS	Z	PS	PB
Change in error(derr)					
NB	PB	NB	NB	NS	NB
NS	NS	PB	Z	NB	Z
Z	NB	Z	NB	NB	PB
PS	NS	NB	PS	PB	NS
PB	NB	NS	PB	PB	PB

Defuzzification:

The centroid method has been used for the defuzzification method. If we use this method, the resultant crisp output is sensitive to all of the active fuzzy outputs of the inference mechanism. Fig.18. and Fig.19.shows the output membership functions chosen for K_p and K_i . For the error input PB (Positive Big), change in error PS (positive Small). The K_p and K_i values will be PS (Positive Small) and NS (Negative Small) respectively.

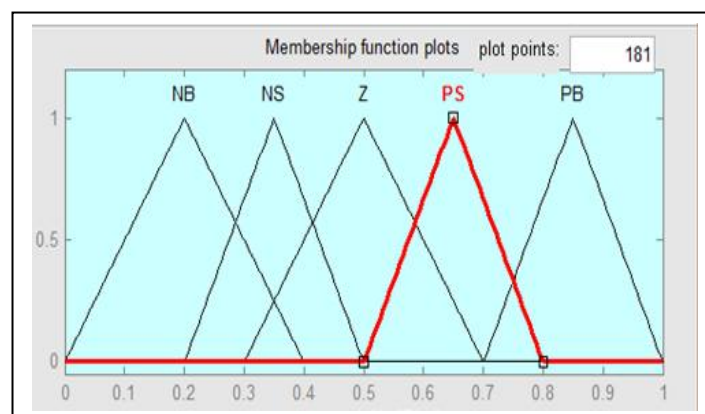


Fig. 18: Output membership function for k_p .

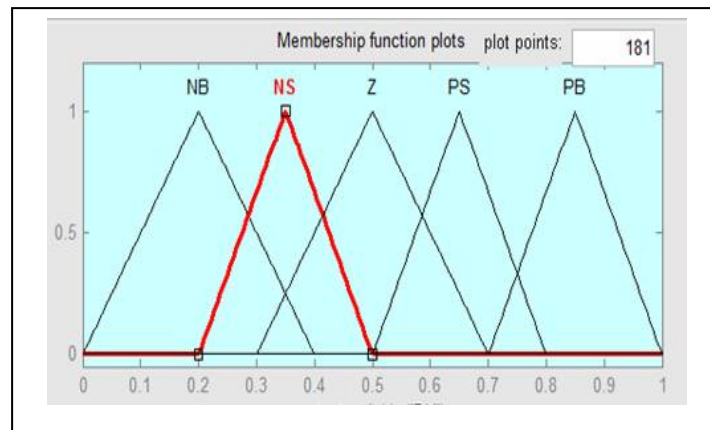


Fig. 19: Output membership function for k_i .

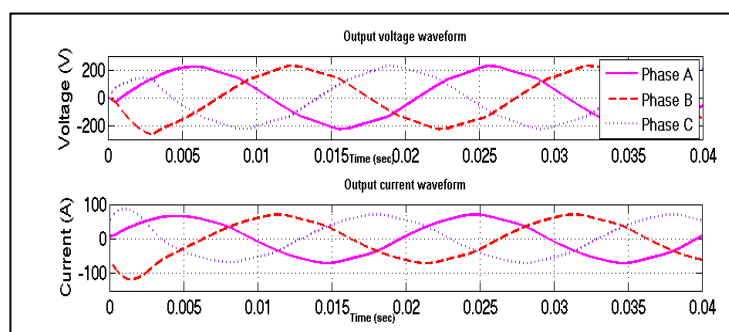


Fig. 20: Output voltage and current waveform with nonlinear load and with STATCOM compensation.

Fig.20. shows the system output voltage and current waveform with nonlinear load and with STATCOM compensation. The waveform shows that the STATCOM compensates the distorted current

waveform occurs at nonlinear load .

Fig.21 shows the THD analysis of nonlinear load using STATCOM compensation that has 3.51% as the total harmonic distortion.

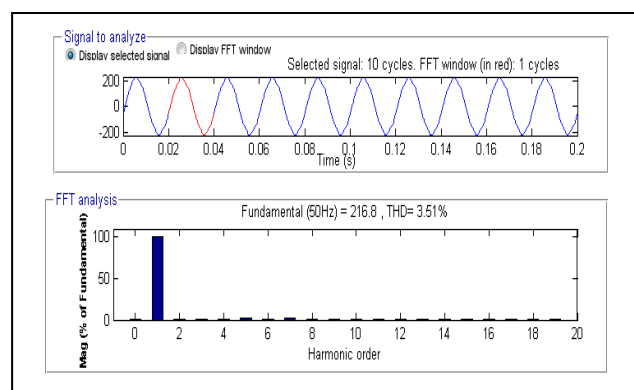


Fig. 21: THD analysis of the non-linear load system with STATCOM compensation.

Table 4: comparison between without and with statcom of the system with nonlinear load.

Factors	Without STATCOM	With STATCOM
THD of Output Voltage	6.43%	3.51%
Power Factor	0.7853	0.9324

Table.IV shows the comparison of the THD level of output voltage and power factor of the system at nonlinear load without and with STATCOM compensation.

By using non-linear load without and with

STATCOM compensation the output voltage THD and power factor will be 6.43% and 0.7853 for without STATCOM and thus 3.51% and 0.9324 for with STATCOM compensation.

Conclusion:

In this paper the reduced switch topology is used to reduce the switches in the nine level multilevel inverter and used in the place of the inverter in STATCOM. The non-linear load will produce the discontinuous and distorted current waveform that can be compensated by the controller using fuzzy logic that tunes K_p and K_i values depending upon the errors of DC voltage and inject decreased amount of current when using nonlinear load to improve power factor. The number of switches in per phase is reduced to 7 compared to 16 switches in CHBMLI. The THD analysis for non-linear load without STATCOM produces 6.43% and the power factor is about 0.7835 whereas with the STATCOM compensation for non-linear load produces 3.51% as THD and also the power factor is 0.9324. Thus the power factor gets increased by using the STATCOM with the reduced switch topology along with the fuzzy controller.

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