Frame of Reversible BCD Adder and Carry Skip BCD Adder and Optimization Using New Reversible Logic Gates for Quantum-Dot Cellular Automata

Neeraj Kumar Misra, Subodh Wairya and V. K. Singh

Abstract

Objective: Reversible logic has become more prominent in the field of low power nanotechnology era. It has specially used in Quantum-dot cellular Automata (QCA) which substituted the CMOS technology. In designing with CMOS it requires a large layout area in making the contacts between the different devices. This work demonstrates the reversible BCD adder and carry skip BCD adder circuit based on three new type of reversible gates, namely Full adder subtraction (FAS), Half adder subtraction (HAS) and Overflow detection (OD) gates, to optimize the adders circuit. The new type of reversible full adder using FAS gate is best circuit in terms of quantum cost. By utilizing these three new types of gates, reversible n-digit BCD adder and 1-digit carry skip BCD adder are also proposed with its algorithm. In addition, lower value of reversible parameters has been presented and has more influence on reducing the circuit cost which is far lower. This OD gate is first ever gate layout design implemented in the QCA and that layout in QCA provided, the more suitable simulation waveform for overflow detection. Also, the realization of the OD gate with QCA results in minimum cell complexity, clock cycle delay (latency) and area which are found to be 174, 3 and 0.27µm² respectively. Area and delay analysis also show that the circuits is optimized in terms of architectural complexity and speed.

INTRODUCTION

Reversible logic has the popular perspective of designing digital logic operation with negligible power consumption. It is explained by Landauer that the loss of each bit of information dissipates heat energy KT ln2 joules, where T is temperature and K is the Boltzmann’s constant (Landauer, 1961). Sometime on Bennett explain that the energy losses could be prevented, if the logic computation is turn to reversible way (Bennett, 1973). A reversible circuit is designed by reversible gates. In reversible gate expression, it computes is bijective, that is, every distinct input pattern yields a distinct output pattern (Bibhash Sen et al., 2013; Guown yang et al., 2005; M.Mustafa et al., 2013; Neeraj Kumar Misra et al., 2015).

Presently Quantum-dot Cellular Automata (QCA) become an attractive research area due to high computing speed, low power and high device density in nano-electronic digital circuits (Bibhash Sen et al., 2015; Ali Newashaharet et al., 2015). In QCA cell formation of four quantum dots placed at the corner of a square and comprise two free electrons (Shaahinangiziet al., 2014). In QCA logic state is laid down by the polarization of electrons. The two stable polarization of electrons are binary logic 0 (P= -1) and binary logic 1 (P=1) as depicted in Fig. 1e. The timing in QCA is versed by the synchronized of four clock zones and each clock zone has 90⁰ phase shift as depicted in Fig 1f. The fundamental QCA layout design are the three input majority voter gate (MV) and an inverter, depicted in Fig 1b, 1c. The majority voter gate described as MV(A,B,C)=(A+B+C). We look into that majority vote (MV) is the optimum preference in designing of logic design such as AND, OR as depicted in Fig. 1d, 1h.

Arithmetic circuits like binary Adder/Subtraction are the essential blocks of digital circuit design (Himanshuthapilyalet al., 2008; Majid Haghparaset et al., 2008; D. Krishnaveniet al., 2011). This essential blocks is mostly used in digital signal processing (DSP) application like convolution, Fast Fourier transform (FFT) and
The rest of the paper is organized as follows: Section 2 is dedicated to the preliminary approach of BCD adder. The proposed three new types of reversible gates and their quantum circuits are presented in Sub-section 3.1. In Section 3.4, related work on this BCD adder and various design issue lemmas are reported. The carry skip BCD adder design procedure is reported in Section 3.5. In Section 4, deals with proposed OD gate layout and simulation result in QCA framework.

2. Background Study:
Several efforts have already been constituted to design of reversible BCD adder and carry skip BCD adder. Preparatory, a reversible BCD adder was presented by Ashish Kumar Biswas et al. [2008]. The design was based on the novel MTSG gate. The BCD adder circuit consist of 10 gate count, 10 garbage output and 55 quantum cost. In Rigui Zhou et al. [2012], a design frame the BCD adder, based on novel ZRQG gate and NCG gate was designed. This BCD adder requires 8 gate count, 11 garbage output and 54 quantum cost. The some other parallel adder/Subtraction and BCD adder designs are explored (Rekha James et al., 2007; Himanshuthapliyalet al., 2007; Majid Mohammadi et al., 2008 and H. G. Rangaraju et al., 2010). Thus, from a careful review of the previous work on reversible BCD adder and carry skip BCD adder design, no such designs in QCA framework.

3. Proposed Design of Reversible Bcd Adder
In this section, we design a compact circuit of reversible BCD adder. To design a compact BCD adder, we propose three new type of reversible gates and their quantum circuits are presented in Subsection 3.1. In approach to less architectural complexity, we design FAS cell and F_F_H cell in subsection of design of parallel adder and design of carry skip adder. These designs are then extensively utilized to design 1-digit and n-digit BCD adder.
3.1 Three Proposed Reversible Gates:

Three new types of reversible gates are proposed which are helpful for the design of reversible BCD adder and carry skip BCD adder circuit. The first is the 3x3 HAS gate. Fig. 2a, 2b depicted the block diagram and quantum implementation of the HAS gate. The HAS gate has a quantum cost and hardware complexity are 5 and 3α+2β+δ respectively. It consist of four XOR gates, two controlled-V and one controlled-V+ gate. The truth table of this 3x3 HAS gate is shown in Table 1. The proposed HAS gate, can implement the operation of half adder and half subtraction, depicted in Fig. 2c.

\[
\begin{array}{ccc}
A & B & C \\
\hline
0 & 0 & 0 \\
0 & 0 & 1 \\
0 & 1 & 0 \\
0 & 1 & 1 \\
1 & 0 & 0 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
1 & 1 & 1 \\
\end{array}
\]

The second new type of 4x4 proposed gate is the FAS gate. Fig. 3a, 3b depicted the block diagram and quantum implementation of the FAS gate. The FAS gate has a quantum cost and hardware complexity are 8 and 8α+2β respectively. It consist of six XOR gates, two controlled-V and one controlled-V+ gate. The truth table of this 4x4 FAS gate is shown in Table 2. The proposed FAS gate, can perform the operation of full adder and full subtraction, depicted in Fig. 3c.

<table>
<thead>
<tr>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
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<tbody>
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</table>
The third new type of 5x5 proposed gate is the OD gate, which produce outputs \( P = (B + C) \oplus D \oplus A \), \( Q = B \), \( R = C \), \( S = D \) and \( T = (B + C)D \oplus E \oplus A \). Fig. 4a, 4b depicted the block diagram and quantum implementation of the OD gate. The OD gate has a quantum cost and hardware complexity are 10 and \( 4\alpha + 2\beta \) respectively. It consist of seven XOR gates, four controlled-V and two controlled-V* gate. The truth table of this 4x4 OD gate is shown in Table 3. When the first input is set to 0, and other four inputs are set to \( B = S_1 \), \( C = S_2 \),
D = S_3 and E = C_3, the OD gate simultaneously realizes Q = S_1, R = S_2, S = S_3 and T = S_3(S_1 + S_2) ⊕ C_3, the logic expression is used for overflow detection, depicted in Fig. 4c.

![Block diagram](image)

**Fig. 4:** Proposed reversible OD gate (a) Block diagram (b) Quantum implementation (c) Block diagram of overflow detection

<table>
<thead>
<tr>
<th>INPUT</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>P</th>
<th>Q</th>
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Table 3: Reversibility of the proposed OD gate.
3.2 Design of Parallel adder

In reversible design, the FAS gate can be used as the full adder module. Therefore, 4-bit parallel adder we use four FAS gates is depicted in Fig. 5. The quantum cost of single FAS gate is 8. Therefore, the quantum cost of 4-bit parallel adder is 32.

QC (4-bit parallel adder) = 4QC (FAS gate) = 4x8 = 32.

\[
\begin{align*}
\text{Fig. 5: Block diagram of 4-bit reversible parallel adder.}
\end{align*}
\]

3.3 Design of Overflow Detection and Correction Circuits:

In this section, we propose a new type of overflow detection and correction circuit. A lemmas is offered for circuit design.

**Lemma-1:**

In BCD addition, the overflow detection circuit can be realized by at least one reversible OD gate.

**Proof:**

A BCD number overflow occurs if the final obtained result is greater than 9 (1001). In FAS cell, the carry-out shown by C and it is fixed by the FAS cell, depicted in Fig 3c. For overflow detection carryout (C3) is applied to OD Gate and also other inputs its enable the overflow detection circuit and generate logic bit expression C_{out} = (S1 + S2)S3 \oplus C3. If C_{out}=0, nothing is required for addition and another case C_{out}=1, binary 0110 (6) should be added to the BCD sum. In overflow detection circuit utilize only one OD gate, depicted in Fig. 4c.

**Lemma-2:**

A reversible BCD adder circuit, overflow correction logic can be realized by at least three reversible gates with 15 quantum cost.

**Proof:**

An overflow correction required when C_{out} is 1 and no correction required when C_{out} is 0. When C_{out} = 1 required to add of 0110 (6). In this circuit, we use one FG as a sum logic, one FAS gate implement as a full adder and one HAS gate as half adder. The proposed BCD overflow correction is depicted in Fig. 6. The QC of FG, FAS and HAS gate are 1, 8 and 5, respectively; therefore the QC of the circuit is 14.

QC (Circuit of BCD overflow detection) = QC (FG)+ QC (FAS)+ QC (HAS)=1+8+5=14

\[
\begin{align*}
\text{Fig. 6: Block diagram of BCD overflow correction.}
\end{align*}
\]

3.4 Design of BCD adder using proposed gates:

A design of 1-digit BCD adder has three levels: First level is parallel adder (Used as FAS cell), second as overflow detection (Used as OD gate), and the third is the overflow correction (Used as F_F_H cell), depicted in Fig. 7a.
Fig. 7a: Design of 1-digit BCD adder.

First level:
4-bit parallel adder operation uses an FAS cell, initially set $C_{in} = 0$ and added a bit ($B_4 \ A_4$, $B_3 \ A_3$, $B_2 \ A_2$, $B_1 \ A_1$) and generate output marked as ($S_3 \ S_2 \ S_1 \ S_0$) and the final carry output marked as $C_3$

Second level:
Overflow occurs when the output logic is greater than 9 (1001) and the $C_{out}$ is set by the OD gate by using logic expression $C_{out} = (S_1 + S_2)S_3 \oplus C_3$. Overflow detection design utilizes only one reversible OD gate.

Third level:
In overflow correction utilize F_F_H Cell.
The new type of 1-digit BCD adder is depicted in Fig. 7a. It has 8 gate count, 11 garbage outputs and 7 constant inputs. Quantum cost of FAS cell, OD gate and F_F_H cell are 32, 10 and 14, respectively; therefore, the quantum cost of 1-digit BCD adder is $QC(1\text{-digit BCD adder}) = 1QC (\text{FAS cell}) + 1QC (\text{OD gate}) + 1 QC (\text{F_F_H cell}) = 32+10+14 = 56$

Fig. 7b depicted the circuit of n-digit BCD adder which is designed by cascading of 1-digit BCD adder.

3.5 Design of Carry Skip BCD adder using proposed gate:
The design of carry skip 1-digit BCD adder uses four levels. Fig. 9 depicts the carry skip 1-digit BCD adder design.

First level indicates the design operation performed by FAS carry skip cell (Fig. 8). The quantum cost of single FAS gate is 8. Therefore, the quantum cost of FAS carry skip cell is 32.

QC (FAS carry skip cell) = 4QC (FAS gate) = 4x8 = 32.

Second level indicates the design of Carry Skip logic, which consists of four gates of two types (3 HAS gate +1 FRG gate). The carry bit named (Y) is found by preparation of propagation logic $P = (P_1P_2P_3P_4)$ where $P_i = A_i \oplus B_i$ i.e $Y = P_{C_3} + \overline{P} C_4$ for analyzing this expression set $P=0$ then the carry $C_4$ propagates like in parallel adder else case $C_4$ propagate for carry skip logic. The generation of $C_4$ will take time. FRG will hold for a generation of the carry bit (Y) until $C_4$ is solved.

Third level: Design operation performed by OD gate.

Fourth level: Design operation performed by overflow correction by using F_F_H cell.
Fig. 8: Block diagram of FAS carry skip cell.

Fig. 9: Proposed design of Carry Skip 1-digit BCD adder.

The new type of carry skip BCD adder is depicted in Fig. 9. It has 13 gate count, 15 garbage output and 11 constant input. Quantum cost of FAS cell, HAS, FG, FRG, OD and F_F_H cell are 32, 5, 1, 5, 10 and 14, respectively; therefore, the quantum cost of 1-carry skip BCD adder is

\[ QC \text{ (1-carry skip BCD adder)} = QC \text{ (FAS cell)} + 3QC \text{ (HAS)} + 1QC \text{ (FG)} + 1QC \text{ (FRG)} + 1QC \text{ (OD gate)} + 1 QC \text{ (F_F_H cell)} = 1 \times 32 + 3 \times 5 + 5 + 5 + 10 + 1 \times 14 = 77. \]
Algorithm. I. Carry Skip 1-digit BCD adder.

Select 4-bit arguments \((B_4, A_4, B_3, A_3, B_2, A_2, B_1, A_1)\), carry in \((C_{in})\) and generate outputs as \((C_{out}, Z_{4}, Z_{3}, Z_{2}, Z_{1})\).

1. Begin
2. Level 1
3. For \((i = 1 \text{ to } 4)\)
   \{ 
   4. \(P_i = A_i \oplus B_i\) // Propagate bit \((P_i)\) is generated from FAS carry cell.
   \}
4. \(P = (P_1, P_2, P_3, P_4)\) // Generate \(P\) from each HAS gate.
5. Level 2
6. Find \(S_i = (A_i \oplus B_i \oplus C_i)\) // Sum from FAS carry cell.
7. Carry \(= \{(A_i \oplus B_i)C_i \oplus A_iB_i\}\) // Carry from FAS carry cell.
8. Level 3
9. Find \(Y = \overline{X_{in}} + \overline{X_{out}}\) // Generate \(Y\) from FRG gate.
10. Level 4
11. Find \(C_{out} = [S_4(S_2 + S_3) \oplus Y]\) // Generate \(C_{out}\) from OD Gate.
12. Level 5
13. Find \(C_{out} > (9)\) // Overflow condition occur then add 0110 and use F_F_H Cell for correction logic.
14. Level 6
15. Record each output \((C_{out}, Z_{4}, Z_{3}, Z_{2}, Z_{1})\)
16. End;

4. QCA Implementation of Od Gate:

We designed the QCA layout structure of the OD gate is depicted in Fig. 11 that is composed of 174 cells and one layer. Five of these, acting as inputs to the cell, are marked A, B, C, D and E. The layout of the OD gate show that there is the minimum cell used with minimum area. The QCA layout of OD gate performs the Boolean expression \(P = (B + C) \oplus A \oplus D\), \(Q = B\), \(R = C\), \(S = D\) and \(T = (B + C)D \oplus E \oplus AD\)

RESULT AND DISCUSSION

The design of OD gate is simulated to test the workability with QCADesigner version of 2.0.3 and follow the truth table of this gate, depicted in Fig 12. We simulate OD gate by using bistable approximation with default parameters. In addition, the overflow detection operation performed by OD gate. The OD gate capability of performing overflow detection condition by fixing input \(A = 0\); and other four inputs \(B, S, D\) and \(E\) \((C_4)\) are for four bits to be added the OD gate simultaneously implements \(Q, R, S, T\) and \(C_{out}\). Fig. 13 reveals that when the input \(S = 1\) and \(S = 1\), then the output becomes \(C_{out} = 1\); when the input \(S = 1\) and \(S = 1\), then the output becomes \(C_{out} = 1\) and when \(C = 1\), then output become \(C_{out} = 1\). In a similar way when output \((C_{out} = 1)\) signifies correction required. In other case \(C_{out} = 0\) means no correction required. From Fig. 12 and 13, we can see that polarization value of all four output signals is fairly better.
Fig. 11: QCA layout of OD gate.

Fig. 12: Simulation result of OD Gate.
Fig. 13: Simulation result of overflow detection by using OD gate.

Table 4: Comparison of BCD overflow detection.

<table>
<thead>
<tr>
<th>Methods</th>
<th>NOG</th>
<th>GO</th>
<th>CI</th>
<th>UD</th>
<th>Quantum Cost</th>
<th>Circuit area in ($\mu m^2$)</th>
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<tr>
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<td>1</td>
<td>1</td>
<td>1</td>
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Table 5: Comparison between Proposed and existing design of BCD adder in terms of evaluation parameters.

<table>
<thead>
<tr>
<th>Methods</th>
<th>1-digit BCD adder</th>
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<td>In Rigui Zhou et al. 2012</td>
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<td>11</td>
<td>7</td>
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Table 6: Comparison between proposed and existing design of carry skip BCD adder in terms of evaluation parameters.

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Table 7: QCA. Overflow detection behaviour analysis by using OD gate

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<tr>
<th>Reversible OD gate</th>
<th>No. of MV’s used</th>
<th>Cell complexity</th>
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<th>Cell area (nm²)</th>
<th>Area usage (%)</th>
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<td>27,5455</td>
<td>56,376</td>
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</table>

Conclusion:
In this paper, a new and improved type of reversible BCD adder and carry skip BCD adder are presented. The proposed circuits is demonstrated around the QCA technology in terms of low clock cycle delay, high device density, high computing speed and no loss of power in signal transition and propagation. In addition, we have proposed three new reversible gates named as HAS gate, FAS gate and OD gate to optimize adder circuit. The new FAS gate can be utilized as a reversible full adder with using only one gate count and eight quantum cost. The OD gate layout verifying the QCADesigner framework and the simulation result found to ensures the correctness of the design. During the QCA layout design of OD gate we take care of minimizing the cells, clock cycle delay, total area and cell area which is found to be 174, 3, 27,5455nm² and 56,376nm² respectively. We have established the optimal parameter with several definitions and lemmas for adder circuit design. Hence we conclude that the new reversible gates, BCD adder and carry skip adder will be absolutely useful in low power digital computing circuits, arithmetic and logic unit, low power nanotechnology era and quantum computer.

REFERENCES
224-240.


