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Design of a Low Power, High Speed Analog to Digital Pipelined Converter for High Speed Camera CMOS using 0.18µm CMOS Technology

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ABSTRACT

Background: In this work one presented the design analog to digital Converter(ADC) of pipeline type of 3bits, 10MS/s and a low power consumption for high speed camera CMOS. The OTA plays an important role in the ADC, because of its conversion rate and power consumption are limited by the performance of the OTA. The designed ADC in this paper employs parallel pipeline architecture based on Double Buffered S&H Circuit with CMOS Switch (SHA), The overall A/D converter performance such as distortion, dynamic range, SFDR and noise are largely dependent on S/H amplifier. The folded cascode OTA functions with a low voltage supply 1.8V and consumes 1mW of power, the design is implemented in TSMC 0.18µm technology; this architecture composed of three stages, a differential stage of entry, followed by a stage of gain, and a Common Mode Feed Back (CMFB) circuit. This latter introduced to improve the performance of OTA. The simulation of the OTA shows that the open-loop gain is 103.94 dB, the phase margin (PM) is 61.06° and the unity gain bandwidth (UGB) is 298.4 MHz. The ADC consumes 13mW at 10MS/s sampling rate and the active area of pipeline ADC is about 0.1461 mm². Finally, the maximum differential nonlinearity (DNL) is +0.5LSB/LSB and the maximum integral nonlinearity (INL) is 0.4LSB/LSB.

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INTRODUCTION

Several works were published earlier in the area of pipeline ADCs. In these ADCs, multi-MHz sampling rates are achieved using parallel pipeline architecture.

Speed pipeline analog-to-digital converters are used in various application areas are important building blocks in modern signal processing and communication systems. There are many types of ADC such as flash ADC (Mostafa and Hassan, 2012), folding and interpolating ADC, pipeline ADC, delta-sigma ADC and integrating ADC (Jipeng, 2003). The pipelined ADC is one of the types of ADC which is having a lot of advantages. One of the benefits, it is being an alternative solution for high speed camera CMOS (Sébastien, 2009; Jérôme, 2008). The block diagram of general Pipelined ADC is shown in Fig. (6), sample-and-hold circuit, digital-to-analog converter (DAC) and the interstate amplifier (Phillip and Holberg, 2000; Jacob baker *et al*., 1998). Sample-and-hold circuit is a vital part in the pipeline ADC architecture and other data-converter systems.

The sample-and-hold circuit can give some isolation between the pipelined ADC and its driving circuit. So, the driver faces less back noise from the comparators in pipelined ADC (Jipeng, 2003). There are many different structures for sample-and-hold circuits. For example, Feedback Improved S&H Circuit, S&H Circuit using Miller Cap, Switched Capacitor S&H Circuit and double buffered sample-and hold circuit. Indeed, this paper focuses on design and implementation of double buffered S&H Circuit with CMOS switch (SHA). The operation of sample-and-hold circuit is divided into two phase which is the sampling phase and hold phase. The design of sample-and-hold circuit in pipelined ADC is challenging especially in a low power consumption application (Bernhard, 2011).

The rest of this paper is organized as follows: The section 2 describes the design of op-amp architecture. The section 3 is dedicated to the description of the proposed circuit of sample-and-hold. In the following, the sections 4 and 5 respectively describe the design of the proposed 3-bit pipeline ADC and the simulation results. The layout and post layout simulation results are provided in Section 6 , Finally, concludes this paper.

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OP-AMP Folded cascode design:

Op-amp is an important part of sample and hold circuit. There are several types of fully differential op-amps which are telescopic, folded-cascode, multi-stage and gain boosted op-amps (Razavi, 2000; Jipeng Li and U.K. Moon, 2004; Thomas B.C and Paul R.Gray, 1995). In designing an op-amp, several electrical characteristics, for example gain-band width, slew rate, common-mode range and output swing have to be taken into consideration. Table 1 shows the performance of amplifier folded-cascode.

Table 1: Performance of amplifier folded cascade.

Specification	Specification values
Supply voltage	1.8 V
Bias current	10 µA
Load cap	1 p
Gain	≥90 dB
Phase margin	> 45 deg
Gain margin	>0 dB
Bandwidth	1 KHz
SR	≥5 V/µs
ICMR-	≤200 mV
ICMR+	≥ 1.5 V
CMRR	≥50 dB
PSRR+-	≥50 dB
Offset	≤-+ 10 mV
Power Dissipation	< 1 mW

The topology of folded-cascode amplifier is shown in Figure 1. The design OTA composed of three stages: 1) a fully differential (in and out) pair with current mirror biasing is employed; 2) a common source amplifiers are used to provide a large gain (Bernhard E,2011); 3) the output of folded cascode op-amp, vo+ and vo- are the inputs to the CMFB circuit while the output is Vcmc.

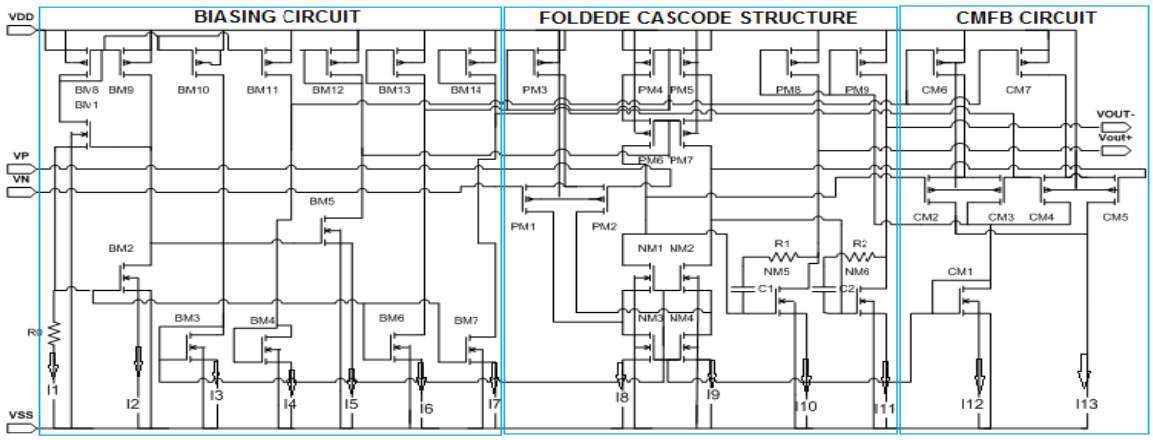

Fig. 1: Fully differential folded cascode op-amp.

For folded cascode Op-Amps the compensation is achieved by load capacitance CL itself and it provides dominant pole compensation. As CL increases, the Op-Amp stability improves but gets slowed down. The basic idea of folded cascode Op-Amp is to apply the opposite type NMOS cascode transistors to the input differential pair of PMOS type. The design of Op-Amp is becoming increasingly difficult as supply voltages and transistor channel lengths are scaled down. There are several Op-Amp topologies possible viz. Two stages CMOS Op-Amp, regulated cascode Op-Amp, folded cascode Op-Amp and Telescopic cascode Op-Amp etc. A two stage CMOS Op-Amp is preferred where high gain and large output swing are required. However, the addition of second stage reduces unity gain frequency and hence speeds of operation. A telescopic cascode Op-Amp offers better power and bandwidth criterion but has severe drawback of reduced output swing and hence not preferred for low voltage applications. Folded cascode Op-Amp provides higher output swing compared to telescopic cascode Op-Amp and better PSRR and speed over two stages Op-Amp. Hence folded cascode Op-Amp is used here.

This arrangement allows the output to be taken at the same bias levels as that of input signal. Even though it is a single stage, the gain is reasonable since the gain is decided by the product of input transconductance and the larger output impedance. The design use common mode feedback circuit (CMFB). The Op-Amp results of Figure 8 shows a unity gain frequency of 298.4 MHz at 61.06˚phase margin and a gain of over 103.94 dB.

The proposed circuit of a Sample and Hold (S/H):

SHA is an important building block in the pipeline ADC architecture and other data-converter systems since the system throughput and accuracy are limited by the speed and precision at which the input and residue analog voltages are sampled and hold. Figure 5 depicts the schematic diagram of SHA architecture utilized in the proposed pipeline ADC. It employs the input is feedback to the first OPAM and the output is feedback to the second OPAM. The main advantages of this architecture are that the charge injection error and the clock feedthrough error are effectively removed. This type of SHA, therefore, obtains a very high-accuracy characteristic (Razavi, 2002; Rudy van de Plassche, 2003).

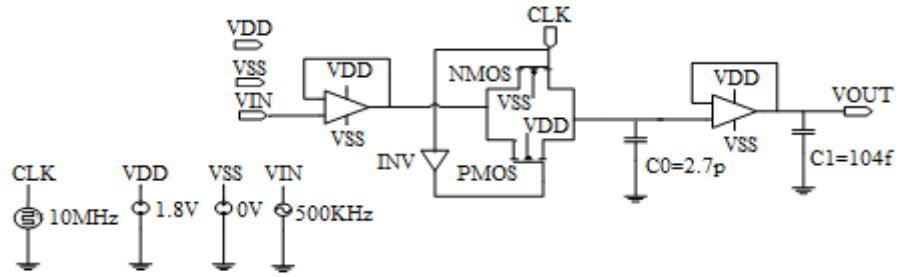

Fig. 2: Fully Double Buffered S&H Circuit with CMOS Switch (SHA).

Proposed 3-bit pipeline ADC:

Figure 3. Shows the block diagram of pipeline ADC, The block diagram illustrates the different blocks of our proposed ADC.

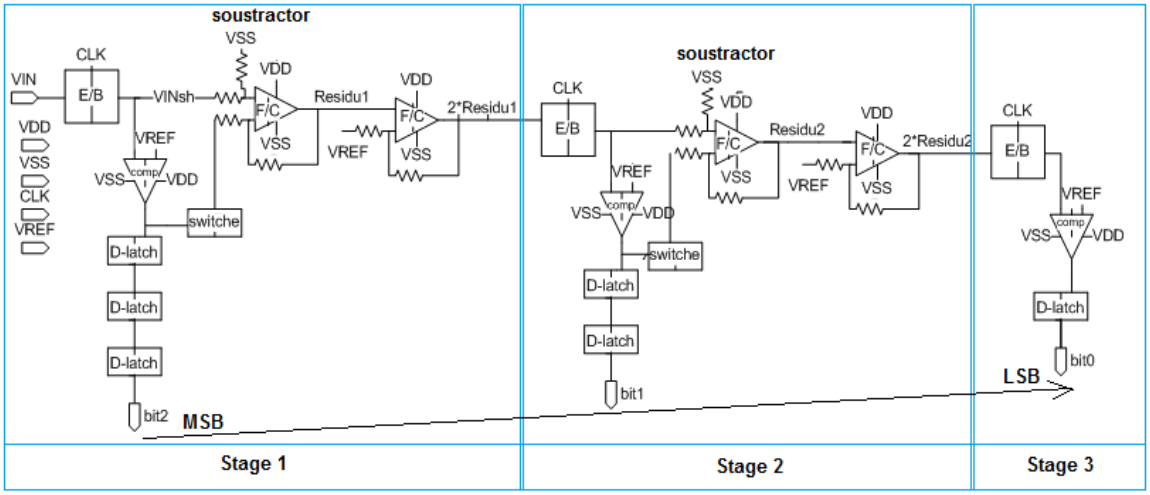

Fig. 3: The proposed 3-bit pipeline ADC architecture.

The required pipelined data converter has a resolution of 3Bits, each stage with an ADC of 1Bit, The blocks used are:

- A sample-and-hold
- A comparator
- A soustractor
- A gain of two amplifiers
- Latches

The description of each stage is as follows:

According to the block diagram from Figure 3, we first need to pass the signal by a comparator, to do so the original analog signal must be sampled and held so the comparator is fed a stable signal. After the first bit is obtained, it needs to be subtracted from the original signal to obtain the residue that will be entering the next conversion stage. The residue will also be amplified to remain in the full-scale range of the comparator to reduce loss of resolution. Each portion of the comparator outputs a bit of the data converter and every single output will contain a latch (H. Chen *et al*., 2001; M. Choe *et al*., 2000; R. C. C. Hui *et al*., 1998; J. Ming *et al*., 2001; I.E. Opris *et al*., 2000; L. Sumanen *et al*., 2001; M.Waltari *et al*., 2001; Y. Wang and B. Razavi, 2000; D. Miyazaki *et al*., 2000).

Manufacturers have recently introduced high-performance analog-to-digital converters (ADCs) that feature outstanding static and dynamic performance.

Simulation results:

The conventional folded cascode (FC) is designed and implemented in 0.18µm CMOS process technology. Simulations of the circuit are performed using Cadence Spectre Simulator.

An Operational FC is selected for which we have optimized the gain in open loop, the stability CMRR (Rate of Common Mode Rejection), PSRR (Power Supply Rejection Ratio), ICMR (Input Common Mode Range), and the Energy dissipated. Figure 4 shows the open-loop gain and phase margin of the proposed FC.

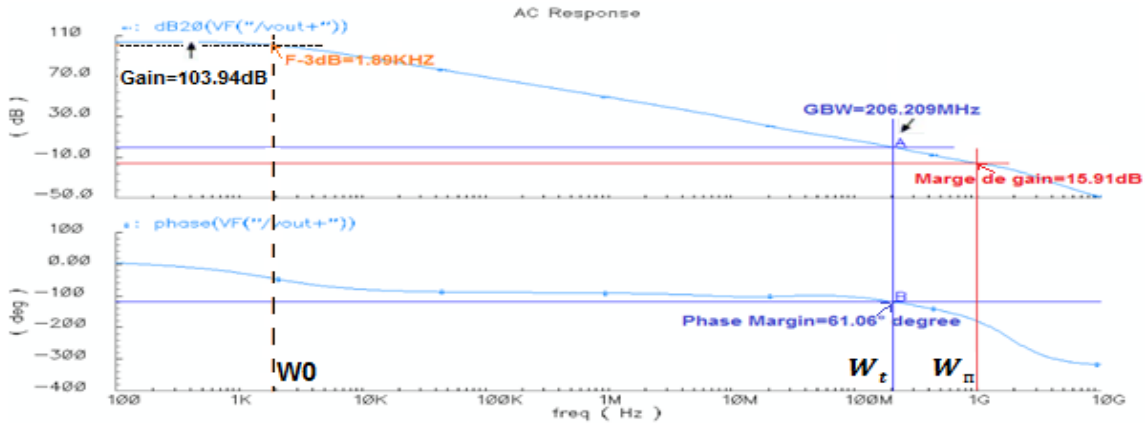

Fig. 4: The Gain and phase plots of folded cascode op-amp.

The table 2 below summarizes the performance achieved by the folded cascode.

Table 2: The performance of our folded cascade.

Specification	Specification values	values Obtained
Supply voltage	1.8 V	1.8 V
Bias current	10 µA	10 µA
Load cap	1 p	1 p
Gain	≥90 dB	103.94 dB
Phase margin	> 45 deg	61.06° deg
Gain margin	>0 dB	15.91 dB
Bandwidth	1 KHz	1.89 KHz
SR	≥5 V/µs	2883.5 V/µs
ICMR-	≤200 mV	180 mV
ICMR+	≥ 1.5 V	1.58 V
CMRR	≥50 dB	106.8 dB
PSRR+	≥50 dB	74.73 dB
PSRR-	≥50 dB	75.14 dB
Offset	≤-+ 10 mV	5.88 mV
Power Dissipation	< 5 mW	1 mW

The outputs of 10Msps sample and hold circuit with a gain of two is shown in figure5.

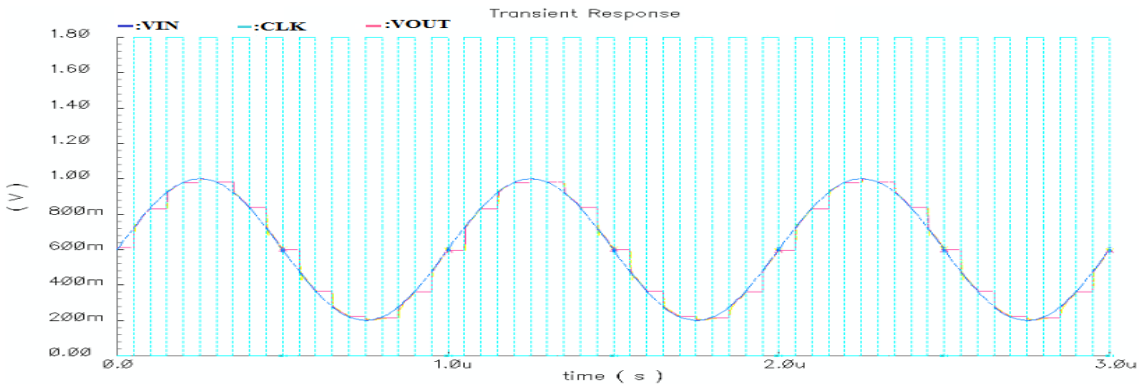

Fig. 5: Sample and Hold outputs.

The proposed ADC has been implemented in a Commercial 0.18µm technology and simulated using Cadence Spectre simulator. The supply voltage used is 1.8V, the reference voltage Vref/2=600mV and the sampling rate is 10MHz.

For the first simulation we took a functional typed simulation for an ordinary case temperature 27° with a 1.8V as a supply voltage, 100ns as time clock system and 3us as a time domain transitory.

The results are presented in the following graphs:

We will be using Cadence to test our previous design.

Now, to analyze the bits as input we should use the signal sine-wave.

The binary output of three stages are bit0, bit1 and bit3:

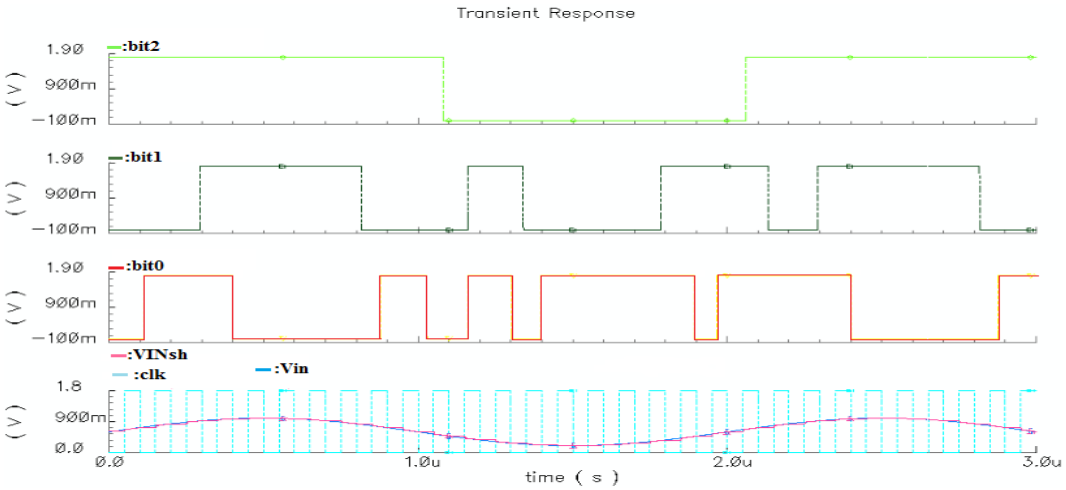

Fig. 6: A typical simulation results for our proposed ADC.

The table 3 below summarizes the performance and comparison achieved by the proposed A/D converter.

Table 3: The performance and comparison of our proposed A/D converter.

Resources	This work	(Dahoumane, M.,*et al*., 2008)
Technology	TSMC 0.18 µm	AMS 0.35 µm
Architecture	Pipelined	Pipelined
Supply voltage	1.8V	2 V
Resolution	3 bits	5 bits
Temperature	27°C	27° C
Conversion rate	10MS/s	25 MS/s
DNL	0.5LSB/LSB	0.7 LSB/LSB
INL	0.4 LSB/LSB	1.2 LSB/LSB
Power dissipation	13 mW	3.42 mW
Layout Area	0.1461mm²	0.056 mm²
ENOB	2.65 bits	-

Simulation result of layout and post layout:

Layout of the OTA Folded Cascode including the CMFB circuit has been drawn using the Virtuoso layout editor and is shown in Fig.7.While verifying the Design Rule Check (DRC) and Layout Versus Schematic (LVS) we finding "Total errors found: 0" for DRC and "the net-lists match" for LVS. (R.Jacob Baker, 2005; Dan Clein, 1999) .The OTA occupies an area of 186.80µm × 61.68µm=0.0115 mm².

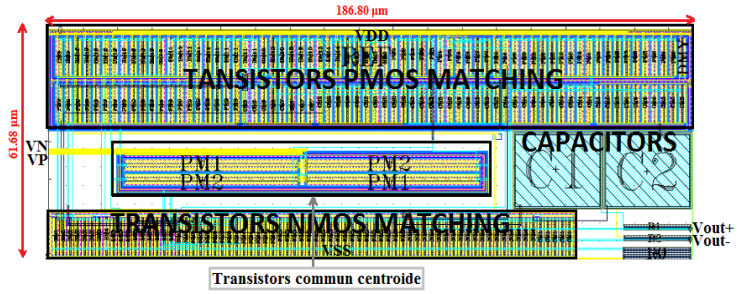

Fig. 7: Layout of the Proposed OTA FC.

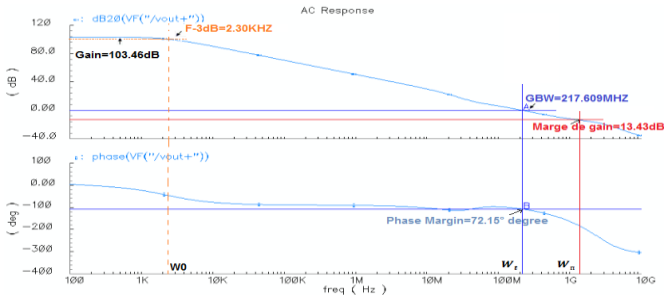

Fig. 8: Post layout simulation of the OTA FC.

MIMCAPMM capacitor of 500fF is used as the load. The post layout simulation for the frequency response is carried out and the result is shown in Fig.8. From fig.8, it may be noted that the dc gain and UGB of the OTA are 103.46 dB and 344.5MHz respectively. The results can be compared with the pre-layout simulation results shown in table 4. It is found that there is a 0.48dB reduction in the dc gain and a 46.1MHz augmented in the unity gain bandwidth.

The table 4 below summarizes the results of post layout compared with the pre-layout

Table 4: The results of post layout compared with the pre-layout.

Specification	Specification values	Results of schematic	Results of post layout
Supply voltage	1.8 V	1.8 V	1.8 V
Bias current	10 µA	10 µA	10 µA
Load cap	1 p	1 p	1 p
Gain	≥90 dB	103.94 dB	103.46 dB
Phase margin	> 45 deg	61.06° deg	72.15° deg
Gain margin	>0 dB	15.91 dB	13.43 dB
Bandwidth	>1 KHz	1.89 KHz	2.30 KHz
SR	≥5 V/µs	2883.5 V/µs	2106.7 V/µs
ICMR-	≤200 mV	180 mV	210 mV
ICMR+	≥ 1.5 V	1.58 V	1.57 V
CMRR	≥50 dB	106.8 dB	106.6 dB
PSRR+	≥50 dB	74.73 dB	75.13 dB
PSRR-	≥50 dB	75.14 dB	75.59 dB
Offset	≤-+ 10 mV	5.88 mV	10 mV
Power Dissipation	< 5 mW	1 mW	1.2 mW

The layout of the low power consumption pipelined ADC using 0.18µm is shown in Fig. 9. Fig.10 and Fig.11 show the Design Rule Check (DRC) and Layout Versus schematic (LVS) are verified and finding "Total errors found: 0" for DRC and "the net-lists match" for LVS [R.Jacob Baker,2005],[Dan Clein,1999]. The area of the layout is 254.1300µm × 575.1750µm = 146169.2227 µm2 = 0.1461 mm².

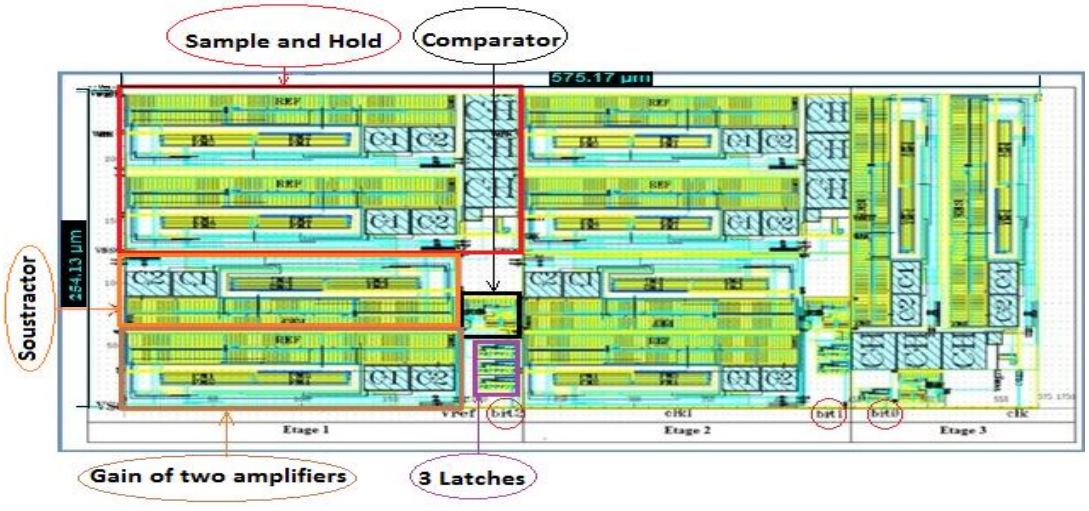

Fig. 9: Layout of the ADC.

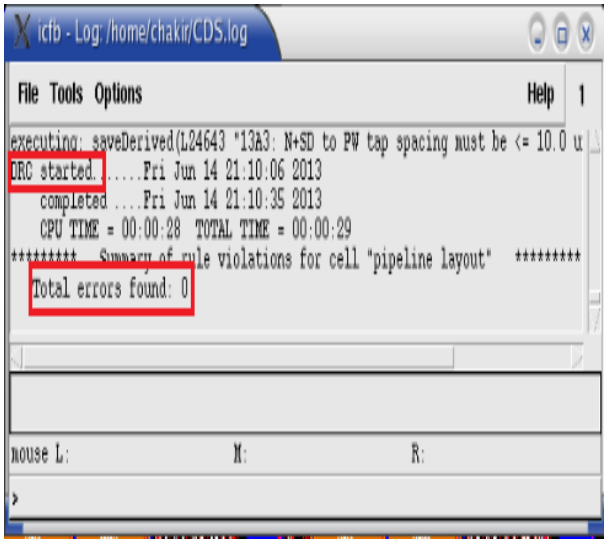

Fig. 10: Design rule check (DRC) of ADC.

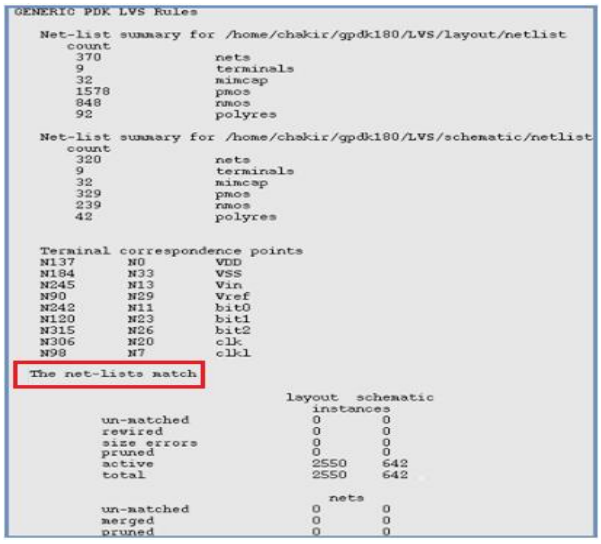

Fig. 11: Layout Versus schematic (LVS) of ADC.

Conclusion:

The proposed conventional folded cascode operational amplifier is implemented in 0.18µm technology. The OTA is studied using both pre-layout and post-layout simulation .The gain and unity gain bandwidth of the OTA obtained through pre-layout and post-layout simulation differ by 0.48dB and 46.10MHz respectively.

In this paper, a 3-bit pipeline ADC is presented. Low-swing operation allows achieving the speed of 10MS/s. The proposed 3-bit ADC achieves a static ENOB of 2.65, INL of 0.4LSB/LSB and DNL of 0.5LSB/LSB while consuming low power of 13mW and area of 0.1461mm2. Consequently, this kind of ADC can be used for high speed camera CMOS.

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