Australian Journal of Basic and Applied Sciences, 9(7) April 2015, Pages: 718-723

ISSN:1991-8178

Australian Journal of Basic and Applied Sciences

Journal home page: www.ajbasweb.com

Fan-Out an Independent Factor of Leakage current in Deep-Submicro meter Circuits

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ARTICLE INFO

Article history:
Received 12 March 2015
Accepted 28 April 2015
Available online 5 May 2015

Keywords:
Leakage current, Fan-out, Input vector, Sub threshold leakage current, Cadence Virtuoso, Cadence Spectre

ABSTRACT

Leakage current is treated as a major concern in deep-sub micrometer circuits. Leakage current is dependent on a number of factors. It is process and supply dependent. The key parameter in the reduction of leakage current is the threshold voltage Vth. Low Vth provides high performance whereas high Vth reduces sub threshold leakage current. Threshold voltage is dependent on two factors. Delay and subthreshold leakage current. Since delay is an important factor in determining the threshold voltage it is mandatory to address whether fan-out has any significance in leakage current. Always the customer requirement is high performance circuit with high speed. That is fast fan-out circuits. If leakage current is increasing with fan-out then it is a serious concern and it has to be addressed. Since optimizing fan-out reduces the capacitance and timing constraints. Immoderate load on the gates due to large fan-out degrades the circuit performance. The simulations are performed on different logic gates with different loads for varying fan-out and the corresponding leakage is measured. The circuits for experiment are set up on cadence virtuoso with the aid of UMC130 libraries. The simulations are performed using cadence spectre. This paper proves that fan-out is an independent factor of leakage current.

To Cite This Article: Philip C. Jose, S. Karthikeyan and K. Batri., Fan-Out an Independent Factor of Leakage current in Deep-Submicro meter Circuits. ***Aust. J. Basic & Appl. Sci.,*** *9(7): 718-723, 2015*

INTRODUCTION

The backbone of the semiconductor industry can be termed to be the exquisite scaling nature of CMOS techniques. For precision technology generation, threshold voltages will be scaled down. This will be reflected in switching power, performance etc. Once we scale the threshold voltage sub threshold voltage will get increases and can be claimed as a major part of the total power dissipation (Siva Narendra,, Vivek De, Shekhar Borkar, Dimitri A. Antoniadis, and Anantha P. Chandrakasan, FEBRUARY 2004). Drastic increase in sub threshold leakage current will results in the acclivity of total leakage current. It is possible to have higher density and performance by assertive scaling of CMOS devices (Saibal Mukhopadhyay, Arijit Raychowdhury, and Kaushik Roy, June 2003).

The main factor of leakage current is claimed to be the threshold voltage Vth (K. Roy, S. Mukhopadhaya, and H. Mahmoodi- Meimand, Feb. 2003).This threshold voltage is influenced by delay and subthreshold leakage current. As the research is moving on technology generation is also termed to be altering. This will ends up with abrupt increase in leakage current and majority of the total power is said to increase. One of the important factor is that normalized delay will degrade quadratically as the threshold voltage demote. The delay will be smaller if the threshold voltage is also downgraded.

It is necessary to scale down threshold voltage for low voltage low power circuits for better performance. Scale up of threshold voltage without affecting performance is a herculean task. If it is possible to use high threshold voltage and low threshold voltage in a way that no compromise is made on performance and leakage current is reduced means a great achievement. For such an achievement it is necessary to consider the fan-out effects of leakage current in deep-sub micrometer circuits. Leakage current has only been claimed to supply and process dependent. If fan-out is a dependent factor means it should have to be considered.

Circuit delay determines the clock rate of a digital computer system (Lianhua Ji and V.P.Heuring, june 1997). Delay characteristics of

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functional units and interconnections are determined by the speed. Fan-out limit is the maximum number of inputs a logic gate can drive. For electronic gates this is pointed out by the current drive ability. Output current must be sufficiently large for to charge the load, gate's input capacitor and wired capacitor in a specified time. Once the logic function is to be mapped to the gate net list two techniques are used to deal with gate fan-out constraints. First introduction of extra buffer stage for to use in clock distribution. Second is the modification of structure of gate net list by inserting intermediate nodes. But these techniques are increasing the circuit depth.

For full advantage of reduction of circuit depth the gate fan-in and fan-out must be within the limit of 8 and 85. The logic synthesis can be simplified by decoupling of fan-in and fan-out from interconnection delay. Fan-out optimization can be defined as the process of finding or obtaining buffer tree topology and sizing the buffer of the topology for constraints to be satisfied. The major research has been in this direction for fan-out optimization.

The paper is organized as follows. Effects of fan-out in leakage current are explained in section II. Section III contains what are the existing methods in fan-out optimization. Experimental setup provided in section IV. Section V contains Experimental results. Section VI concludes the paper.

Effects Of Fan-Out In Leakage Current:

From the customers perspective they always needs device whose performance is at the best. For circuits performance mainly stick on to the delay. As the number of gates inside a circuit is increased probably the delay will also increase. This makes it clear that fan-out is playing a vital role in determining the performance of a circuit. So fan-out optimization is a necessary thing which in turn helps to reduce capacitance, timing problem of large circuits etc. The main objective is to create fast fan-out circuits where area is not a major factor.

CMOS devices are subjected for scaling with an intention of higher density, performance, and disrate power consumption. By this it is possible to reduce the transistor delay times so that an upper hand in performance of microprocessors. For this objective threshold voltage Vth has to be scaled down for better drive current and improvement in performance. But this will results in decrease of delay and increase in subthreshold leakage current. But a bust in threshold voltage results in higher leakage current.

Leakage current affects the performance of dynamic gates (Mohamed Elegebaly and Manoj sachdev, august 2002). Noise immunity, increased leakage current, large process variations, low supply voltages, high clock frequency and crosstalk results in the downgrading the performance. Due to reduction in performance designers reduce the threshold voltage to meet the performance goal. So they have kept the leakage current in the defined boundary for better performance and ineffectively it affects fan-out since the association with delay.

For domino OR logic gates the leakage current is proportional to the fan-in (Farshad Moradi, Ali Peiravi, and Hamid Mahmoodi, Dec. 2004). Noise immunity is claimed to reduce with increase in fan-in. Actually for circuits with larger logic depth fan–in of the primary gates are acting as the fan-out of the subsequent stages. As the logic depth of a circuit increases the leakage current is said to increase and a number of gates will be at their worst case leakage. So it is necessary to point out what is the significance of fan-out in leakage.

Gate sizing is claimed to be a technique that can reduce circuit delay. Further it is possible to attain reduction in delay by inserting buffer of predefined size. This makes it evident that fan-out will subjected to change since the above discussed technique deals with process and geometry variation of the devices. So a change in threshold voltage which in turn leads to altered leakage and delay.

Existing Methods In Fan-Out Optimization:

The paper (David S. Kung, June 1998) deals with a fan-out optimization algorithm for near continuous buffer libraries. It is derived from optimal algorithm. By fan-out optimization it is possible to reduce capacitance and timing problem due to large fan-out. The fan-out optimization technique is particularly very effective transform but time consuming especially for technology-dependent timing optimization. The problem is NP-Complete. They have applied this particular technique for 19 fan-out cases and they have finded out it is a good algorithm for timing with only 1% increase in area.

In (Kanwar Jit Singh, Alberto Sangio Vanni-Vincentelli, Jun 1990) they have presented an algorithm for to distribute the signal to destination. The problem is the construction of a fan-out tree for signal so that time constraint at source node is met and fan-out trees have minimum area. Fan-out problem NP-complete and area cannot be a major factor. So main objective is the design of fast fan-out circuits without area constraints. The algorithm builds fan-out trees by partitioning fan-out signals into subsets and solving each problem independently. Algorithm capable of building fan-out tree that is an improvement of the previous work.

Major factor that is considered in the electronics industry are fast turn-around time and performance aspects are analyzed during synthesis process. Timing analyses helps to remove combinatorial circuits which make circuits to fail in performance test. Such circuits are re synthesized by reducing critical path. This work propose methods for improving performance due to high fan-out gates. Algorithm which is capable of computing fan-out of network with increase in size and depth of circuits are also available. Delay through the gates especially

NAND, AND is proportional to the number of fan-in. But here in this paper the authors have observed that delay through a gate is proportional to the no of output it drives.

(Hirendu Vaishnav and Massoud Pedram, June 1993) have proposed an algorithm which improves circuit performance while having an order restriction in fan-out. It is obtained by a comparison placement of mapped circuits. By this placement it produce fan-out trees which are free of internal edge crossing which gives good routing and chip area.

The research has been focused on the techniques which maximizes the logic sharing in which circuits with large number of fan-out nodes are obtained. Large load on the gates with large fan-out leads to performance degradation of the circuits. Fan-out optimization produces inverters of heavily loaded gates which improves the circuit performance. A good option is to optimize the number of fan-out or buffer. Unit delay model is inefficient or inadequate since it doesn't consider the load.

(Benham Amelifard, Farzan Fallah, Massoud Pedram, 2005 aug) deals with the low power fan-out optimization with multiple threshold voltage inverters. The delay can be preserved by splitting and merging. It also gives power and input capacitance optimization. For this purpose fan-out trees are converted into inverter chains and for the particular chain optimal size and threshold voltages are determined. It is mandatory to distribute signal through several destination in vlsi under a predefined timing constraint for a particular destination. Limitation is on the load that can be driven.

A fan-out optimization algorithm which is suitable for digital circuits designed for submicron CMOS technologies in (P. Cocchini, M.Pedram, G.Piccinini, M.Zamboni, nov 1998). They have dealt with bipolar LT-trees and optimal fan-out tree is obtained using dynamic programming. Buffer selection done with continuous buffer sizing technology on delay model which is specially crafted for submicron CMOS process. Minimum cost fan-out tree with required timing constraints are possible if active load, signal polarity, and signal propagation and transition time are specified.

It is necessary to create each output to be critical for that purpose the algorithm must take care of slack. In this work they have created an independent submicron CMOS delay which can be used for the computation of propagation time and output slope. LT-bipolar trees are introduced and optimized buffers are exploited for speed and area. Dynamic programming algorithm is implemented by them for tree selection.

An algorithm for gate sizing and fan-out optimization for a time critical path of a circuit in simultaneous way presented in (Wei Chen, Cheng-Ta Hsieh, Massoud Pedram, nov 2000). The optimization problem is formulated as a non-convex mathematical problem and is solved using non-linear programming package. Timing constraints are important factor in VLSI for to meet these constraints gate sizing and fan-out optimization is used.The non-linear programming is solved by LANCELOT.

Logical effort-based fan-out optimizer for area and delay (LEOPARD) presented in (Peyman Rezvani, and Massoud Pedram, Dec 2003). It is based on the availability of near continuous size buffer library. With the help of logical effort the algorithm tries to optimize total buffer area for required time, input capacitance, and buffer sizing assignment. The algorithm is capable of producing optimal fan-out tree especially for chain buffers. They were able to reduce the round-off error by transforming continuous time buffer to discrete.

The main objective was total buffer area reduction by LEOPARD. The algorithm presented by them where able to find fan-out tree and size of the buffer of tree by decomposing whole problem to sub problem. For each sink the sub problem is solved separately. This solutions are merged together to form the whole problem.

GFO is presented in (Rajeev Murgai, 2001). Research has been focused on fan-out optimization problem for single net (LFO). For real one it should optimize the delay through the entire circuit. An optimum solution to GFO is possible if visiting the nets of networks in reverse order and by applying LFO algorithm to each net. Then compute the required time of source by propagating the delay. This means GFO solvable in polynomial time. The paper finds the flaws in the above statement and proved that GFO is NP-Complete and it reverses the topological algorithm.

Experimental Setup:

The main objective of this paper is to verify whether fan-out has any effect over leakage current in deep-submicro meter circuits. For that leakage current of basic gates for 130µ meter technology with increasing fan-out are measured. The experiment is done up to fan-out 4 to finalize the results. Figure depicts the experimental setup for fan-out 4 of all the gates which is crafted by cascading the output of primary gates with different logic gates. At the first stage a primary gate is selected and it has to drive a single gate at its output which indeed forms fan-out 1.In this work the single gate that is driven by the primary gate at its output is selected to be as same for simplicity and it is a NAND gate. For the corresponding circuits the inputs are applied and the circuit is simulated and corresponding leakage current is measured for the primary gate and the gate connected at its output. The main aim of the work is to determine whether fan-out has any impact over leakage current. For to determine such a phenomenon we need to check whether the leakage current measured for the primary gate change with increase in fan-out.

For fan-out 2 to the output of primary gate two gates are connected. First is a NAND and second is a NOR. The circuit is simulated and the corresponding leakage current is measured for primary gate and the gates at its output. Fan-out 3 is analogous to the above described setup only difference is the number of gates driven by the primary gate output will be 3 which in turn contains NAND, NOR, and AND gate. A homogeneous setup of fan-out 3 with additionally cascaded fourth gate forms fan-out 4 setup and the gates are NAND, NOR, AND, and NOT. The results are analyzed for all the 4 fan-out stages to determine whether leakage current has modified in accordance with the increase in fan-out stages. The circuit for the experiment is set up in cadence virtuoso and are simulated using cadence spectre for 130 µ meter technology. The simulations are done at 27º c. Supply voltage fixed at 1.2 v and input applied to all the gates is logic ‘1’. The subsequent section elucidates the pictorial representation of the circuit set up for leakage measurement for fan-out 4 stages. The leakage current associated with each gate at that particular instant is also noted in the figure.

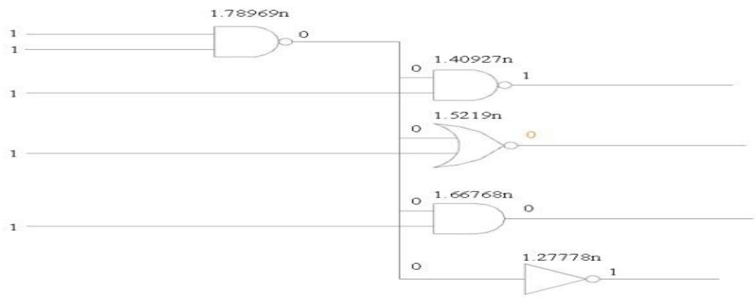

Fig. 1: Leakage (A) Measured For Nand Gate As The Primary Gate In Fanout 4.

Fig. 2: Experimental setup for measuring leakage current (a) of basic gates with varying fanout in cadence virtuoso.

Experimental Results:

We have executed the experiment to verify whether fan-out has any finicky effect over leakage current. Table 8 depicts the measured leakage current for various logic gates once the fan-out is increased from 1 to 4. Leakage current of the primary gate is not changing with increase in fan-out stages. From these results it is evident that leakage current remains to be a constant irrespective of the number of fan-out stages. Table 1 to Table 7 depicts the leakage current measured for the various gates for different input vectors.

Table 1: Leakage (A) Measured For Not Gate.

INPUTS	LEAKAGE(A)
0	1.278n
1	894.85p

Table 2: Leakage (A) Measured For 2 Input Nand Gate.

INPUTS		LEAKAGE (A)
0	0	234.06n
0	1	1.46092n
1	0	1.6764n
1	1	1.7897n

Table 3: Leakage (A) Measured For 2 Input Nor Gate.

INPUTS		LEAKAGE(A)
0	0	3.47671n
0	1	1.52719n
1	0	1.35257n
1	1	161.289n

Table 4: Leakage (A) Measured For 2 Input And Gate.

INPUTS		LEAKAGE (A)
0	0	972.96p
0	1	1.66763n
1	0	1.47981n
1	1	1.72596n

Table 5: Leakage (A) Measured For 2 Input Or Gate.

INPUTS		LEAKAGE (A)
0	0	2.27241n
0	1	2.14664n
1	0	1.84412n
1	1	1.3275n

Table 6: Leakage (A) Measured For 2 Input Exor Gate.

INPUTS		LEAKAGE (A)
0	0	3.8845n
0	1	4.01565n
1	0	4.38051n
1	1	3.74643n

Table 7: Leakage (A) Measured For 2 Input Exnor Gate.

INPUTS		LEAKAGE (A)
0	0	4.4216n
0	1	3.9103n
1	0	4.03879n
1	1	4.29297n

Table 8: Results Of Measured Leakage For Various Logic Gates.

Primary Gate	Leakage (A) for primary gate	Leakage (A) for fan-out 1 NAND	Leakage (A) for fan-out 2 NOR	Leakage (A) for fan-out 3 AND	Leakage (A) for fan-out 4 NOT
NAND	1.78969n	1.40927n	-	-	-
	1.78969n	1.40927n	1.52719n	-	-
	1.78969n	1.40927n	1.52719n	1.66768n	-
	1.78969n	1.40927n	1.52719n	1.66768n	1.27778n
NOR	161.289p	1.40918n	-	-	-
	161.289p	1.40918n	1.52719n	1.66763n	-
	161.289p	1.40918n	1.52719n	1.66763n	-
	161.289p	1.40918n	1.52719n	1.66763n	1.2777n
NOT	894.845p	1.40921n	-	-	-
	894.845p	1.40921n	1.52719n	-	-
	894.845p	1.40921n	1.52719n	1.66763n	-
	894.845p	1.40921n	1.52719n	1.66763n	1.2777n
AND	1.72596n	1.78979n	-	-	-
	1.72596n	1.78979n	161.366p	-	-
	1.72596n	1.78979n	161.366p	1.72399n	-
	1.72596n	1.78979n	161.366p	1.72399n	894.948p
OR	1.3275n	1.78979n	-	-	-
	1.3275n	1.78979n	161.371p	-	-
	1.3275n	1.78979n	161.371p	1.72599n	-
	1.3275n	1.78979n	161.371p	1.72599n	894.948p
EXOR	3.74643n	1.40921n	-	-	-
	3.74643n	1.40921n	1.52719n	-	-
	3.74643n	1.40921n	1.52719n	1.66764n	-
	3.74643n	1.40921n	1.52719n	1.66764n	1.27773n
EX-NOR	4.29297n	1.78979n	-	-	-
	4.29297n	1.78979n	161.371p	-	-
	4.29297n	1.78979n	161.371p	1.72599n	-
	4.29297n	1.78979n	161.371p	1.72599n	894.948p

Australian Journal of Basic and Applied Sciences, 9(7) April 2015, Pages: 718-723

We have compared the results in Table 1, 2, 3, 4, 5, 6, 7, 8, and 9 to study whether any of the logic gates has any impact on fan-out. But the comparison has proved that none of the gates leakage have any impact on fan-out. It has been already proved by the researchers that leakage current is particularly dependent on supply and process parameters. Apart from that this experiment has evidence that fan-out does not has any impact on leakage current and this is mainly due to its dependency on the primary input vectors applied at the input of the circuitry. From the comparative study of the table for example take the case where primary gate is NOT Gate. If the 2 inputs to the gate is logic '1' means it produce a leakage current of 161.289n amps. If we consider the fan-out setup for NOR gate leakage current of 161.289n amps in neither decreasing nor increasing as the number of fan-out increases. This clearly elucidates that fan-out does not have any impact on leakage current and it can be treated as an independent factor.

Conclusion:

In this paper we have studied the problem of fan-out effects on leakage current. The objective was to determine whether the fan-out can be treated as a dependent or independent factor of leakage current. The results and the findings proved that Fan-out cannot be treated as an important factor of leakage current but it depends primarily on the input vector that is applied to the input of the circuitry. So in the next stage of our research we plan to put forward an algorithm which specifically selects the best suitable input combination so that the leakage current can be reduced significantly.

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