Multilevel Inverter based DVR using Multi Carrier Sinusoidal Pulse Width Modulation Technique with Fuzzy Logic Controller

1M.Maheswari, 2S. Thangavel, 3C. Vivekandan

1E-mail: maheswarim894@gmail.com

Abstract
Presently the quality of the power is considerably affected due to the introduction of the semiconductor based drives in industries and in domestic sector as well. Series compensators and their combinations are available to mitigate this power quality issue. In this paper, a twenty seven level cascaded multilevel inverter based Dynamic Voltage Restorer (DVR) using multicarrier SPWM technique with fuzzy logic controller is proposed to handle deep voltage sags and swells on a three phase system. Vertical arrangement multicarrier sinusoidal pulse width modulation techniques are chosen for modulation to control the cascaded H-bridge inverter during the occurrence of sags and swells. Phase Disposition PWM (PDPWM), Phase Opposition Disposition PWM (PODPWM) and Alternate Phase Opposition Disposition PWM (APODPWM) are the three modulation techniques preferred in this paper and the DVR with these three techniques are designed, simulated and its performances are analyzed. It is observed that APODPWM based DVR yields the best performance among the three techniques and the DVR is capable of handling sags up to 90% of its nominal value and swells up to 80%.

Introduction
Voltage sags and swells in a power system are, in general, due to abrupt changes in the load, resulting in very low quality of the power delivered to loads. Sudden starting of induction motors in industries, energizing large capacitor banks or symmetrical and unsymmetrical faults on the power system cause voltage sags and swells. Tripping of adjustable speed drives (ASD) and faulty operation of PLCs in automation industries are certain unwanted consequences of voltage sag and swell, resulting adverse monetary impact. Dynamic Voltage Restorer (DVR) can provide the most cost effective solution to mitigate voltage sags, swells and outages by establishing the proper voltage quality required by sensitive loads. As per IEEE 519-1992 and IEEE 1159-1195 standards, voltage sag is a sudden reduction in supply voltage, ranging from 10% to 90% and voltage swell is a sudden rise of supply voltage ranging from 110% to 180% both for a period of 10ms to 1 minute on a 50 Hz supply (Ramasamy, M, and S. Thangavel, 2012; Boonchiam, P., 2006; Gunther, E.W, and H. Mehta, 1995). A DVR system comprises of a PWM voltage source inverter (VSI), a series injecting transformer, a control circuitry and a DC source. Among all the components, VSI is the major component of a DVR. A basic three-level VSI is realized using a full bridge configuration, in which the number of levels in the output voltage waveform is three and therefore, the amount of total harmonic distortion (THD) is very high (Rosli Omar, et al., 2009; Agileswari, K., et al., 2005; Benachaiba, C., and B. Ferdi, 2009). With every addition of a full bridge to the basic configuration, the number of levels in the output increases by two, resulting improvements in THD as the output voltage waveform approaches pure sinusoidal with every addition. In this proposed work, a cascaded H-bridge inverter configuration with 27 levels is used as VSI in DVR with 13 full bridge configurations. Despite the increase in complexity, appreciable improvement in the performance of the DVR system is obtained. Proper switching of the devices in different levels of the VSI is mandatory to obtain the proper functioning of DVR, which is achieved through modulation techniques. Presently, two major types of modulation techniques, viz. high frequency switching and fundamental frequency switching, are used. Due to the fast response characteristic, latter method is preferred in this work along with multicarrier SPWM technique for improved performance.

Keywords: Voltage Restorer (DVR), Multi Carrier Sinusoidal Pulse Width Modulation(MCSPWM), Phase Disposition PWM(PDPWM), Phase Opposition Disposition (PODPWM), Alternate Phase Opposition Disposition (APODPWM).
Proposed DVR:

The schematic diagram of the proposed DVR is depicted in Fig.1. In the event of a sag or swell, the proposed DVR compensates voltage fluctuation across the load by injecting the compensatory voltage to bring the load voltage back to nominal value, through a series injection transformer.

\[ |V_{\text{DVR}}| = |V_{\text{in}}| = |V_{\text{presag}}| - |V_{\text{sag}}| \]  

From the schematic diagram of DVR, the expression for voltage injected by DVR is,

\[ V_{\text{th}} + V_{\text{DVR}} = V_{L} + Z_{\text{th}}I_{L} \]  

Where \( Z_{\text{th}} = R_{\text{th}} + jX_{\text{th}} \)

Hence \( V_{\text{DVR}} \) may be expressed as

\[ V_{\text{DVR}} = V_{L} + Z_{\text{th}}I_{L} - V_{\text{th}} \]
where $P_L$ and $Q_L$ respectively are the real and reactive components of the load power.

![Single phase leg of 27 level cascaded H-bridge inverter](image)

**Fig. 3:** Single phase leg of 27 level cascaded H-bridge inverter

The reference voltage and supply voltage are constantly measured using respective measurement modules and the output of these modules, which are represented in a-b-c frame, are transformed into equivalent d-q-0 frame using Park’s transformation. The magnitudes of the d-q-0 outputs, which are the representatives of supply voltage and reference voltage, are compared and the error is fed to a fuzzy logic controller. The fuzzy logic controller for the proposed DVR has two inputs, named error and change in error. The membership functions of the error and change in error inputs are triangular. The triangular membership function is used here because the steady state error is minimum under this condition. The steady state error is reduced for membership functions with the reduced value of the nucleus. For a triangular membership function the nucleus is a single point and it is the height. It is very easy to implement a triangular membership function. The input signals are fuzzified and represented in fuzzy set notations by membership functions. There are 49 rules utilized here to produce the optimum control signal. The fuzzy rules are shown in table 1. The rules provide a functional mapping between the input and the output using linguistic variables. The foundation of a fuzzy mapping rule is a fuzzy graph, which describes the relationship between the fuzzy input and the fuzzy output.

<table>
<thead>
<tr>
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<th>MN</th>
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<th>S</th>
<th>SP</th>
<th>MP</th>
<th>LP</th>
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<td>PB</td>
<td>PB</td>
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<td>PM</td>
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<td>PM</td>
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<td>NM</td>
<td>NM</td>
<td>NB</td>
<td>NB</td>
<td>NB</td>
</tr>
</tbody>
</table>

The output of the fuzzy logic controller in d-q-0 frame is transformed back to a-b-c frame using inverse Park’s transformation which is the modulation signal for PWM generator. The modulating signal is shifted by an angle $\delta$, the angle between the presag and sag voltages. This shift enables the DVR to inject the compensating voltage in phase with the load voltage. Obviously the frequency of the modulating is 50Hz, whereas the magnitude and $\delta$ of it depend on the magnitude of the error (Ganesh SNV, et al., 2011; Leela, S., and S.S. Dash, 2009; KasuniPerera, 2006). In PWM generator the modulating signal is compared with 26
different carrier waveforms, arranged vertically, and whenever the magnitude of the modulation signal exceeds that of a carrier signal the gating pulses are generated to switch-on the corresponding bridge. The output of the multilevel inverter is injected into the bus bar to mitigate the sag or swell to maintain the load voltage constant so as to protect the sensitive loads (Mohan, D., Sreejith B. Kurub, 2012; Carrara, G., 1992). The schematic of a27 level H-bridge cascaded multilevel inverter, realized using 13 cascaded full bridge inverters with individual DC sources, to create the stepped waveform, is given in Fig. 3. The output of the multilevel inverter is the algebraic sum of the individual outputs of the full bridges. The upper two devices of \(i^{th}\) bridge are designated as \(S_i^1\) and \(S_i^2\) and those of the lower are designated as \(S_i^3\) and \(S_i^4\). When the bridge is in off mode all the four devices are in off state and the output of the \(i^{th}\) bridge is zero volts. The pair \(S_i^1\) and \(S_i^3\) or the pair \(S_i^2\) and \(S_i^4\) only will be on during on-mode and if the pair \(S_i^1\) and \(S_i^3\) is switched on the individual output of \(i^{th}\) module is \(+V_{\text{dc}}\) and on the other hand if the pair \(S_i^2\) and \(S_i^4\) is switched on the output of the same module is \(-V_{\text{dc}}\). To inject positive half cycle, the first pair of the modules 1 to 13 are switched on successively in a proper manner to generate the voltages 0, \(V_{\text{dc}}\), \(2V_{\text{dc}}\), ..., \(12V_{\text{dc}}\), \(13V_{\text{dc}}\) to raise the voltage from 0 volts to \(V_{\text{peak}}\) where \(V_{\text{peak}} = 13 \sqrt{2} V_{\text{im}}\) volts in a stepped manner and the modules are switched off in the reverse order so as to bring the voltage from \(V_{\text{peak}}\) down to 0 again in stepped manner, resulting the number of levels per half cycle is 27. For negative half cycle in the same manner the second pairs of the full bridge modules are switched on and off (Jose Rodriguez, et al., 2002; Lai, J.S., and F.Z. Peng, 1996; Jose Rodriguez, 2007; IlhamiColak, et al., 2011; Kazmierkowski, M.P., and L. Malesani, 1998; Rodriguez, J., et al., 2009; AnshumanShukla, ArindamGhosh and Avinash Joshi, 2011; Pedro Roncero Sanchez, 2009; Shukla, A., et al., 2008; Loh, P.C., et al., 2005).

**Modulation Technique:**

The performance of multilevel inverters of DVR in terms of switching losses, harmonic content and the like, mainly depend on the type of the modulation technique chosen to control the switches. Out of the two available strategies viz. fundamental frequency switching and high frequency switching techniques the latter is preferred in this work. The two major classifications of fundamental frequency technique, with respect to carrier signal, are vertical arrangement and horizontal arrangement. The three different kinds of vertical carrier distribution technique are phase disposition (PD), phase opposition disposition (POD) and alternate phase opposition disposition (APOD) whereas the only horizontal arrangement is known as phase shift (PS) control technique. The preferred switching strategy in this work for the inverters of the DVR is vertical carrier distribution fundamental frequency technique with multi carrier sinusoidal pulse width modulation technique (MCSPWM) and the DVR is simulated with all the three strategies i.e. PD, POD and APOD, to evaluate its performance (Leon, M., et al., 1999; Aglidis, and M.Calasis, 1998). In general, for all three techniques, if \(n\) is the number of levels of inverter, \(n - 1\) carrier signals, with same frequency and amplitude but at different phase are required and obviously \(n\) is an odd number. The carrier waves are disposed in such a way that they occupy contiguous bands. The maximum amplitude of the modulating reference and its frequency are taken as \(A_m\) and \(f_m\) respectively and those of carrier are \(A_c\) and \(f_c\) and the zero of the modulating reference waveform is centered in the middle of the carrier set as shown in Fig. 4. In case of PD modulating technique all the \(n - 1\) carrier waveforms are in-phase quantities where as in POD it is similar to PD except that lower half carrier waveforms are shifted by 180° with respect to upper half counterparts. In APOD the alternate carrier waveforms are shifted by 180° i.e. there will be a phase shift of 180° between any two adjacent carrier waveforms. Fig. 4, Fig.5 and Fig. 6 depict the three different carrier signals along with the modulating signal where \(n = 5\) and may be extended for any higher level (Leon, M., Tolbert and G. Thomas, 1999; Aglidis, and M.Calasis, 1998; Mcgrath, B.P., and D.G. Holmes, 2002). Instant of time the modulating signal is compared with each of the carrier signals and if the magnitude of the modulating signal is greater than that of a carrier signal, the gating signal for the corresponding switch is generated to switch it on and the gating signal is removed to switch it off otherwise.
Fig. 4: Carrier arrangement for PDPWM

Fig. 5: Carrier arrangement for PODPWM

Fig. 6: Carrier arrangement for APODPWM
Fig. 7: Simulation model for Multilevel Inverter based DVR

Simulation of DVR:

A three phase distribution system has been chosen in this work to demonstrate the capabilities of the proposed 27 level H-Bridge based DVR using multicarrier SPWM techniques for mitigating voltage sags and swells. The simulation block diagram of the proposed scheme is given in Fig.7. The entire system is simulated in MATLAB–Simulink. Voltage sag of 30% i.e., bringing down the supply voltage to 290 Volts from 415 Volts, is introduced at 0.3 second, which lasts for 200 milliseconds and a voltage swell is introduced at 0.7 second, with a magnitude of 500 Volts i.e. 20% swell, which lasts for 200 milliseconds as shown in Fig. 8.

Fig. 8: Supply voltage with 30% sag and 20% swell

The simulation parameters are shown in Table I and the total simulation period is 1 second.

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Description</th>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Voltage Source</td>
<td>Line Voltage</td>
<td>415 V</td>
</tr>
<tr>
<td>2</td>
<td>Filter</td>
<td>Filter Inductance</td>
<td>38mH</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Filter Capacitance</td>
<td>20µF</td>
</tr>
<tr>
<td>3</td>
<td>Injection Transformer</td>
<td>Power</td>
<td>7.5 KVA</td>
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<tr>
<td></td>
<td></td>
<td>Voltage Rating</td>
<td>415/415 V</td>
</tr>
<tr>
<td>4</td>
<td>Load</td>
<td>Load Resistance</td>
<td>20 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Load Inductance</td>
<td>10mH</td>
</tr>
<tr>
<td>5</td>
<td>PI Controller</td>
<td>Proportional Gain(Kp)</td>
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<td></td>
<td></td>
<td>Integral Gain(Ki)</td>
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<td>6</td>
<td>Carrier Signal</td>
<td>Triangular Wave</td>
<td>Vp = 1 V</td>
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<td></td>
<td></td>
<td></td>
<td>20 kHz</td>
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RESULTS AND DISCUSSIONS

It is observed from the simulation that during the sag period, i.e., from 0.3 second to 0.5 second, the error voltage is 125 Volts. The swell is between 0.7 second to 0.9 second with the error amplitude of 85 Volts and both sag and swell are shown in Fig.9. The error signals are fed to fuzzy logic controller and the outputs from the fuzzy logic controller for sag and swell are shown in Fig.10. It may be noticed that the output of fuzzy logic controller for swell is 180 degree out of phase to that of sag and hence, it may be easily concluded that for the $i^{th}$ bridge, if pair $S_i^1-S_i^2$ is selected during sag to inject positive voltage the pair $S_i^3-S_i^4$ will be selected during swell to inject negative voltage. The output of fuzzy logic controller is in d-q-0 frame and is transformed into a-b-c frame and the a-b-c transformed waveform is 50 Hz sinusoidal as shown in Fig.11, which is the modulation signal for PWM generator.

![Fig. 10: Fuzzy Logic controller output](image)

![Fig. 11: Modulating signal for MC SPWM generation](image)

It is observed that for the present 30% sag the peak magnitude and phase of the modulating signal are 1100 Volts and $\delta$ is $9^\circ$ respectively and for 20% swell the same are respectively 680 Volts and $198^\circ$. The performance of the DVR is simulated with all three modulating techniques viz. PDPWM, PODPWM and APODPWM. Irrespective of the phase shift among the adjacent and/or upper and lower half carrier signals the functioning of DVR remains same. Hence, the functioning of the DVR and the outcome of it are discussed with respect to APODPWM only and may be extended for the remaining two techniques also. The thirteen 20 kHz, 1 V peak carrier signals are arranged vertically in tandem. During the positive half cycle, the 50 Hz modulating signal raises sinusoidally between $\omega t = 0$ and $\pi/2$ and crosses all the 13 carrier signals in succession. During this phase, once the modulating signal crosses a carrier, the gating pulse for the corresponding bridge is generated to switch-on that particular bridge so as to increase the magnitude of the DVR output by the factor $V_{dc}$. Between $\omega t = \pi/2$ and $\pi$ the modulating signal falls, resulting the switching-off the bridges in the reverse order which brings down the DVR voltage to zero. During the negative half cycle of the modulating signal, the same process is repeated to generate the negative half of the compensating voltage. The generated gate pulses by MCPWM and the compensating voltages for all the three phases are given in Fig. 12 and Fig. 13 respectively. The magnitudes of the compensating voltage injected are directly proportional to the magnitudes of the corresponding error voltages, which is also evident from Fig.13.
From Fig. 14 it is observed that the sag and swell are completely compensated with the proposed DVR, bearing negligible glitches during the on and off moments of the DVR. The quality of the energy in the system is measured in terms of the magnitude of the line voltage during disturbances, load power factor and THD. These performance metrics for all the three modulating techniques are estimated and given in Table II. The THD waveforms of all the three modulating techniques are shown in Fig. 15, Fig. 16 and Fig. 17.
Table II: Thd Analysis For Inverter Modulation Techniques

<table>
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<th>System</th>
<th>RMS load Voltage</th>
<th>Load PF</th>
<th>% THD</th>
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</thead>
<tbody>
<tr>
<td>DVR with APOD using PI Controller</td>
<td>382</td>
<td>0.85</td>
<td>6.3</td>
</tr>
<tr>
<td>DVR with APOD using Fuzzy logic Controller</td>
<td>412</td>
<td>0.93</td>
<td>3.4</td>
</tr>
</tbody>
</table>

Conclusion:

A 27 level H-bridge inverter based DVR has been proposed in this paper to mitigate the voltage sags and swells in a three phase distribution system. The proposed DVR has been designed, simulated and the performances of it with three different types of modulating techniques have been estimated. The performance of the proposed DVR has been estimated using the metrics supply voltage, load power factor and THD and tabulated in Table II. It is observed from Table II that the performance of DVR with APOD using fuzzy logic controller is better than DVR with PI controller. It may also be noted that only DVR with APODPWM using fuzzy logic controller compensates the both voltage sag and swell completely and the other technique also fair well in this aspect. However, the magnitudes of the harmonics vary, the maximum is found in case of PDPWD, minimum in APODPWD and PODPWD falling in between. Further, it is observed that APODPWM with fuzzy logic controller only complies with IEEE standards where as the other fail to satisfy. Hence, it may be concluded that APODPWM using fuzzy logic controller is best suited for the proposed DVR. The Fuzzy logic controllers may be replaced by stochastic controllers such as, Neural Network controllers and the like to improve the overall performance of the DVR with all the three modulating signals.

REFERENCES


