# Harmonic Reduction for Diode Clamped and Cascaded H-Bright, Five to Nine Levels of Multilevel Inverters Application

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**A R T I C L E   I N F O**

**A B S T R A C T**

This paper presents a comparative study of two types of multilevel inverters, comprises of diode clamped and cascaded H-Bridge multilevel inverter for reduction of harmonics in the multilevel inverter output. The proposed system is designed using MATLAB/SIMULINK and it consists of diode clamped and cascaded H-Bridge multilevel inverters. The controller is based on the pulse width modulation (PWM) technique which is applied to the purposed three phase multilevel inverters. The various performances of simulation results of the diode clamped and cascaded H-Bridge multilevel inverters have been investigated. The Total harmonic distortion (THDv) of the output voltage is measured for the two types of multilevel inverters. Based on varying simulation results, it is found that the THD voltage of the H-Bridge multilevel inverter is considerably lower than the diode clamped multilevel inverter.

## INTRODUCTION

Nowadays, multilevel inverters have become more attractive for their use in high-voltage and high-power applications. Multilevel converters (or inverters) have been used for ac-to-dc, ac-to-dc-to-ac, dc-to-ac, and dc-to-dc power conversion in high power applications such as utility and large motor drive applications (F. Peng, 2001). Multilevel inverters provide more than two voltage levels. The generalized multilevel inverter topology can balance each voltage level by itself regardless of inverter control and load characteristics the concept of multilevel converters has been introduced since 1975 (P. Karuppanan, 2011).

Converting static structures that comprise mainly applications of power electronics are becoming increasingly powerful, the technology has had to adapt to the growth of the power to convert. This growth has been possible thanks to the development of technologies of semiconductor components. Changing templates voltage and current as well as improved performance of these components has to use more power electronics performance for applications of greater power (I. Colak, 2010).

To solve this problem and using more efficient components, new structures have been developed. These structures are known as multilevel inverters they have more than two output voltage levels at the output. Created in a first time to be able both to several switches in series and ensure properly withstand voltage across them later, these inverters showed interesting properties of the output waveforms The rotary electric actuators play a very important role in the industry and particularly in electric traction. The performance required for these actuators are higher and higher, both in terms of the dynamics of the speed of the precision of torque delivered (Y. Zou, 2004).

The DC machine has been used to make the most of these actuators given the simplicity the order. However, the current machine has several drawbacks associated with its mechanical commentator. In contrast, AC machines (synchronous and asynchronous) possess many advantages. The absence of collector allows them to have a smaller footprint, increased reliability and high operating speed.

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Indeed, the permanent magnet synchronous machine is distinguished by its excellent performance and its large mass couple is allowed to prevail in applications require very high static and dynamic performance, particularly in areas of applications such as flexible manufacturing systems, robotics, aeronautics and space. The emergence and development of new components controllable powers opening and closing as the GTO (gate turn-off thyristor) and IGBT (insulated gate bipolar transistors) allowed the design of new converters reliable, fast and powerful. Thus, all drives (static machine converter current AC) saw costs are reduced considerably.

Progress in the field of the microcomputer (fast and powerful microcontrollers) allowed the synthesis control algorithms of these sets more efficient converter machine and robust (a. Chen, 2004). The Pulse Width Modulation (PWM) is a technique to control static converters for interfacing between a load (electrical machine) and supply means (three-phase inverter). It is a technique used for energy conversion, having its base in the field of telecommunications (signal processing). It bears the English name of Pulse Width Modulation (PWM) or Pulse-Duration Modulation (PDM), using a name older. Far from being an accessory element in the chain of variable speed (inverter power associated with an electric machine), the PWM stage plays an important role with impact on the performance of all system performance driving, loss in the inverter or in the machine, the acoustic noise, electromagnetic noise, even the destruction of the system, eg due to over voltages which occur during the use of long cables (Du et al. 2007). Multilevel inverters have three topologies Cascaded H-bridge (CHB) Diode–Clamped (NPC) Flying Capacitors (FC) Cells with separated DC sources shown in Figure.1.
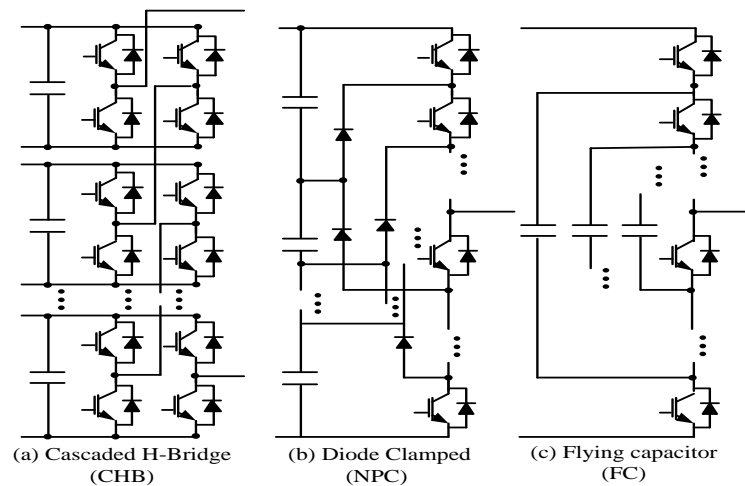


(a) Cascaded H-Bridge (CHB)    (b) Diode Clamped (NPC)    (c) Flying capacitor (FC)

**Fig. 1:** Topologies of Multilevel Inverter, (a) Cascaded H-Bridge (CHB), (b) Diode Clamped (NPC) (c) Flying Capacitor (FC).

The Concepts of multilevel inverters (MLI) depends not only on two voltage levels to create the AC signal. Instead, it is added to most levels of voltage to the other to create a form of the reinforced smooth wave, show Figure 2, with a low dv/dt and less harmonic distortion. With more in the inverter voltage levels, it creates a smoother waveform becomes, but with many levels of design becomes more complex, with more components and must be a more complex controller for inverter.
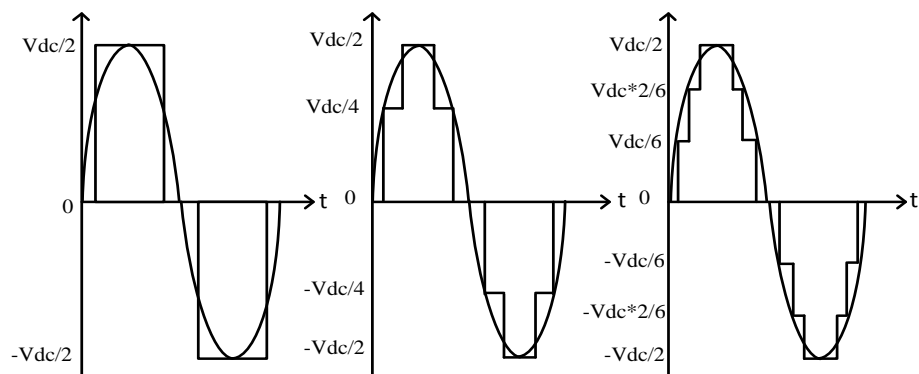


**Fig. 2:** A three-level waveform, a five-level waveform and a seven-level multilevel.

***Control Techniques Pulse Width Modulation (PWM):***

Multilevel inverters and attract the attention of researchers, the demand for power adapters that are suitable for high power applications high voltage increase due. Multilevel inverters achieve high voltage switching through a series of work steps. One of the most important problems in the control of multi-level inverter is to get a variable amplitude and frequency sinusoidal output using a simple control technique. A first impression of multilevel converters is that a large number of switching may cause the switch configuration of complex algorithms. However, proved the first developments in this area is relatively simple nature of the multi-level inverters. Under side to reduce the harmonic content, several inverters are the highest levels of importance (B. F. O. W. Drive, 2013).

It is generally accepted that the performance of the inverter, with strategies for change may be related to the harmonic content of the output voltage to it. The researchers studied power electronics are always the most innovative control techniques for reducing harmonics in this wavelength. Many techniques are applied to the inverter topology. Control technologies can be divided into multi-PWM inverter technology and selective harmonic elimination car. This section presents the methods, and reviews some of the basic research of the novel that appeared in this area (Y. Tang, 2013). This is accomplished regular PWM inverters modified two levels through the comparison between the carrier wave and triangular wave signal. Wave signal has a frequency, necessary amplitude for the signal output voltage, and the triangular carrier wave has a capacity of a continuous input, in the case of ordinary single half DC voltage, and frequency dependent on the application, but must be higher than the signal frequency of the wave. In the application of electrical energy and the carrier, frequency is often of the order of kHz (M. S. Bakar, 2010).

Decides signal wave frequency how often the switches to the inverter changes state, whenever the triangular carrier wave reflected wave signals switches on or off. Can be found on the grounds of the PWM signal to two ordinary levels, the output voltage of the carrier wave in Fig3. If a cross reference of the carrier wave such that the top of the switch signal O upper switch and turns downwardly into the two-level inverter, so that Vdc/2 and becomes the output. When the carrier passes through the reference again, and receives much less than the signal, change status and become switches output -Vdc/2. When the signal is positive, the output voltage is Vdc/2 for most of the time, which leads to an alternating current signal to output a positive AC signal. A simple example is that if the wave is the constant reference voltage to zero, the carrier wave, and then he went up and down with the same time between each passage, which makes the Vdc/2 and -Vdc/2 being for equal time, each session. This leads to the average output voltage over a single carrier wave becomes zero (S. M. Cherati, 2011).
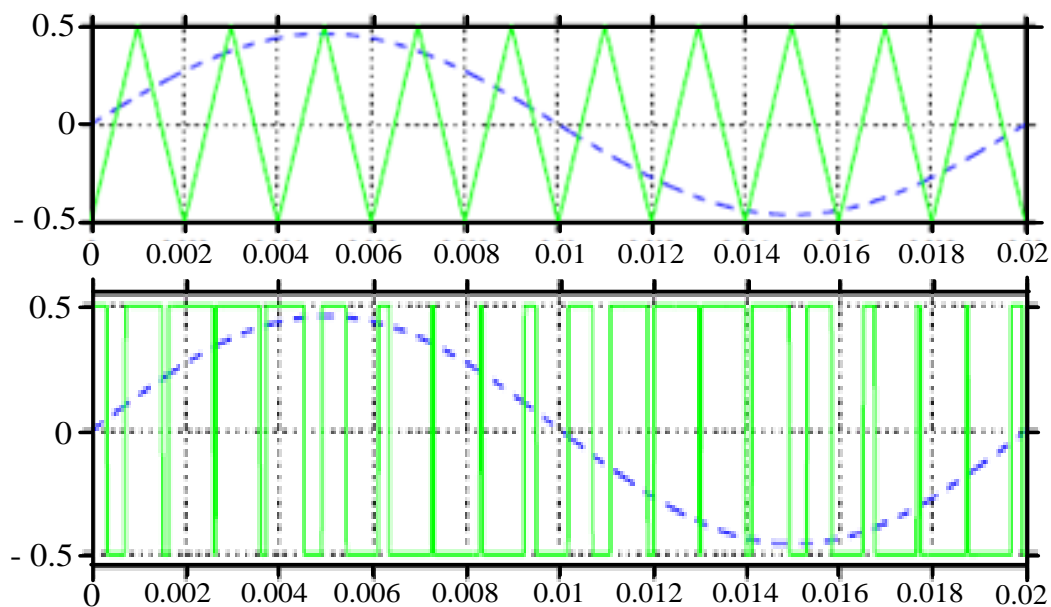


**Fig. 3:** PWM reference (blue dashed) and triangular carrier (green solid) wave in upper plot and output voltage (green solid) eave in lower plot.

***Sinusoidal Pulse-Width Modulation:***

The generations of gating signals with sinusoidal Pulse Width Modulation SPWM are shown in Fig. In addition, all this can be implemented using the building blocks of chips and one or more available on the market, however, the implementation of such an analog circuit comes with various problems commonly

associated with analog circuits. The peak of the output voltage of the converter using depends SPWM modulation index. One can obtain a higher output voltage by increasing the modulation index to "0.95". However, the sinusoidal PWM output shows weakness when the modulation index is near "0.95". This is because the pulse widths that are near the peak of the sine wave do not vary significantly with changes in the composition of the index, because of the characteristics of a sine wave (E. Engineering, 2012). The idea is to use multiple triple signals, sinusoidal signal and modify one. And this technique can be widely applied to supporters of the N-level, and there will be a need Airlines N-1. Carriers have the same frequency and the same peak-to-peak, and are willing to take contiguous poets. Sinusoidal signal has a frequency change of the output voltage. The intersections of the signal modulating the wavelength of the triangle are the points of the switch.

       If the modulation of higher unit triangle support set to "on" position signal, and if the reference configuration is less than the carrying unit Triangle Generation to the "off" position results to give the level of effort that is needed in the production plant (N. Kashappa, 2011).
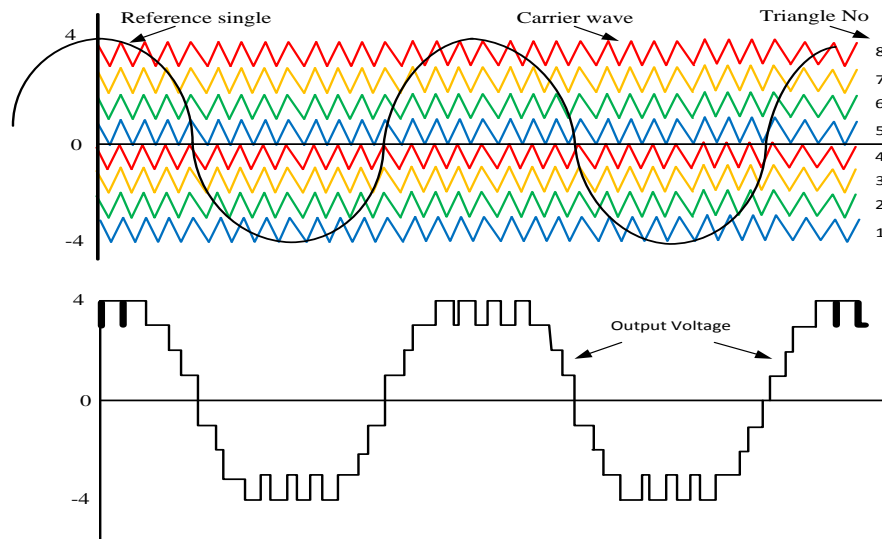


**Fig. 4:** Sinusoidal Pulse-Width Modulation for Nine levels Inverter (J. Huang, 2006).

***Topologies Multilevel Inverter:***
***A.    Multilevel Diode Clamped/Neutral Point Inverter, NPCMLI:***
       This inverter was later derived into the Diode Clamped Multilevel Inverter, also called Neutral-Point Clamped Inverter (NPC), show Figure 4. NPCMLI topology and the use of voltage limiting diodes are essential. Shared DC bus is divided by an even number, depending on the number of voltage levels of the inverter and the majority of capacitors in series with the neutral point in the middle of the line see the left side of Figure 4. Inverter one leg present on five levels NPC. By adding two identical circuits arranged three phase legs together can generate three-phase DC-bus signals where sharing is possible. In, Table 1 is showing the various states of the inverter NPC on five levels. Note that there is a possibility to convert only on (and off) each switch once for each session, which means that the inverter can generate a sine wave form with a stepped frequency switch fundamental (A. H. T. 2013).
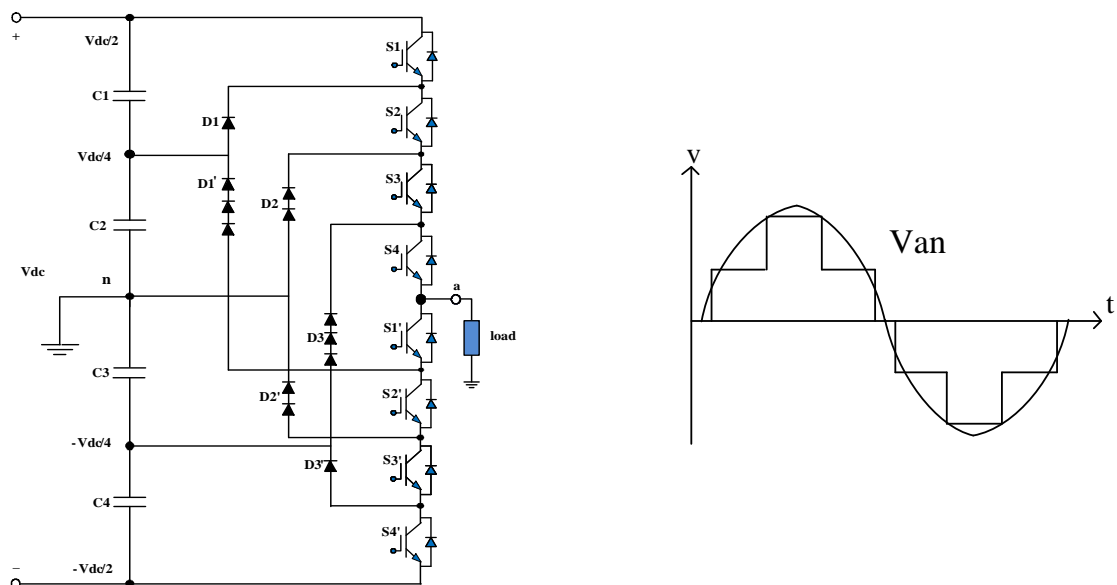
**Fig. 4:** One phase-leg of a five-level NPC Inverter.

**Table 1:** Switching states of one five-level phase leg.

| Output voltage | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_1^{'}$ | $S_2^{'}$ | $S_3^{'}$ | $S_4^{'}$ |
|---|---|---|---|---|---|---|---|---|
| Vdc/2 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| Vdc/4 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| -Vdc/4 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| -Vdc/2 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

### B.  Cascaded H- Bridge Multilevel Inverter, CMBMLI:

The total output voltage is the sum of the outputs of all units of the full bridge inverter and all the H-bridge can create three voltages VCHB, 0 and - VCHB. To change the level of a voltage to the output phase CHBMLI rotates on a switch (one off) in an H-bridge unit show in figure 5. Unit for voltage H-bridge to add the VCHB $S_1$ and $S_4$ turned on -VCMC switch is turned on $S_2$ and $S_3$. When it is due to the current through the bridge complete 0 voltage is obtained by running two buttons on the top half of the full bridge ($S_1$ and $S_3$).and ($S_2$ and $S_4$). With a large number of H-bridges can be generated waveform (D. Based, 2012). The maximum output voltage is (m-1)/2 VCHB = s VCHB = Vdc/2 (and minimum voltage m-1 2 (-VCHB) = s (-VCHB) = - Vdc/2), where m is the number of levels and the number of H-bridge modules. It should be noted that CHBMLI unable to suppress the total volume of the voltage source in the direction of positive and negative alike, while many other topologies can make that half of the total DC-bus voltage source (M. S. Rosli Omar, 2013).
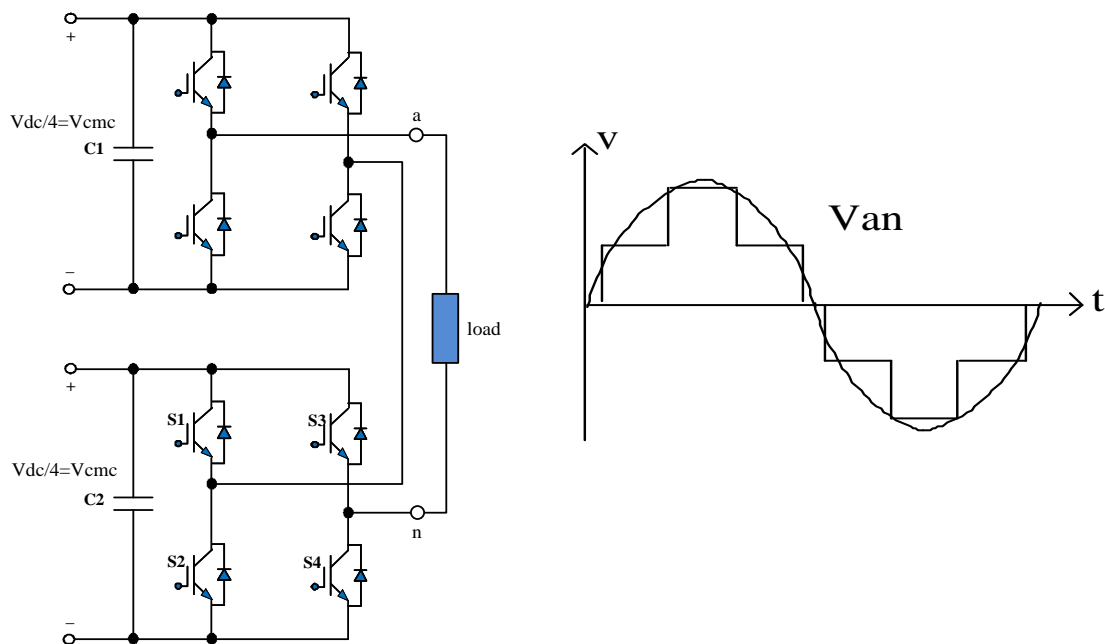


**Fig. 5:** A five-level Cascaded Multilevel Inverter.

### Study of Mutlilevel Inverter Based on Matlab/Simulink Modeling:

This paper describes the study of the three phase diodes clamped and cascading H-Bridge in multilevel inverters using MATLAB/SIMULINK. It describes the layout of the proposed multilevel inverters to simulate the step-by-step procedure to build the simulation model. MATLAB / Simulink version 7.8 was used to model, analyse and Simulink for five to nine levels for modelling, simulation and analysis. It supports the systems, as in the time of linear, time samples and non-linear, constantly. As for the model, Simulink provides the construction of models and diagrams. Control block generates a PWM signal is given to the new level inverters for reduce total harmonic distortion can be calculated using equations (3.1, 3.2, 3.3).

$$THD_{.} = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}^2}}{H_1} \qquad (1)$$

Where: $H_1$ is the amplitudes of the fundamental component, whose frequency is w0 and $H_n$ is the amplitudes of the nth harmonics at frequency nw0

$$h_n = \frac{4E}{n\pi} \sum_{k=1}^{s} \cos(n\alpha_k) \qquad (2)$$

$$h_n = \frac{4E}{n\pi} \sum_{k=1}^{s} \cos(n\alpha_k) \, let H_{(n)} = h_n \, and H_1 = h$$

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} (\frac{1}{n} \sum_{k=1}^{s} \cos(n\alpha))^2}}{\sum_{k=1}^{s} \cos(n\alpha_k)} \qquad (3)$$

The generations of gating signals with sinusoidal Pulse Width Modulation (SPWM) are shown in Figure (a). There are sinusoidal reference waves ($\upsilon_{ra}, \upsilon_{rb} \, and \, \upsilon_{rc}$) and each is shifted by $120^0$. A carrier wave is compared with the reference signal corresponding to a phase to generate the gating signal for that phase. Furthermore, when comparing the carrier signal $\upsilon_{rc}$ with the reference phase $\upsilon_{ra}, \upsilon_{rb} \, and \, \upsilon_{rc}$ it produced $g_2$ and $g_5$, respectively as shown in Figure (b). The instantaneous line-to-line output voltage is $\upsilon_{ab} = Vs(g1 - g3)$. The output voltage as shown in Figure (c), is generated by eliminating the condition that two switching devices in the same arm cannot be conducted at the same time. The normalized carrier frequency, $mf$, should be odd and multiplied by three. Thus, all phase-voltage ($\upsilon_{ra}, \upsilon_{rb} \, and \, \upsilon_{rc}$) were identical, but $120^0$ out of phase was without even harmonics; moreover harmonics at frequency multiplier of three were identical in amplitude and phase in all the phases. For instance, if the ninth harmonic voltage in phase *a* is

$$\upsilon_{aN9}(t) = \upsilon^\sim 9 \sin(9wt) \qquad (4)$$

The corresponding ninth harmonics in phase *b* will be,

$$\upsilon_{aN9}(t) = \upsilon^\sim 9 \sin(9wt - 120)) = \upsilon^\sim 9 \sin(9wt - 1080)) = \upsilon^\sim 9 \sin(9wt) \qquad (5)$$

Thus, the ac output line voltage $\upsilon_{ab} = \upsilon_{aN} - \upsilon_{bN}$ does not contain the ninth harmonics. Therefore, for the odd multiples of three time of the normalized carrier frequency $mf$, the harmonics in the ac output voltage appeared to be at a normalized frequency $fh$ centred around $mf$ and its multiple, specifically, at

$$n = jmf \pm k \qquad (6)$$

$$n = jmf \pm k \pm 1 \qquad (7)$$

Besides, it is considered as good quality for the output voltage if the modulation index (MI) is in the range of 0 to 0.95. In the case of MI is greater than 0.95, there is a direct correlation between the anti-wave quality and amplitude of the output voltage if the quality decreases, and then increases the output voltage wave size. The SPWM technology has its limitations regarding the maximum voltage that can be achieved, and the transfer of power. In the case of a three-phase inverter, the proportion of the main ingredient to the line of maximum possible line voltage to a DC supply voltage is 86.6% and this indicates the use of poor DC power supply. Besides, the SPWM is an effective way to reduce the lower harmonics of the system while varying the output voltage. However, the low-frequency harmonic content is in minimum value.

### A. Modeling Diode Clamp Multilevel Inverter:

The simulation study was based on the parameters of the diodes clamped in multilevel inverters, as shown in Table 2. Figure 7 five levels SPWM diode clamped multilevel inverter. The building techniques consisted of Thyristor and all the simulation systems were modelled show in Figure 8 using the MATLAB/SIMULINK. In this simulation, a fixed SPWM was used. In addition, the GTO switches were used in the diode clamped (NPC) Thyristor. The carrier frequency ($f_c$) used in this design was around 2500 Hz.
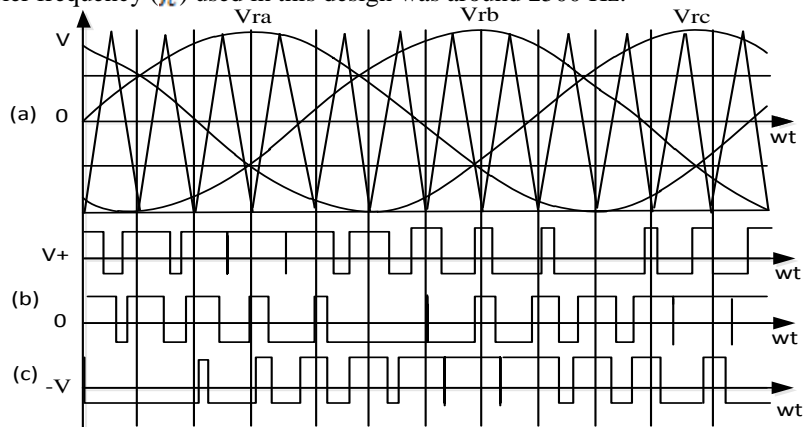


**Fig. 6:** Sinusoidal Pulse Width Modulation for three-phase inverter.
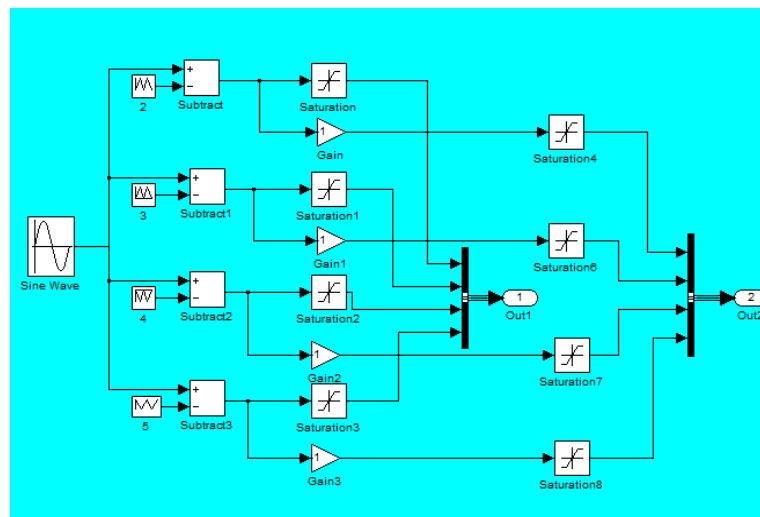


**Fig. 7:** Simulink Multilevel Inverter diagram with Five Levels of control signal generated by Clamped Diodes.

**Fig. 8:** Switching GTO Thyristor for five Levels with Diodes Clamped in Multilevel Inverter.
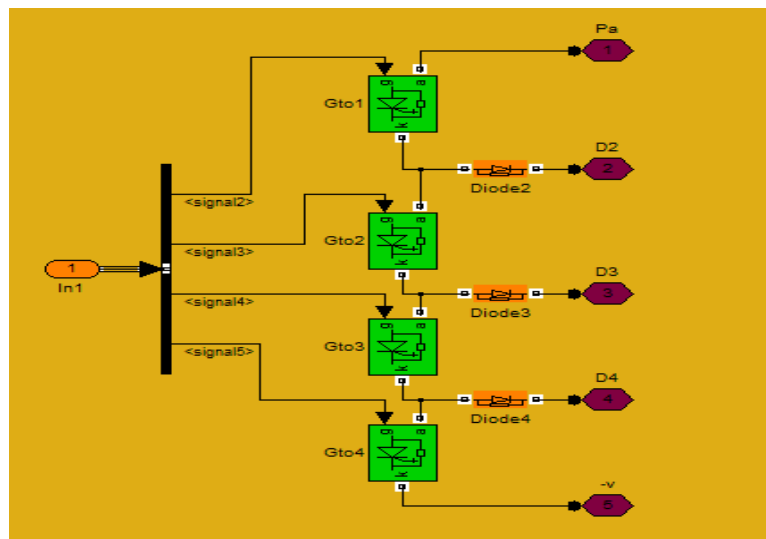
**Table 2:** Parameters of Diode Clamped Multilevel Inverters (NPC).

| Parameters | Value |
|---|---|
| Modulation Index | M =0.95, 0.8 |
| DC Voltage | Vdc =100V |
| Output Frequency | 50 Hz |
| Carrier Frequency | 2500 |
| GTO Thyristor | 8 One bloke - 48 switches, |

### B. Modeling Cascaded H-Bridge Multilevel Inverter:

The simulation study carried out a three-phase Multilevel inverters behaviour based on a three-phase Cascaded H-Bridge that was developed and the parameters are as shown in Table 2. In 9 shows the nine levels of building a multilevel inverter model with MATLAB/ SIMULINK simulation diagrams for the five and seven levels, similarly, in one block. In this simulation, the constant SPWM, and 4 in one bloke switches GTO in the Cascaded H-Bridge (CHB) Thyristor were used. The carrier frequency used in this designed was about 2500 Hz.
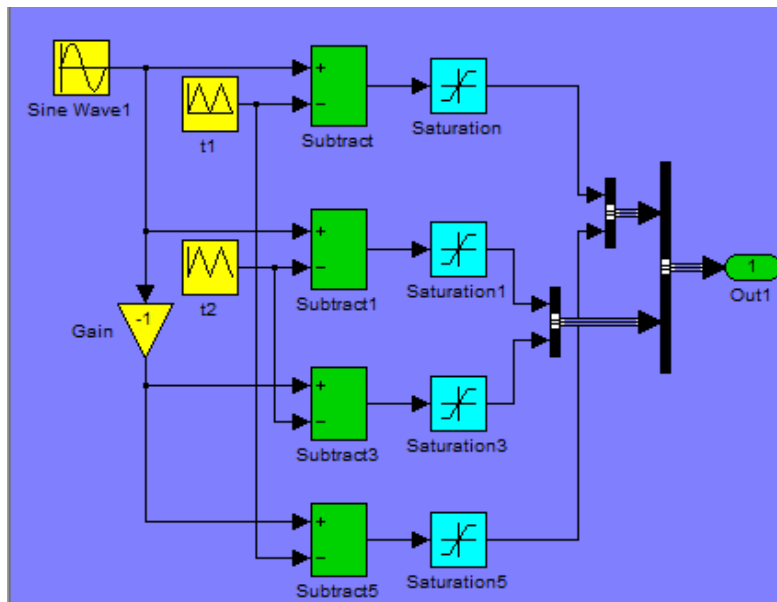


**Fig. 9:** Simulink with Five Level of control signal Cascaded H-Bridge in Multilevel Inverter.
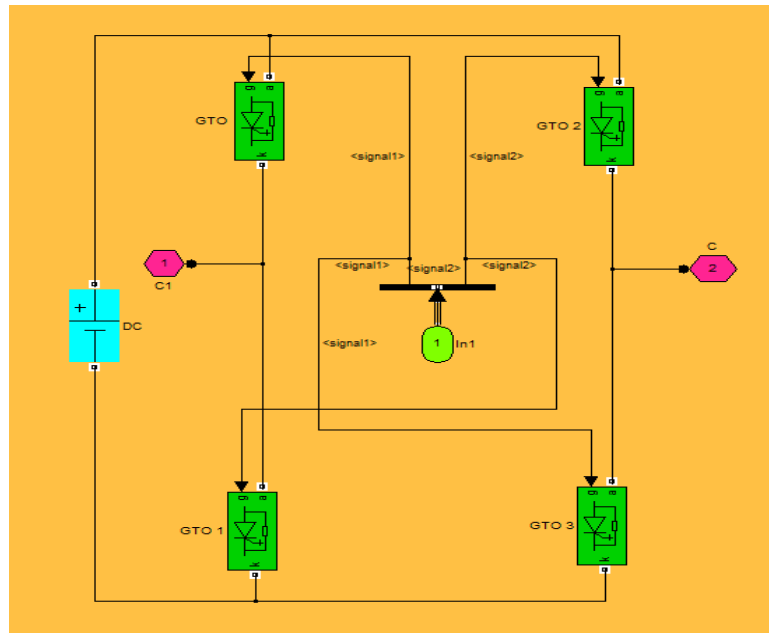
**Fig. 10:** Switching GTO Thruster for Nine Levels with Cascaded H-Bridge in Multilevel Inverter.

***Harmonic Reduction by Increasing the Number of Voltage level***

This paper explains the strategy of amplitude modulation for multilevel converters which generate a greater number of levels with high voltage inverter. It had been studied in comparative studies between the two types of multilevel converters. The output line voltage of the diodes clamped (NPC) was slightly higher than the line voltage output with H-bridge cascade (CHB) in multilevel inverters due to longer losses experienced in the clamped diodes. However, the THDv from both the converters and the multilevel values were reduced to follow the IEC standard.

Reduction of harmonics in multilevel converters could not be achieved by increasing the number of levels of the staircase wave form output. THD was produced less by increasing the number of voltage sources. The effective values of the output voltage depended on the number of units in a multilevel inverter. The switching pattern that was used in this dissertation for all of the multilevel inverters was indeed a harmonic elimination method. In this method, the switching angles for the switches were calculated in such a way that the lower dominant harmonics were eliminated. In this study, the cases of 5-level, 7-level and 9-level multilevel inverters were investigated. For the 5-level inverter, the 5th harmonic was eliminated. On the other hand, as for the 7-level inverter, the $5^{th}$ and the $7^{th}$ harmonic were removed. Lastly, in the 9-level inverter, the $5^{th}$, $7^{th}$ and $11^{th}$ harmonics were eliminated. The Fourier analysis was conducted to determine the frequency spectra of the output wave form.

The equations for level five that was based on Fourier series, are described below(8-9).

$$f\left(t\right) = f_{\theta 1}\left(t\right) + f_{\theta 2}\left(t\right) = \frac{2V_{dc}}{\pi}\sum_{h=1}^{\infty}\left[\cos\left(h\theta_1\right) + \cos\left(h\theta_2\right)\right] \qquad (8)$$

$$\frac{3V_{dc}}{\pi}\sum_{h=1}^{\infty}\left[\sum_{i=1}^{3}\left[\cos\left(h\theta_i\right)\right]\frac{\sin\left(hwt\right)}{h}\right] \qquad (9)$$

In the case of 7-level multilevel inverter, the common equations are described below (10-12).

$$f\left(t\right) = f_{\theta 1}\left(t\right) + f_{\theta 2}\left(t\right) + f_{\theta 3}\left(t\right) \qquad (10)$$

$$\sum_{h=1}^{\infty}\left[\cos\left(h\theta_1\right) + \cos\left(h\theta_2\right) + \cos\left(h\theta_3\right)\right] \qquad (11)$$

$$\frac{3V_{dc}}{\pi}\sum_{h=1}^{\infty}\left[\sum_{i=1}^{3}[\cos(h\theta_i)]\frac{\sin(hwt)}{h}]\right] \tag{12}$$

The model of 9-level in the multilevel inverters was investigated using the following equations: (13-15).

$$f(t) = f_{\theta 1}(t) + f_{\theta 2}(t) + f_{\theta 3}(t) + f_{\theta 4}(t) \tag{13}$$

$$\sum_{h=1}^{\infty}\left[\cos(h\theta_1) + \cos(h\theta_2) + \cos(h\theta_3) + \cos(h\theta_4)\right] \tag{14}$$

$$\frac{4V_{dc}}{\pi}\sum_{h=1}^{\infty}\left[\sum_{i=1}^{4}[\cos(h\theta_i)]\frac{\sin(hwt)}{h}]\right] \tag{15}$$

Where;
Vdc: Voltage of voltage sources for each cell was in unity
$\theta i$: The switching angle
h: The harmonic order

***Simulation Result and Discussion Multilevel Inverter:***
In order to validate the performance of the proposed schemes, a simulation model for a three-phase diodes clamped, and Cascaded H-Bridge in Multilevel inverters were developed. The parameters of the both multilevel inverters are as shown in the MATLAB/SIMULINK simulation diagrams. In this simulation, the constant SPWM was used. In diodes clamped configuration, it used 8 switches of GTO in one bloke Thyristor, while in Cascaded H-Bridge, it required 48 switches of GTO; 4 switches of GTO in one bloke Thyristor. The carrier frequency used in these designs was about 2500 Hz.

***A.   Diode Clamped Multilevel Inverter Results:***
The simulation result is shown in Figure 11. As for the five-level diodes clamped in the multilevel inverter, the output voltage wave form for line to neutral with Modulation Index was equal to 0.95 and the output voltage was 167.6 V RMS in value. When the Modulation Index decreased to 0.8, as shown in Figure 12, the inverter output voltage was equal to 158.7 V RMS. The number of steps for both the figures were 5 (*n*=5) for the quarter wave and  in the case of full wave, the number of steps was 10 (2*n*=10,*n*=5).The simulation result  is shown in Figure 13, for the five-level diodes clamped in the multilevel inverter. The output voltage wave form for line to line in the of number of steps in this level increased to 10 for the quarter wave and 20 steps for full wave, with the Modulation Index equal to 0.95, whereas, the output voltage produced 285.5 V RMS. When the Modulation Index decreased to 0.8, the output voltage value was equal to 272.6 V RMS. The number of steps used was similar, as in Figure 14.
The THD$_V$ for voltage for the five level output diodes clamped in the multilevel inverter was measured when the Modulation Index was equal to 0.95. It was found that the value of THD$_V$ for voltage was around 7.21%, as shown in Figure 15. Furthermore, FFT analysis is shown in Figure 16 for the five level Diodes clamped in the multilevel inverter output. The THD$_V$ for voltage obtained from the output of diodes clamped in the multilevel inverter when the Modulation Index was equal to 0.8, was actually lower when the Modulation Index was equal to 0.95 and its value was 7.06%.
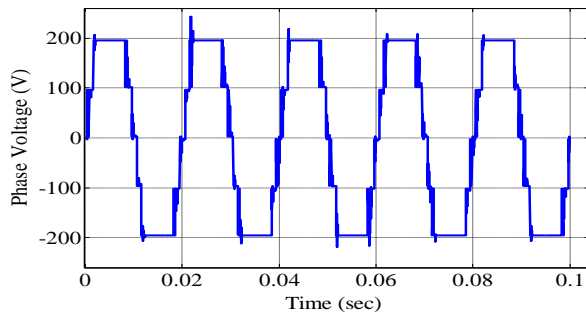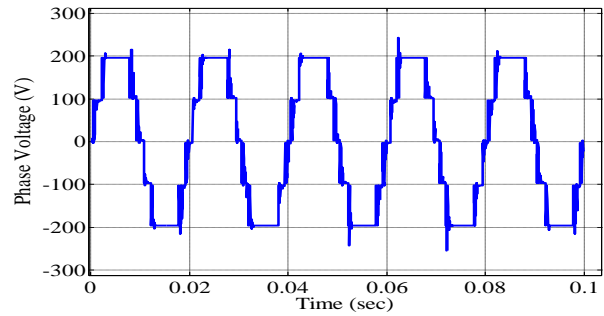
**Fig. 11:** Phase Voltage of MI=0.95.
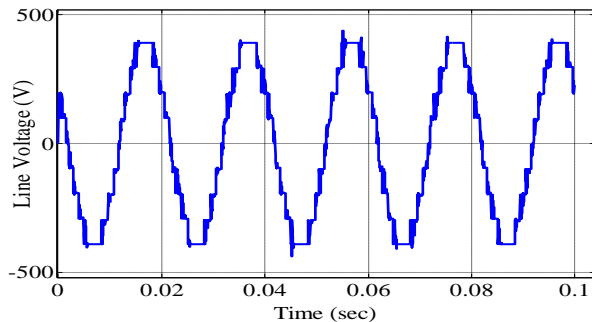


**Fig. 12:** Phase Voltage of MI= 0.8.



**Fig. 13:** Line Voltage of MI=0.95.
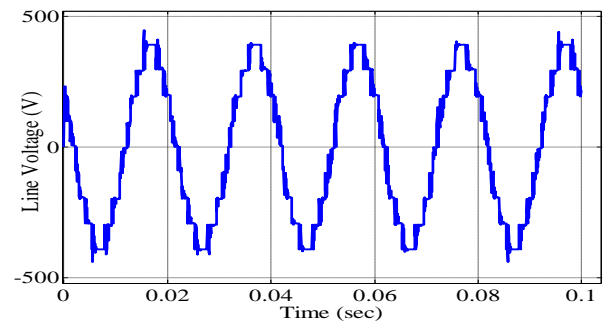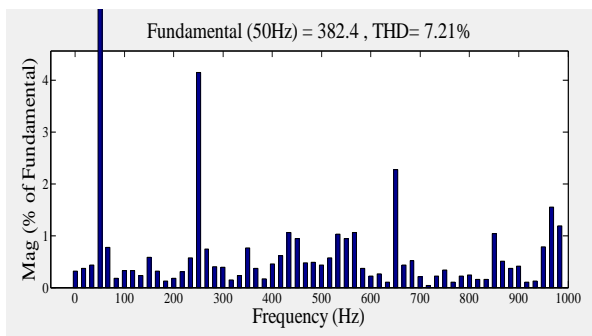


**Fig. 14:** Line Voltage of MI=0.8.



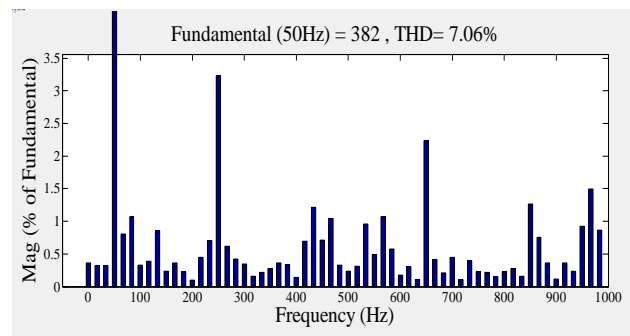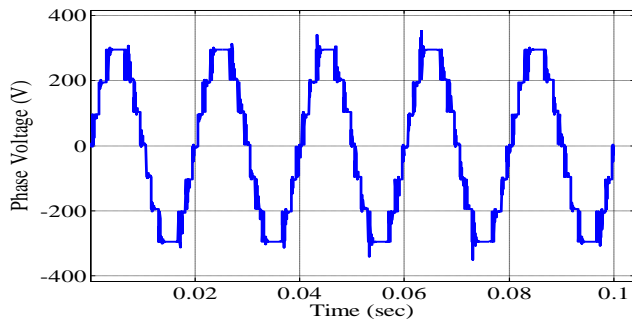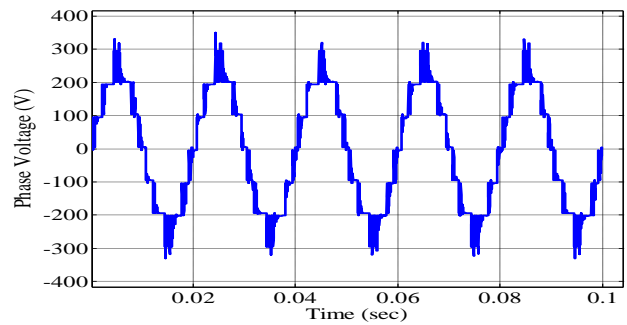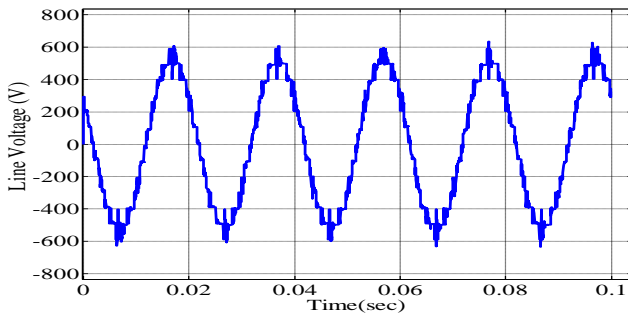**Fig. 15:** Harmonic Voltage of MI=0.95.



**Fig. 16:** Harmonic Voltage of MI=0.8.

The simulation result is shows in Figure 17. for the Seven-level diodes clamped in the multilevel inverter. The output voltage wave form for line to neutral with the Modulation Index was equal to 0.95, as shown in Figure 18, and the output voltage was 216.4 V RMS. The Modulation Index decreased to 0.8 as the inverter output voltage was equal to 174.1 V RMS. The number of steps for both the figures were 7 (*n*=7) for the quarter wave and in the case of full wave, the number of steps was 14 (2*n*=14,*n*=7). Next, the simulation results for the Seven-level diodes clamped in multilevel inverter showed that the output voltage wave form for line to line in the number of steps increased to 14 for the quarter wave and 28 steps for the full wave, with Modulation Index equal to 0.95, as shown in Figure 19. The output voltage produced was about 373.6 V RMS. When the Modulation Index decreased to 0.8, the output voltage value was equal to 300.1 V RMS. The number of steps used was similar as in Figure 20.

The $THD_V$ for voltage of the seven level output for the diodes clamped in multilevel inverter was around 5.74% when the Modulation Index was equal to 0.95, as shown in Figure 21. The FFT analysis is shown in Figure 22 with the seven level Diodes clamped in multilevel inverter. The $THD_V$ for the voltage obtained when the Modulation Index was equal to 0.8, was lower when the Modulation Index was equal to 0.95 and its value was 5.34%.

**Fig. 17:** Phase Voltage of MI=0.95.



Fig. 18: Phase Voltage of MI=0.8.



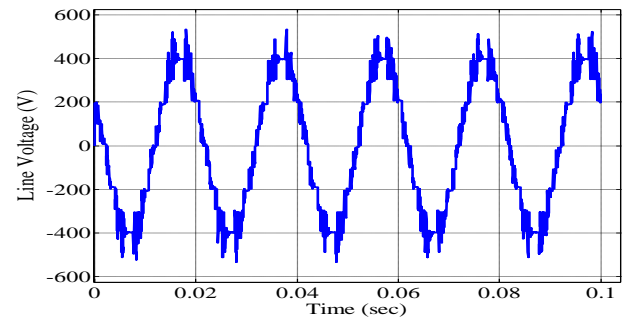**Fig. 19:** Line Voltage of MI=0.95.


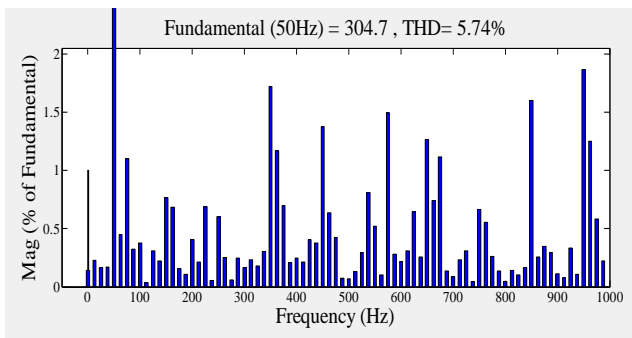
**Fig. 20:** Line Voltage of MI=0.8.
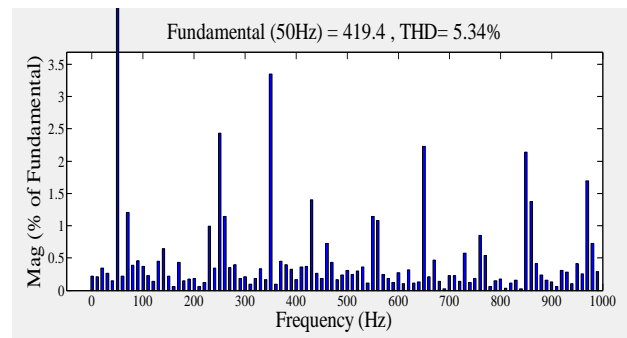


**Fig. 21:** Harmonic Voltage of MI=0.95.



**Fig. 22:** Harmonic Voltage of MI=0.8.

Next, the simulation result is shown in Figure 23. for the Nine-level diodes clamped in multilevel inverter. The output voltage wave form for line to neutral when the Modulation Index was 0.95, was 315.5 V RMS. When the Modulation Index decreased to 0.8, as shown in Figure 24 the inverter output voltage was equal to 285.4 V. The number of steps for both figures were 9 (*n*=9) for the quarter wave and in full wave, the number of steps was 18 (2*n*=18,*n*=9). As for the Nine-level diodes clamped in multilevel inverter, the simulation result is shown in Figure 25 The output voltage wave form for line to line in the number of steps for this level increased to 18 for the quarter wave and 36 steps for the full wave with Modulation Index equal to 0.95. The output voltage produced was about 542.7 V RMS. When the Modulation Index decreased to 0.8, the output voltage value was equal to 492.9 V RMS. The number of steps used was similar as in Figure 26.

The THD$_V$ for the voltage of the output diodes clamped in multilevel inverter was measured when the Modulation Index was equal to 0.95. It was found that the value of the THD$_V$ of the voltage was around 3.9%, as shown in Figure 27. The FFT analysis is shown in Figure 28 for Diodes clamped in multilevel inverter. The THD$_V$ for the voltage was obtained when the Modulation Index was equal to 0.8, which was lower, when the Modulation Index was equal to 0.95 with value of 3.07%.
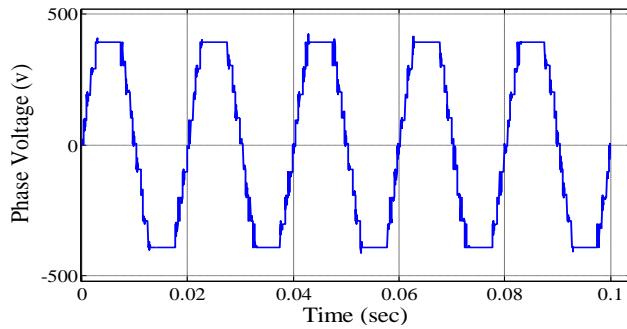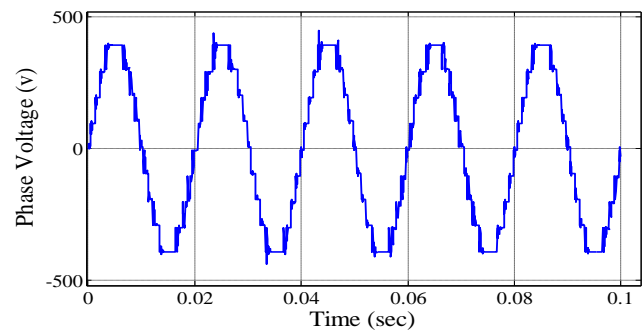
**Fig. 23:** Phase Voltage of MI=0.95.


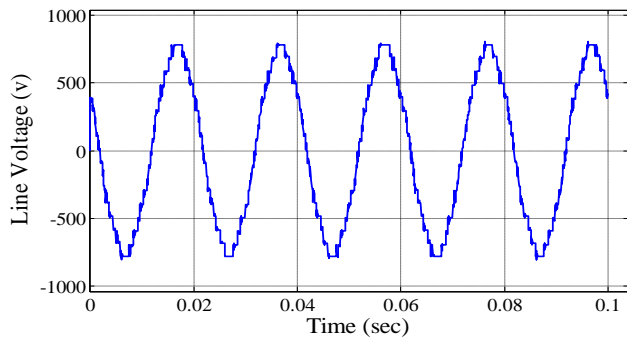
**Fig. 24:** Phase Voltage of MI=0.8.



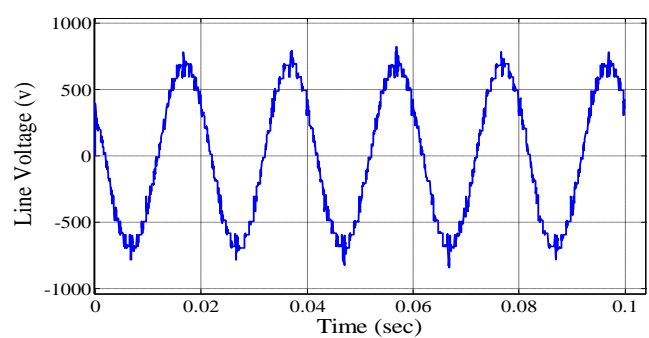**Fig. 25:** Line Voltage of MI=0.95.



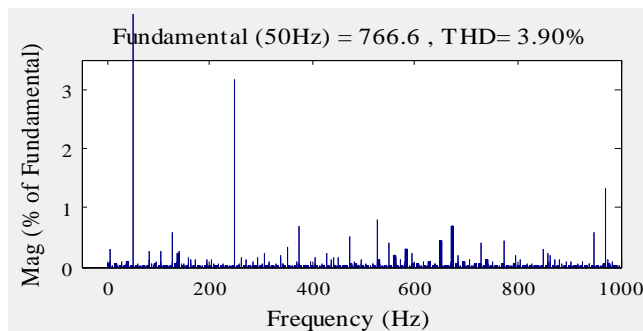**Fig. 26:** Line Voltage of MI=0.8.



**Fig. 27:** Harmonic Voltage of MI=0.95.



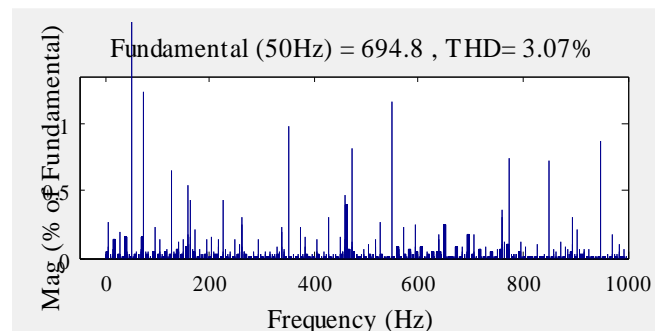**Fig. 28:** Harmonic Voltage of MI=0.8.

***B. Cascaded H-Bridge Multilevel Inverter Results:***

The simulation result is shows in Figure 29 for Five-level Cascaded H-Bridge in multilevel inverter. The output voltage wave form for line to neutral was about 159.6 V RMS with the Modulation Index equalled to 0.95. When the MI decreased to 0.8, as shown in Figure 30, the inverter output voltage was equal to 144.3V RMS. The number of steps taken for both figures were 5 (*n*=5) for the quarter wave, and as for the full wave, the number of steps was 10 (2*n*=10, *n*=5). Next, the simulation results are shown in Figure 31. for Five-level Cascaded H-Bridge in multilevel inverter. The output voltage wave form for line to line in the number of steps increased to 10 for the quarter wave and 20 steps for the full wave, with the Modulation Index equalled to 0.95. The output voltage produced was about 271.9 V RMS. When the Modulation Index decreased to 0.8, the output of voltage was 246 V RMS. The number of steps at this level was similar as in Figure 32.

The $THD_V$ for voltage at the five level output Cascaded H-Bridge in multilevel inverter was measured when the Modulation Index was equal to 0.95. It was found that the value of $THD_V$ of the voltage was around 6.07%, as shown in Figure 33. The FFT analysis is shown in Figure 34 for the five levels Cascaded H-Bridge in multilevel inverter. The $THD_V$ for the voltage obtained when the Modulation Index was equal to 0.8, was lower when the Modulation Index was equal to 0.95 and its value was 6.51%.
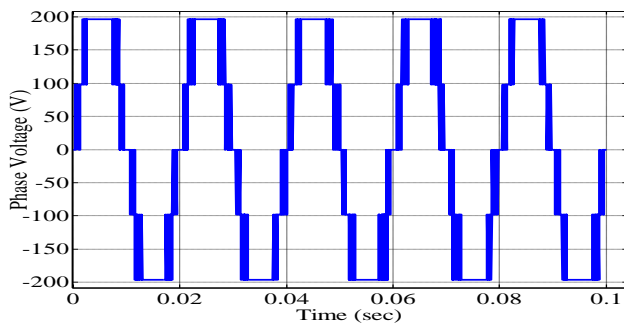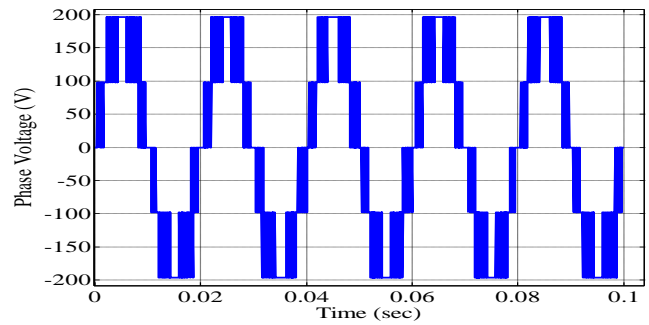
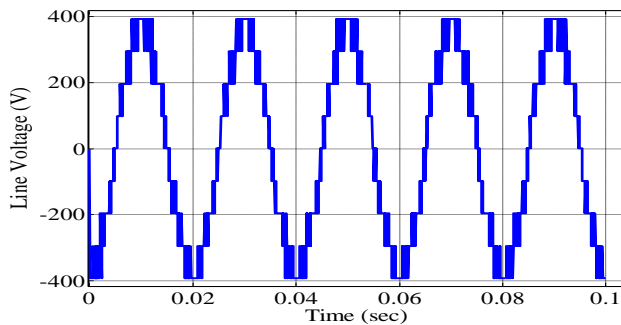**Fig. 29:** Phase Voltage at MI=0.95



**Fig. 30:** Phase Voltage at MI=0.8.



**Fig. 31:** Line Voltage at MI=0.95.
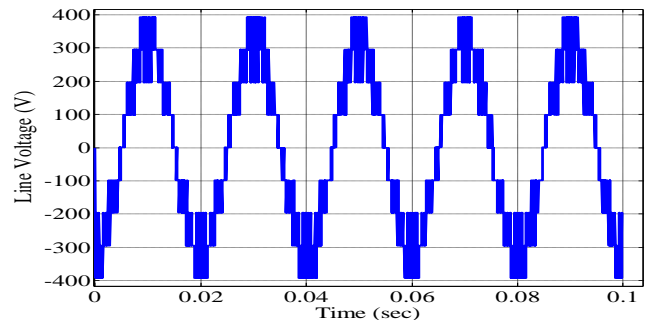


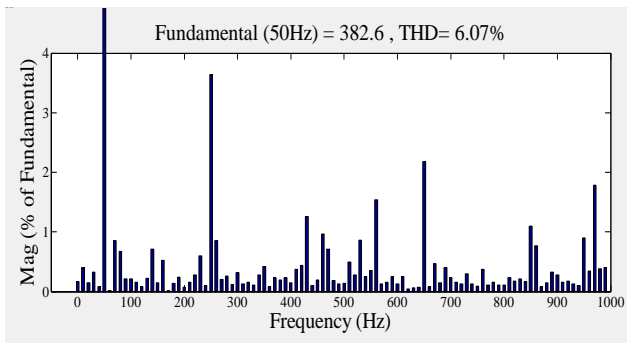**Fig. 32:** Line Voltage at MI=0.8.
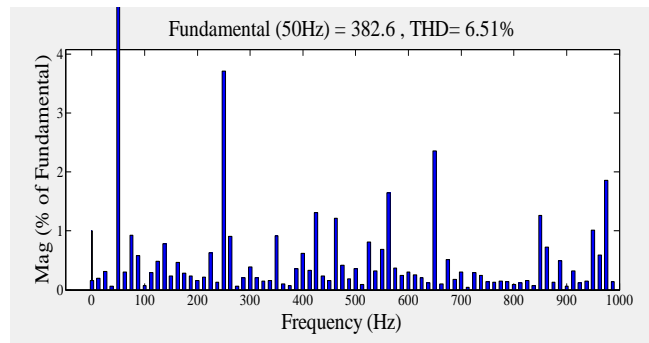


**Fig. 33:** Harmonic Voltage at MI=0.95.



**Fig. 34:** Harmonic Voltage at MI=0.8.

   The simulation result is shows in Figure 35 Seven-level Cascaded H-Bridge in multilevel inverter. The output voltage wave form for line to neutral was about 194.5 V RMS with the Modulation Index was equal to 0.95. When the MI decreased to 0.8, as shown in Figure 36, the inverter output voltage was equal to 152.7 V RMS. The number of steps for both figures was 7 ($n$=7) for the quarter wave and for the case of full wave, the number of steps was 14 ($2n$=14, $n$=7). Next, the simulation results are shown in Figure 37. for Seven-level Cascaded H-Bridge in multilevel inverter. The output voltage wave form for line to line in the number of steps increased to 14 for the quarter wave and 28 steps for the full wave with the Modulation Index equalled to 0.95. The output voltage produced was about 333.8 V RMS. When the Modulation Index decreased to 0.8, the output voltage equalled to 260.9 V RMS. The number of steps used was similar as in Figure 38.

   The $THD_V$ for voltage on the seven level output Cascaded H-Bridge multilevel inverter was measured when the Modulation Index was equal to 0.95. It was found that the value of the $THD_V$ of the voltage was around 5.98%, as shown in Figure 39.The FFT analysis is shows in Figure 40 for the seven levels Cascaded H-Bridge in multilevel inverter output. The $THD_V$ for the voltage was obtained when the Modulation Index was 0.8 and the value was equal to 6.01%.
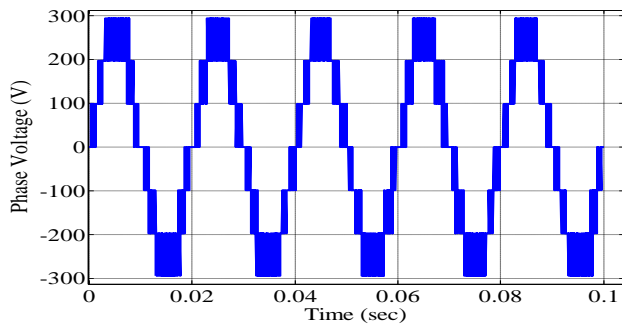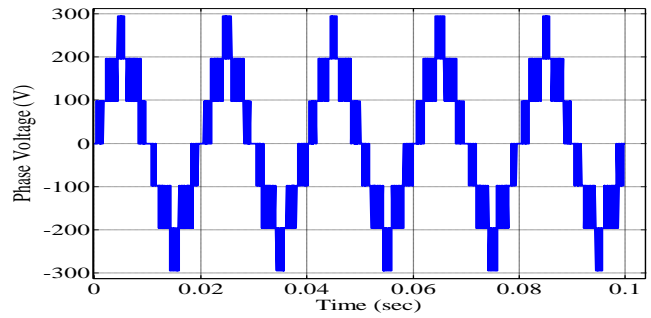
**Fig. 35:** Phase Voltage at MI=0.95
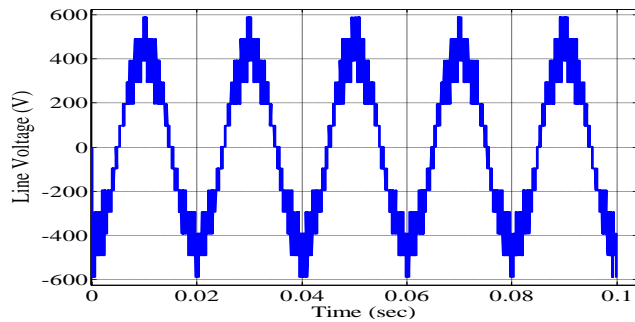


**Fig. 36:** Phase Voltage at MI=0.8.



**Fig. 37:** Line Voltage at MI=0.95.
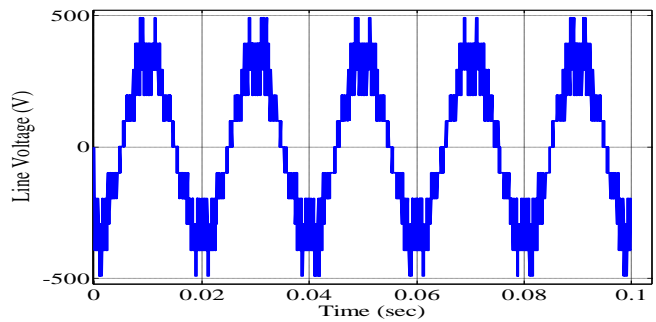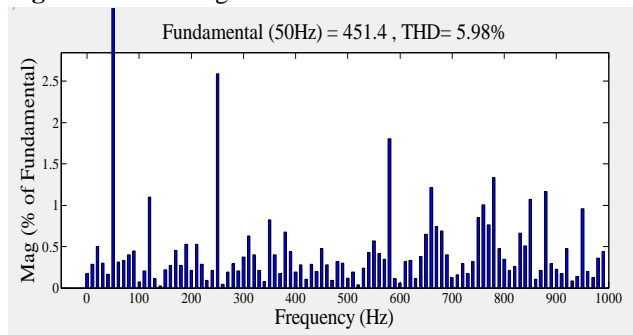


**Fig. 38:** Line Voltage at MI=0.8.



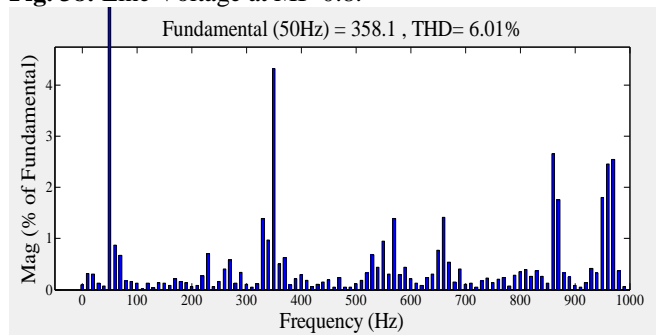**Fig. 39:** Harmonic Voltage at MI=0.95.



**Fig. 40:** Harmonic Voltage at MI=0.8.

Next, the simulation result is shown in Figure 41 for the Nine-level Cascaded H-Bridge in multilevel inverter. The output voltage wave form for line to neutral with the Modulation Index 0.95 was 262.2 V RMS. When the MI decreased to 0.8, as shown in Figure 42, the inverter output voltage was 202.8V RMS. The number of steps for both figures was 9 ($n$=9) for the quarter wave and in the full wave, the number of steps was 18 ($2n$=18, $n$=9). The simulation results are shown in Figure 43. for Nine-level Cascaded H-Bridge in multilevel inverter. The output voltage wave form for line to line in the number of steps increased to 18 for the quarter wave and 36 steps for the full wave, with the Modulation Index equalled to 0.95. The output voltage produced was about 452.8 V RMS. When the Modulation Index decreased to 0.8, the output voltage was 349.7 V RMS. The number of steps used was similar as in Figure 44.

The $THD_V$ for the voltage on the output of Cascaded H-Bridge in the multilevel inverter was measured when the Modulation Index was 0.95. It was found that the value of the $THD_V$ of voltage was around 2.92%, as shown in Figure 45. The FFT analysis is shows in Figure 46 for the Cascaded H-Bridge in multilevel inverter output. The $THD_V$ for the voltage was obtained when the Modulation Index was 0.8 and the value was equal to 3.58%.
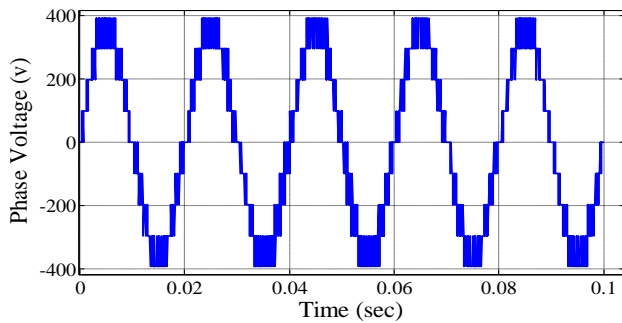
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**Australian Journal of Basic and Applied Sciences, 8(3) March 2014, Pages: 211-227**



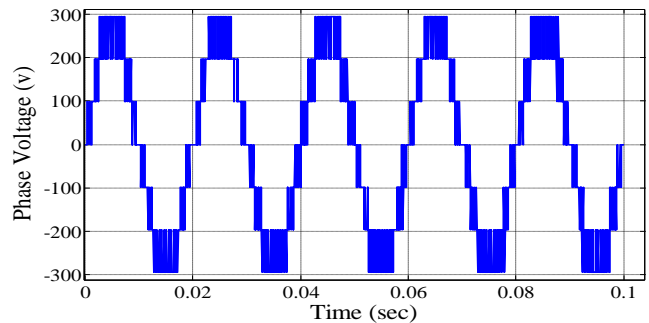**Fig. 41:** Phase Voltage at MI=0.95.



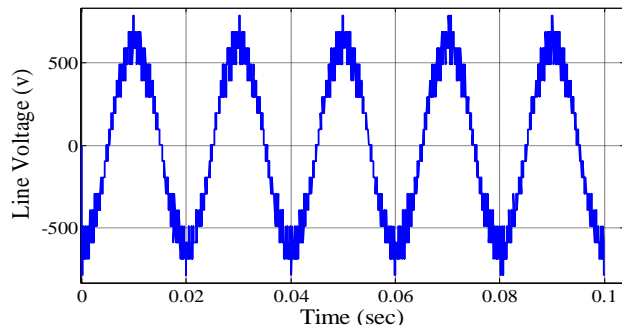**Fig. 42:** Phase Voltage at MI=0.8.



**Fig. 43:** Line Voltage at MI=0.95.
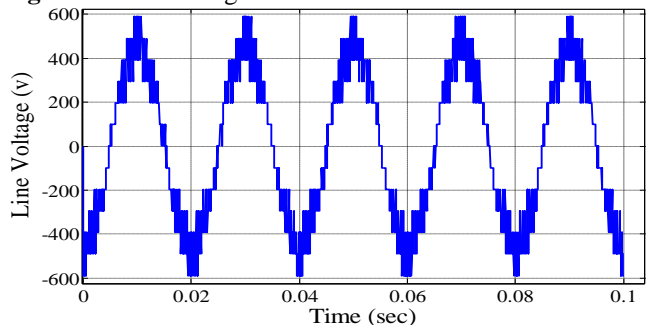


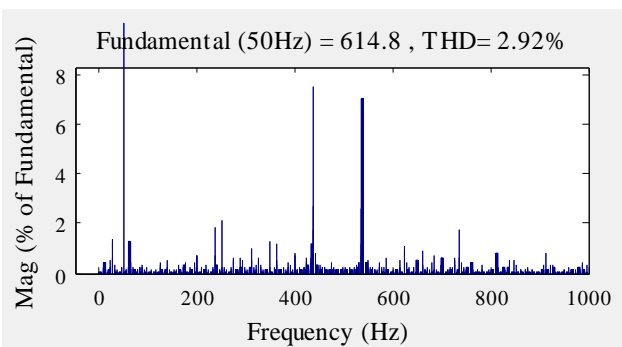**Fig. 44:** Line Voltage at MI=0.8.



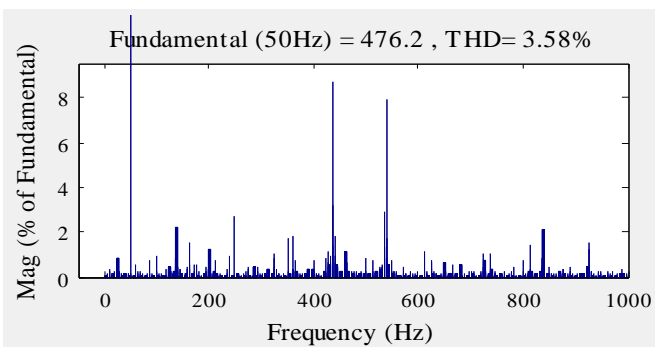**Fig. 45:** Harmonic Voltage at MI=0.95.



**Fig. 46:** Harmonic Voltage at MI=0.8.

**Table 3:** Comparison of Diodes Clamp and Cascaded H-Bridge Inverters with Different Modulation Index (MI=0.95, MI=0.8).

| Level(N) Index(M) | | Phase Voltage RMS | | Line Voltage RMS | | THD | |
|---|---|---|---|---|---|---|---|
| | | Diode | H-Bridge | Diode | H-Bridge | Diode | H-Bridge |
| Five | MI=0.95 | 167.6 | 159.6 | 285.5 | 271.9 | 7.21% | 6.07% |
| | MI=0.8 | 158.7 | 144.3 | 272.6 | 246 | 7.06% | 6.51% |
| Seven | MI=0.95 | 216.4 | 194.5 | 373.6 | 333.8 | 5.74% | 5.98% |
| | MI=0.8 | 174.1 | 152.7 | 3000.1 | 260.9 | 5.34% | 6.01% |
| Nine | MI=0.95 | 315.5 | 262.2 | 542.7 | 452.8 | 3.90%. | 2.92% |
| | MI=0.8 | 285.4 | 202.8 | 492.9 | 349.7 | 3.07%. | 3.58% |

*Conclusions:*

The comparative studies between the two types of multilevel inverters had been investigated. The diode voltage output line imposed (NPC) slightly higher results than the line output voltage of the cascaded H - bridge (CHB) in multilevel inverters, due to more losses in the diode clamp available. However, each THDV in the multilevel inverters were reduced and values follow the IEC standard. The choice was based on the topology of each inverter and depended on the use of the inverter. Each topology had its advantages and disadvantages. By increasing the number of levels, the THDv dropped, but the cost on the other hand, was high as well. On the other hand, the cascaded H-bridge in multilevel inverter topology required only a single DC power source. The multilevel inverter topology diode imposed unequal sharing effort between the capacitors connected in series leading to a condenser, DC linkage disequilibrium, which require a large number of clamping diodes at a higher level, so that the cost would not be higher than cascade H-bridge. It seemed that the duo imposed inverter topology among all other topologies that the THD lost, cost and energy among other types of inverters. Hence, multilevel inverters have become effective and practical solution for multi-level increased energy and to reduce

harmonic of AC wave forms. The main advantages of multilevel PWM converters are that the series of connection allow high voltage without increasing the voltage on the effort of switches. Besides, the wave forms in the multilevel reduced the dv/dt at the output of the inverter. As for the same switching frequency, the inverter may be at several levels of harmonic distortion due to lower levels of output wave form over the inverter with respect to a single cell. Other advantages of using these multilevel inverters are: 1) reduce switching losses, 2) high voltage capability, 3) provide power at the highest quality, 4) useful to drive applications, 5) contribute to very high yields (> 98%) due to the minimum switching frequency, 6) can improve power quality and dynamic stability of utility systems and, 7) they are suitable for medium to high power applications. Thus, multilevel inverters can be utilised in various fields with numerous benefits.

## ACKNOWLEDGEMENTS

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