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Binary-Aware Symmetric (BAS) High Performance SOI SRAM Cell Design

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ABSTRACT

Background: Static random access memory (SRAM) represent a major portion of chip, and it is expected to increase in portable devices and high performance processors in the future. To achieve high performance and low power consumption, the feature size of CMOS devices has been dramatically scaled to smaller dimensions. Therefore, nowadays, Silicon On Insulator (SOI) technology is broadly used in IC designs. To establish larger reliability and longer battery life for portable application, low power SRAM array is necessity. **Objective:** To propose new partially depleted SOI Binary-Aware Symmetric SRAM architecture to reduce the power consumption because write power consumption in any SRAM cell is a significant portion of the overall power consumption due to large voltage swing in the large bit lines. **Results:** The simulated result shows that the write power of the proposed cell is reduced approximately 36% at 0.9V and 47.62% at 1.2V compared to the 6T cell due to lower discharging activity at bit lines. Both static noise margin and read access delay are maintained same as the 6T cell after carefully sizing of all the transistors. **Conclusion:** In the proposed cell, the write circuit does not discharge for any write operation and hence the write activity factor of the discharging BL is less than "1" which makes the proposed cell more power efficient during write operations compared with the conventional cell.

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INTRODUCTION

SRAM represents a large portion of the chip and it is expected to increase in future in both portable devices and high-performance processors. To achieve high performance and low power consumption, the feature size of CMOS devices has been dramatically scaled to smaller dimensions. Therefore, nowadays, Silicon On Insulator (SOI) technology is broadly used in IC designs. Its performance is merited with low power dissipation, low noise, high rejection to radiation, and no latch-up effect in contrast with conventional CMOS cell (Jacob, J.B *et al*., 1998, Francis, P *et al*., 1992, and Bruel, M, 1995). Thus, SRAM cell's performance can be enhanced based on SOI technology. Some SRAM circuits are proposed based on circuit level modification, but their stabilities are always poor whereas others are based on devices modifications with complicated processes involved (Lage, M *et al*., 1996, Noda, K *et al*., 2001, Thomas, O *et al*., 2003, Thomas, O *et al*., 2005, and Semenov, O *et al*., 2002). Over the years, power reduction requirement in SRAM has undergone tremendous advancement (Kim, C.H *et al*., 2005, Peter Geens *et al*., 2005, Yamaoka, M *et al*., 2006, Inaba, S *et al*., 2006, and Amrutur, B *et al*., 1994). Cache accesses include read and write operations. Because cache read occurs more frequently than the write, especially for the instruction cache, most low-power techniques focus on reducing the cache read power. However, the write power usually larger than the read power due to large power dissipation in driving the long bit lines to full swing. The power dissipated in bitlines represents 70% of the total SRAM power consumption during write operation. Many techniques have been proposed to reduce the write power consumption particularly by reducing the voltage swing level on the bit lines (Prabhu, C.M.R *et al*., 2009, Chang, Y.J *et al*., 2004, Ramy E. Aly *et al*., 2007, and Zhiyu Liu *et al*., 2008).

In this paper, we have proposed a new partially depleted SOI BAS SRAM to reduce power dissipation and increase performance during write operation. The pull down path of the respective inverter, in the proposed BAS SOI SRAM cell, contains an extra tail transistor whose switching behavior is controlled by the logic level at the respective bit line. During write operation, the pull down path of one of the inverter is disconnected from ground through OFF tail transistor. This facilitates the writing of the cell from "0" to "1" and vice-versa. The proposed cell is simulated in terms of write/read power consumption, write/read access delay and read stability

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in 0.12µm SOI CMOS technology at room temperature using SPICE simulation and advance BSIM 4 model (MICROWIND CAD tool). The rest of the paper is organized as follows. The proposed BAS SOI SRAM cell is explained in section II. The simulated results of write power consumption, write/read performance, Static Noise Margin (SNM) are presented in section III. The layout of the BAS SOI SRAM cell is shown in section IV and section V concludes the paper.

Proposed Circuit Description:

The use of Silicon-On-Insulator (SOI) technology is bringing new possibilities compared to conventional bulk technology. Performance improvement concerns the power consumption and speed. The SOI technology may cut the power consumption nearly by half, with speed improvements close to 30% (Etienne Sicard *et al*., 2007). SOI refers placing a thin layer of silicon on top of silicon oxide insulator as shown in Fig. 1. The transistors are built on top of this thin layer. The basic idea is that the SOI layer will reduce the parasitic junction capacitance of the transistor to increase the switching time of transistor. The parasitic capacitances, namely junction capacitances Csb and Cdb, are strongly reduced using the thicker silicon dioxide. The source/bulk junctions of the SOI device can be significantly forward-biased due to the impact ionization. In MICROWIND (Etienne Sicard *et al*., 2007), the kink effect is modelized in the case of partially-depleted SOI devices, thanks to a new parameter ASOI. In SOI 0.12µm technology, the dielectric thickness is 300nm, and silicon thickness on the top of the insulator is 150nm. The complete schematic for the proposed BAS SOI cell is shown in Fig. 2.

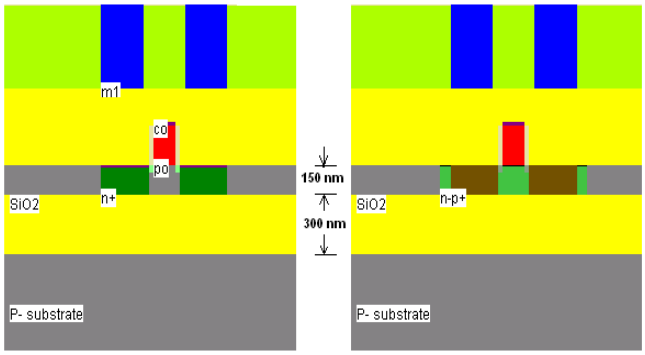


Fig. 1: Cross section of the nMOS and pMOS devices.

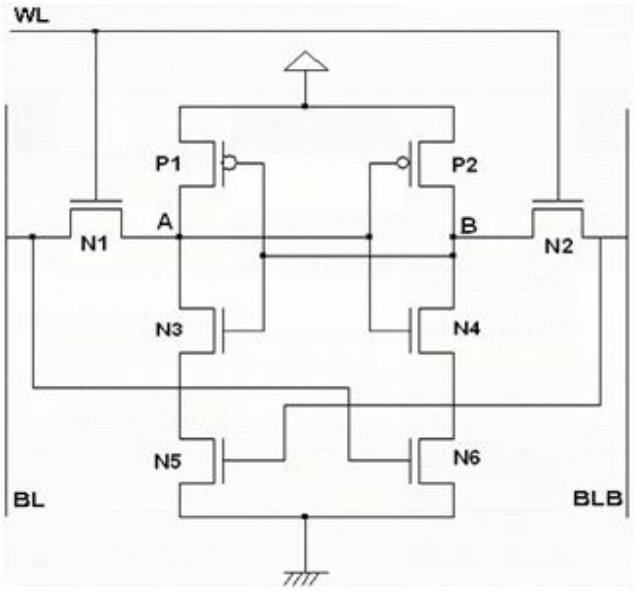
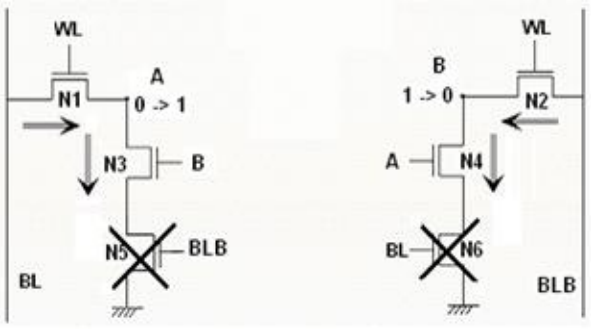


Fig. 2: A Binary-aware symmetric SRAM SOI cell.

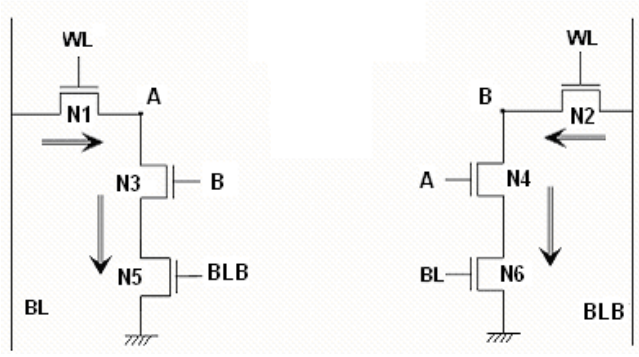
The write operation of the proposed BAS SOI SRAM cell depends on cutting off the pull-down path of one of the inverters using tail transistors N5 and N6. Due to absence of any extra signal to control switching behaviour of the tail transistors (Chang, Y.J *et al*., 2004), there is no extra hardware burden. The detailed operation of the BAS SOI SRAM cell is described as: In write "1" mode, node "A" must be written to high that

can be performed by setting BL to "1" (BLB is complement of BL) and then asserting WL to "high". This causes transistor N5 to turn OFF and disconnects the pull-down path of the inv.1 as shown in Fig.3 (a). This flips the node "A" to "high" without being waiting for the node B to discharge. Write "0" mode can be performed by setting BLB to "high" and asserting WL to "high" which causes N6 to turn OFF and disconnects the pull down path of the inv.2 from ground as shown in Fig. 3 (b). This flips the node B to "high" without being waiting for the node A to discharge. The write access time in the proposed BAS cell is smaller compared to the conventional 6T cell due to no discharging activity of the respective bit line. The read critical path contains three series connected transistors as shown in Fig. 4. The three series connected transistors degrade the driving capability of the cell unless these transistors are carefully sized.



(a) **(b)**

Fig. 3: Write path (a) cell state from "0"->"1" and (b) cell state from "1"->"0".



(a) **(b)**

Fig. 4: Critical read path when (a) A = "0" and (b) A = "1".

Simulation Results and Discussions:

This section provides the detailed analysis of the proposed BAS SOI SRAM cell in terms of write/read power consumption, delay and stability. We have simulated the proposed BAS SOI SRAM circuit and Conventional SOI SRAM circuit using SPICE and advanced BSIM4 (SOI MOSFET) model. The SPICE waveform during write operation of the proposed cell is shown in Fig. 5. Fig. 7 shows the power dissipation of BAS SOI SRAM cell and the 6T SOI SRAM cell. The proposed BAS PD SOI SRAM cell consumes at least 47.62% lower power at 1.2V supply voltage and 36% at 0.9V supply voltage compared to the conventional 6-T SOI SRAM cell. The lower power consumption during write operation is due to lower discharging activity at bit lines. Write delay is determined by using the definition as mentioned in reference (Chang, Y.J *et al*., 2004). The write access time of BAS SOI SRAM cell under different VDD in 0.12µm technology is given in Table I. In the proposed SOI SRAM cell, the access delay during the write transition is improved approximately 83.61% as compared to the conventional 6T cell due to no discharging activity of the respective bit line.

The read SPICE waveform of the proposed BAS cell is shown in Fig. 6. Read delay is defined as the elapsed time from asserting WL to the sufficient bit line swing for correct data sensing (Chang, Y.J *et al*., 2004). Because of the symmetric inverter pair in BAS SOI SRAM cell, read "1" and read "0" delay are same. The introduction of two tail transistors N5 and N6 degrades the read access delay. Fig.8 shows the variation of read delay of BAS cell and 6T cell with (W/L) ratio of the tail transistors. From Fig. 8, it is observed that selecting $\beta_{N5} = \beta_{N6} \leq 2$ is not sufficient to maintain the read delay of purposed cell same as the conventional cell whereas $\beta_{N5} = \beta_{N6} \leq 2.2$ strongly improves the driving capability of the proposed cell. Here β defines the W/L ratio of the respective transistor.

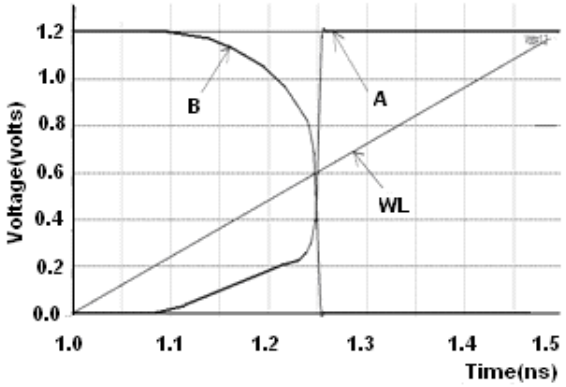


Fig. 5: SPICE waveform during write.

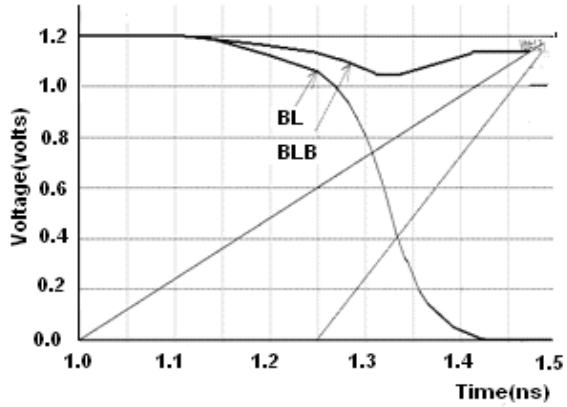


Fig. 6: SPICE waveform during read.

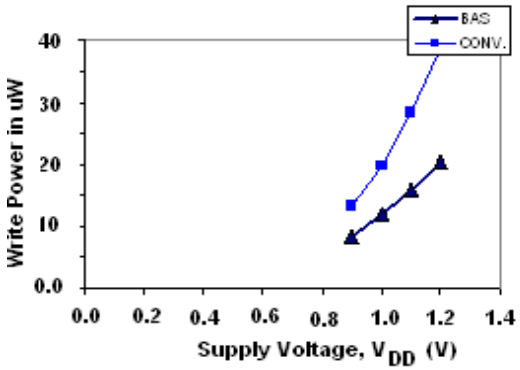


Fig. 7: Power dissipation.

The cell stability can be measured as the static noise margin (SNM). The SNM is defined as the maximum dc noise voltage required to flip the cell stored data (Ramy E. Aly *et al*., 2007). SPICE simulation shows that the SNM of a conventional 6T SOI SRAM cell is 120mV at VDD =0.9V. The butterfly curve of BAS PD cell has symmetrical lobes which depend on the tail transistor size (see Fig 9). The SNM of the proposed cell is simulated before and after choosing (W/L) ratio of the respective tail transistors. At 0.9V, before making any enlargement in the width of the tail transistors, the SNM of the proposed cell is degraded as seen in Fig. 9(a). From simulated results it is found that the read SNM for BAS SOI SRAM cell is 225mV for ($\beta_{N5} = \beta_{N6} \leq 2.5$, $\beta_{N3} = 3$, $\beta_{N1} = 1$) which is 1.875x better than the conventional cell. The main drawback of the proposed cell is a significant timing requirement in between the read and the write operations due to bit lines coupled transistors N5 and N6. If read operation perform slowly, the cell may lose data before read operation for unselected cells (when WL= high) when we are performing write operation on the selected cell. This can be rectified by selecting very short write pulse. The short write pulse also removes the problem in the operation of the cells which are not selected by WL but holding data.

Table I: Write delay with different supply voltage.

V_{DD} in volts	Write Delay in ps	
	BAS SOI	6T SOI
0.9	41	82
1	26.5	73
1.1	14	67
1.2	10	61

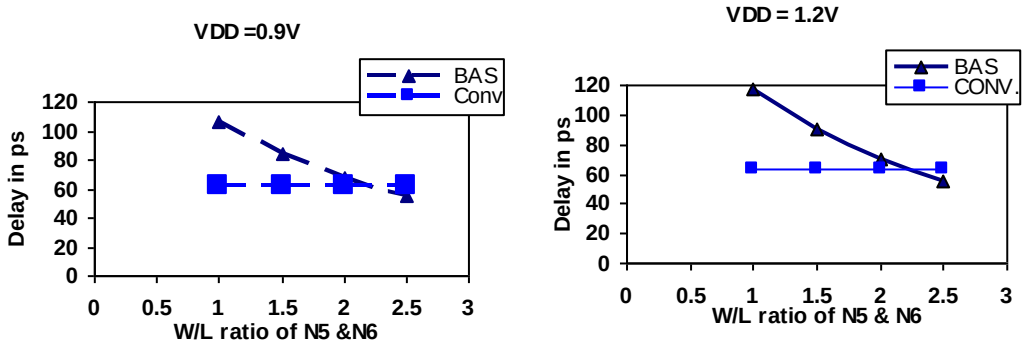


Fig. 8: Read delay varies with different W/L ratio for different V_{DD}

A total two metal layers are employed to design the BAS SOI SRAM cell. Fig. 10 shows the physical layout of the proposed BAS SOI SRAM cell. One of the important features of the SOI technology is that the CMOS cell-density increase due to relaxed design rule constraints between N+ and P+ diffusions. In CMOS bulk technology, the n-channel device is separated from the p-channel device by at least 12 lambda. In SOI CMOS technology, the design rule drops to only two lambda. Therefore, the proposed BAS SOI SRAM cell size is 2.64µm x 2.76µm and the conventional cell size is 2.22µm x 2.76µm size. It is important to note that the height of both cells is purposely maintained same. Compared to the conventional 6T SOI cell, the BAS SOI cell area is increased from 6.13µm2 to 7.29 µm2 in 0.12 µm technology. Most area overhead is introduced by the tail transistors N5 and N6 that enforces about 18.92% cell area overhead. Because, the percentage of the cell array to cache area is about 70%, the overall cache overhead is round 18.92%x70%=13.244% due to two extra tail transistors.

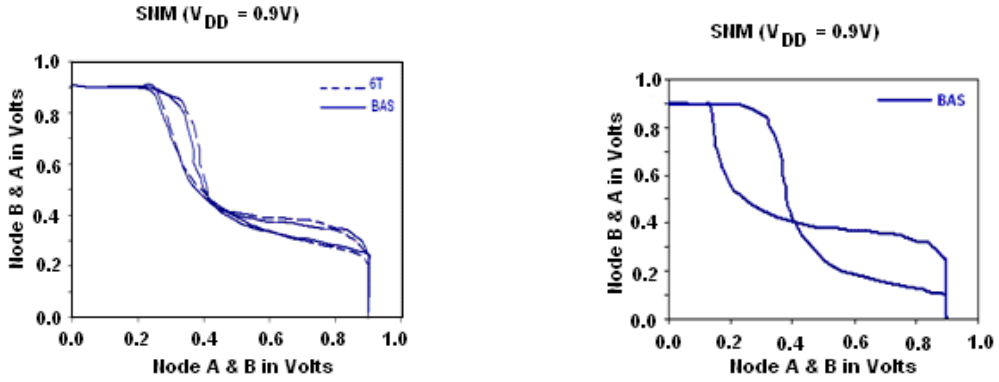


Fig. 9: (a) SNM (no change in W/L ratio) (b) SNM with ($\beta_{N5} = \beta_{N6} \leq 2.5$, $\beta_{N3} = 3$, $\beta_{N1} = 1$).

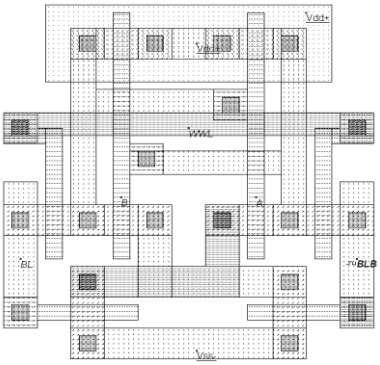


Fig. 10: BAS SOI SRAM Cell Layout.

Conclusions:

The proposed BAS SOI SRAM cell consumes approximately 50% less write power than the conventional 6-T SOI SRAM cell. The proposed cell also provides an improved read SNM after proper adjustment of tail transistor's width. This improvement is approximately two times of the conventional 6T SRAM cell. The write access delay is lower than the conventional one whereas read access delay degrades due to tail transistors which can be compensated by choosing proper (W/L) ratio of the tail transistors. The cell occupies approximately 18.92 % more area on the chip than the conventional 6T SOI SRAM cell.

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