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A Novel Method for Component Assessment of Current-Fed Impedance-Source Inverters

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Abstract: This paper presents an analytic method of designing the impedance network of a ZSCI. A set of nonlinear equations derived in steady-state analysis should be used to obtain values of the impedance network components. In order to obtain these components the mathematical equations should be solved simultaneously by means of numerical methods, which is not a simple task in designing of the impedance network. The proposed design method can also be used to achieve the critical values of the components below which static states appear during the operating cycle. Furthermore, this paper presents guidelines in approximate sizing of the impedance network components by means of linearization techniques. It is evident from the results of the design that the approximate values are very close to the accurate values. Therefore, when low ripple factors are selected, approximate values can be treated as the accurate values without much error. Computer simulation results verify the accuracy of the design method.

Key words: Z-source inverter, impedance network, steady state analysis

INTRODUCTION

Traditionally power inverters can be widely classified either as voltage source inverters (VSI) or current source inverters (CSI). The current source inverter is dual of a voltage source inverter as it has been proposed by Peng (2003). Because of the presence of the relatively large dc inductor fed by a voltage source, the input dc current can be limited and any output short circuit does not destroy the device. Recently applications of the CSI are increased since the semiconductor switches have been improved. Due to the inverter intrinsic output short-circuit protection, ruggedness, and direct current control ability, it has lots of applications. Some examples of the applications are uninterrupted power supplies, ac drives, and reactive power compensators (Wu, *et al*, 2008; Zmood and Holmes, 2001). However, CSI possesses several drawbacks as follows (Peng, *et al*, 20003):

- The ac output voltage is higher than the original dc voltage that feeds the dc inductor; therefore it is a boost inverter. For applications where a wide voltage range is desirable, an additional dc-dc buck converter is needed. This additional stage increases the system cost and lowers its efficiency.
- At least one of the upper switches and one of the lower ones have to be gated on. Otherwise, a dc inductor open circuit would occur and destroy the devices. The open-circuit problem is a major threat of the inverter in the term of reliability. Therefore, an overlap time for the safe current commutation is needed which also causes waveform distortion.
- Since this circuit is a boost inverter, it is very sensible to current swell and will lose its capability during this operation mode (Peng, 2004):

To overcome the limitations of the traditional current source inverter, the current-fed Z-source inverter (ZSCI) is proposed by Peng (2004) and it is shown in Fig. 1.

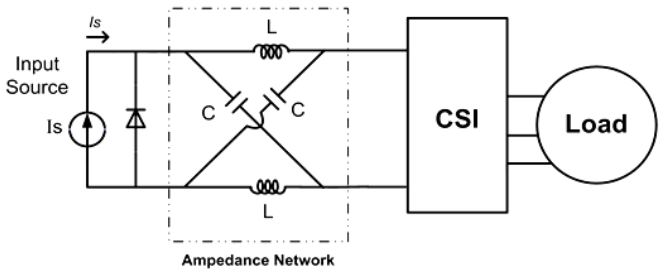

Fig. 1: A ZSCI with symmetrical impedance network.

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A symmetrical impedance network consists of two identical inductors and two identical capacitors connected in a specific manner to achieve the desired properties. This circuit has an additional zero vector. It is open-circuit switching state that is forbidden in the traditional I-source inverter. For the traditional I-source, both switches of any phase leg can never be gated off at the same time or an open circuit would occur and destroy the inverter. The new Z-source inverter advantageously utilizes the open circuit states to boost the DC bus current by gating off both upper and lower switches of a phase leg. Therefore, the Z-source inverter can buck and boost current to a desired output current that is greater than the available dc input current. In addition, the reliability of the inverter is greatly improved since the zero open circuit is not a threat for the devices. Thus it provides a low-cost, reliable, and high efficient single-stage structure for boosting current.

The most works have been published on the ZSCI are the switching devices control. The main idea on those works is maximizing the current-boost ratio while minimizing the device stresses (Loh, *et al*, 2007; Fang, 2008; Thangaprakhash and Krishnan, 2010; Shajith and kamaraj, 2011). However, there are a few publications on the designing of the ZSCI impedance network to provide guidelines in the sizing of its components. This paper provides guidelines to design the impedance network components accurately and a much simpler method also is presented in approximate sizing by means of linearization techniques.

Steady-State Analysis of the ZCSI:

Switching states of the semiconductor devices on its input and output terminals affect on the operating state of the impedance network. The diode D_s on its input side has two switching states as "On" and "Off," and the CSI on its output side has three switching states 1, 2, and 3 as shown in Fig. 2

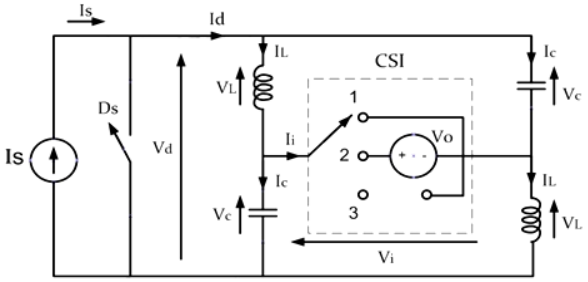

Fig. 2: Switching equivalent of the ZSCI

During the state 1, which is known as "short" state, input terminals of the CSI are effectively short-circuited by switching on the devices at the top and bottom of one or more of its three legs similarly. In state 2, known as "Active" state, CSI applies one of the six nonzero- switching vectors to the load while using a load-dependent voltage from its input source. The voltage used from the impedance network during this state can be represented by a constant voltage source V_o by neglecting its ripple content. A conventional CSI can only be operated in one of these two input state, but the ZSCI can be operated in a third input state, which is known as the ''Open circuit'' state too. Unlike the traditional CS inverters where an upper and lower power switch are always turned ON to conduct the dc link current i_s, ZSCI can assume an open circuit state by turning OFF all switches without breaking any inductive current. In general, at a given time the impedance network of the CSI can operate in any one of the six possible states given in Table I.

Table 1: Possible Operating Of The Impedance Network

CIS	Short Circuit		Active		Open	
Diode(Ds)	Off	On	Off	On	On	Off
Impedance Network	Short-1	Short-1	Active-1	Active-2	Open-1	Open-2

There are six operation states of the impedance network during a switching cycle of the CSI. But only Short-1, Active-1 and Open-1 are desired states in practical applications. The other three stats, Short-2, Active-2 and open-2 are undesirable and should be avoided by proper sizing of the inductors and capacitors of the impedance network.

The common equations that describe the impedance network can be written as follows:

$$V_l = L(dI_l/dt) \qquad I_c = C(dV_c/dt) \tag{1}$$

$$V_d = V_c + V_l \qquad I_d = I_c + I_l \tag{2}$$

$$V_i = V_c - V_l \qquad I_i = I_l - I_c \tag{3}$$

where V_l and I_l are the voltage across and current through any of the two inductors, V_c and I_c are the voltage and current of any of the capacitors, V_d and I_d are the voltage and current at the input terminals of the impedance network connected to the source paralleled with the diode, and V_i and I_i are the voltage and current at the input terminals of the CSI. As given in the following sections, the characteristics of each operating state can be described separately, by neglecting the presence of parasitic resistances of the source, inductors, and the capacitors.

A. Short-1 state:

The following equations define the Short-1 state:

$$I_d = I_s \qquad V_i = 0 \tag{4}$$

By substituting (4) in (1)–(3), the voltage across the capacitor and its current can be expressed as:

$$\frac{d^2 I_l}{dt^2} + \frac{I_l}{LC} = \frac{I_s}{LC} \tag{5}$$

$$I_l = I_s + X_{sh} \sin(\omega t + \Phi_{sh}) \tag{6}$$

$$\omega = {}^{1}/_{\sqrt{LC}} \tag{7}$$

$$X_{Sh} = \sqrt{(I_{lish} - I_s)^2 + [V_{cish}/L\omega]^2} \tag{8}$$

$$\Phi_{sh} = tan^{-1}((I_{lish} - I_s)\frac{\omega L}{V_{cish}}) \tag{9}$$

With the initial values of the capacitor voltage and the inductor current in Short-1 state denotes by V_{cish} and I_{lish} respectively. With positive values of V_{cish} and I_{lish} the range of the initial angle is $\Phi_{sh} < \pi/2$. As a result, the inductor current will increase in a sinusoidal manner with time. Furthermore, the capacitor and the inductor currents in this state are given by:

$$I_c = I_s - I_l \qquad I_i = 2I_l - I_s \tag{10}$$

At $\omega t + \Phi_{Sh} = \pi/2$, the inductor current achieves its peak value and the capacitor and source voltage drop to zero. If the CSI is operated in Short state beyond the limiting time of $t_{shmax} = (\pi/2 - \Phi_{sh})/\omega$, the diode Ds would turn on as the voltage V_d tries in the reverse direction. This signifies the end of Short-1 state and the beginning of Short-2 state.

B. Short-2 state:

In the Short-2 state, the diode remains in the On-state and the CSI is in the Short state. Therefore, the state-defining equations are given as:

$$V_d = 0 \qquad V_i = 0 \tag{11}$$

Since, the impedance network remains isolated from the source and the load, all system variables remains constant during this state. In order to avoid this state, the necessary condition can be seen as:

$$V_{cfsh} > 0 \tag{12}$$

Where V_{cfsh} is the final value of the capacitor voltage in the Short-1 state. Fig. 3 shows the approximate waveforms of I_l and V_c for Short-1 and Short-2 states.

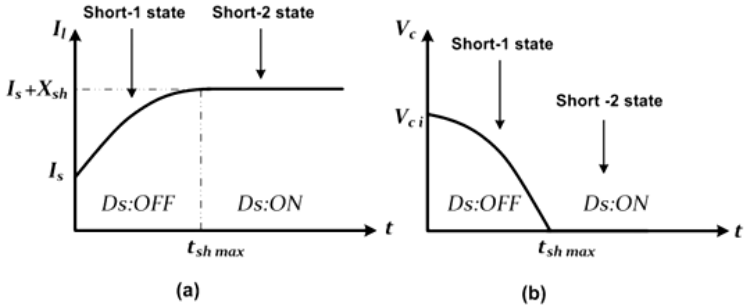

Fig. 3: Steady-state approximate waveforms of (a) inductor current and (b) capacitor voltage for the operation with short-1 and 2 states.

C. Active-1 state:

As it can be seen in the equivalent circuit given in Fig. 2, the only difference between Short-1 and Active-1 states is the presence of the constant voltage source V_o across the input terminals of the CSI.

The state-defining equations for Active-1 state are:

$$I_d = I_s \qquad V_i = V_o \tag{13}$$

Substituting (13) in (1)-(3), the inductor current and system voltages can be derived as:

$$I_l = I_s + X_A \sin(\omega t + \Phi_A) \tag{14}$$
$$V_l = V_c - V_o = (V_d - V_o)/2 = X_A \omega L \cos(\omega t + \Phi_A) \tag{15}$$
$$X_A = \sqrt{(I_{liA} - I_s)^2 + ((V_{ciA} - V_o)/\omega L)^2} \tag{16}$$
$$\Phi_A = tan^{-1}((I_{liA} - I_s)\omega L/(V_{ciA} - V_o)) \tag{17}$$

With initial values of the capacitor voltage and the inductor current in Active-1 state given by V_{ciA} and I_{liA} respectively. For the capacitor current and output current, their relationships with inductor current, given by (10), hold true even for the Active-1 state. Comparing (14) and (15) with those for the Short-1 state given in (5) and (6), it can be seen that Short-1 state is a special case of Active-1 state, While $V_o = 0$. As the load voltage V_o increases from zero, the peak value of the sinusoidal components of both capacitor voltage and inductor current will decrease and reach to a minimum when $V_o = V_{cA}$. Furthermore, the initial angle Φ_A will increase by increasing V_o and reach to a value of $\pi/2$ at $V_o = V_{ciA}$.

From (15), it can be seen that the voltage across the diode V_d will be zero and the diode will turn on when $V_c = -V_l = V_o/2$. It is interesting to note here that the inductor current charges to the peak value and then discharges before approaching the above operating point which marks the end of Active-1 state and the beginning of Active-2 state. If the duration of the Active-1 period is t_A, the final values of the two state variables can be written as:

$$I_{lfA} = I_s + X_A \sin(\omega t_A + \Phi_A) \tag{18}$$
$$V_{cfA} = V_o + X_A \omega C. \cos(\omega t_A + \Phi_A) \tag{19}$$

D. Active-2 state:

The state-defining equations for Active-2 state are:

$$V_i = V_0 \qquad V_d = 0 \tag{20}$$

Substituting (20) in (2) and (3), it can be seen that the voltage remains constant at $V_c = -V_l = V_o/2$ and the inductor discharges linearly with time at the rate of $V_o/2L$.

In order to avoid Active-2 state from appearing during operation, the necessary condition is:

$$V_{cfA} > V_o/2. \tag{21}$$

Fig. 4 shows the approximate waveforms of I_l and V_c for the Active-1 and Active-2 states.

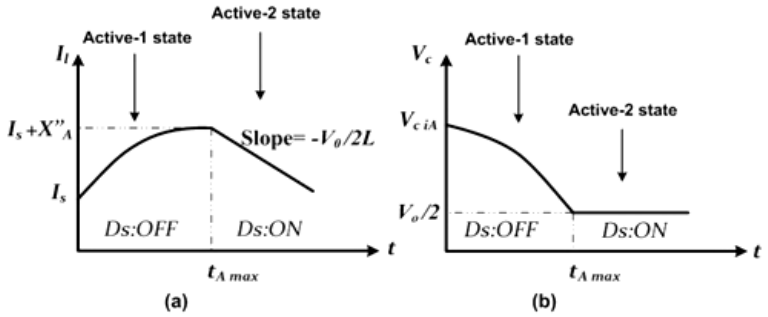

Fig. 4: Steady-state approximate waveforms of (a) inductor current and (b) capacitor voltage for the operation with Active-1 and 2 states

E. Open-1 state:

The state-defining equations for Open-1 state are:

$$V_d = 0 \qquad I_i = 0 \tag{22}$$

Substituting (22) in (1)-(3), the capacitor voltage and its current can be concluded as:

$$I_l = I_c = I_d/2 = X_o \sin(\omega t + \Phi_o) \tag{23}$$
$$V_l = -V_c = X_o \omega L \cos(\omega t + \Phi_o) \tag{24}$$
$$X_o = \sqrt{(I_{lio})^2 + (-V_{cio}/\omega L)^2} \tag{25}$$
$$\Phi_o = \tan^{-1}(-I_{lio}\omega L/V_{cio}) \tag{26}$$

With the initial values of the capacitor voltage and the inductor current in Open-1 state given by V_{cio} and I_{lio} respectively. Since $\pi/2 < \Phi_o < \pi$ inductor current by (23) is dropping from its initial value in a sinusoidal manner by increasing the time in this state. Simultaneously, the capacitor voltage given by (24) increasing toward its peak value in a sinusoidal manner by increasing the time. This indicates that the energy stored in the inductors during Short and Active states is transferred to capacitors during the Open state, thereby allowing the boosting of the current applied to the CSI. The Open-1 state ends and the Open-2 state begin when the diode D_s gets reverse biased and comes in to conduction. This occurs when the I_d drops to the level of I_s. Thus, from (23), it can be seen that $I_l = I_s/2$ at the end of Open-1 state. If the duration of the Open-1 state is t_o, then the final values of the two state variables can be written as following:

$$I_{lfo} = X_o \sin(\omega t_o + \Phi_o) \tag{27}$$
$$V_{cfo} = -X_o \omega L \cos(\omega t_o + \Phi_o) \tag{28}$$

F. Open-2 state:

The defining equations of Open-2 state are:

$$I_d = I_s \qquad I_i = 0 \tag{29}$$

Substituting (29) in (1)-(3), it can be seen that $I_c = I_l = I_s/2$ and $V_l = 0$ in this state. Moreover, the capacitor voltage ramps up linearly at a rate of $V_c = (I_s/2c)t$ with time. Hence, it is unsafe to let the converter operated for long periods in this state, as the increasing currents could damage the diode D_s and the switching devices of the CSI very soon. In order to prevent appearing of Open-2 state during the operation, the necessary condition is:

$$I_{lfo} > I_s/2 \tag{30}$$

Fig. 5 shows the approximate waveforms of the I_l and V_c for the Open-1 and Open-2 states.

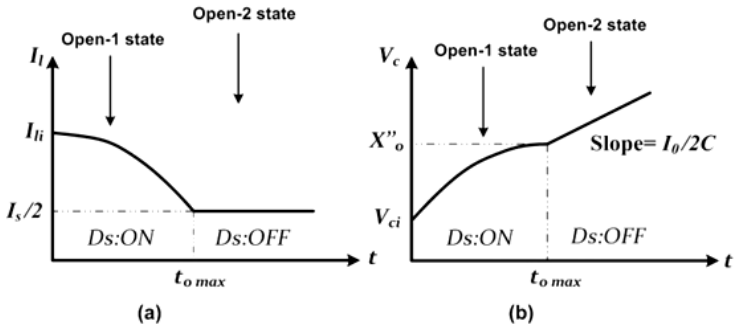

Fig. 5: Steady-state approximate waveforms of (a) inductor current and (b) capacitor voltage for the operation with open-1 and 2 states

G. Overview of operating state:

From the preceding discussion, it is clear that the Short-2, Active2 and Open-2 states do not contribute to the power conversion process and should be avoid. Thus, they are named as "*static state*" in this paper. Practical convertors are operated only in two or three of the Short-1, Active-1 and Open-1 states. They are hereby named as "*dynamic state*". Since the three static states appear only when the capacitor voltage and inductor current fluctuate in a wide range, leading to the violation of conditions given in (12), (21) and (30), it is necessary to limit the ripples of the related voltage and current by increasing the size of the inductors and capacitors appropriately. Therefore, after designing the circuit, a check can be made with these three conditions to ensure the limitation of operation only to the three dynamic states.

Designing of Impedance Network for Operation with Two Dynamic States:

As it is discussed in Section 2, Short-1 and Active-1 states behave in a similar manner. Therefore, Short-1 period can be considered as part of the Active-1 period without much error in the design. The three static states are also neglected as they are not useful to the power conversion process and should be avoided by appropriately sizing of the inductors and capacitors.

Hence, CSI is assumed to be operated only in Active-1 and Open-1 states as depicted in Fig. 6. Since the final value of a variable in one state is the initial value of the same variable in the other state, the boundary conditions can be defined as:

$$\mathrm{I_{liA}} = \mathrm{I_{lfo}} = \mathrm{I_{min}} \qquad \mathrm{I_{lio}} = \mathrm{I_{lfA}} = \mathrm{I_{max}} \tag{31}$$

$$\mathrm{V_{ciA}} = \mathrm{V_{cfo}} = \mathrm{V_{max}} \qquad \mathrm{V_{cio}} = \mathrm{V_{cfA}} = \mathrm{V_{min}} \tag{32}$$

Where $\mathrm{V_{min}}$ and $\mathrm{V_{max}}$ are the minimum and maximum values of the capacitor voltage and $\mathrm{I_{min}}$ and $\mathrm{I_{max}}$ are the minimum and maximum values of the inductor current, respectively. $\mathrm{T_s}$ is the period of switching cycle of CSI, which is assumed to be known.

$$t_A + t_O = T_s \tag{33}$$

Since the equivalent dc link current applied to the CSI is given by the average value of the I_i during the Active-1 state($\bar{I}_i$), it can be expressed using (10), (14) and (15) as:

$$\bar{I}_{iA} = \frac{1}{t_A}\int_0^{t_A} I_i.\,dt = I_s + 2\left(V_{ciA} - V_{cfA}\right)/(\omega^2 L t_A) \tag{34}$$

For a 3-phase CSI operated with sinusoidal PWM, the peak value of the fundamental line to neutral output current (I_m) is given by $M\bar{I}_{iA}/2$ where M is the modulation index. The relationship between M and the duty ratio of the Open-1 state $d_s = t_s/T_s$ is a result of the control strategy that is adopted to switch the CSI. In a simple boost control (Peng, 2004), d_s is kept constant at $(1 - M)$. For example, by adopting a simple-boost control strategy, equation (34) can be rewritten as:

$$2T_s I_m/t_A = I_s + 2\left(V_{ciA} - V_{cfA}\right)/(\omega^2 L t_A) \tag{35}$$

Where I_m and I_s are known for a given application.

By considering the lossless power transfer through the impedance network,

$$\frac{I_s}{t_A}\int_0^{t_A} E_s\,.dt = \frac{V_0}{t_A}\int_0^{t_A} I_i\,.dt \Longrightarrow \frac{I_s}{t_A}\int_0^{t_A}(V_0+2V_l)\,.dt = \quad V_0\bar{I}_{iA}$$
$$I_{lfA} - I_{liA} = V_0\left(V_{ciA} - V_{cfA}\right)/(\omega^2 L^2 I_s) \tag{36}$$

Where V_0 is also a known parameter in a given application. The voltage applied to the CSI achieves the peak value when the inductors are at their highest current. i.e. at the end of Active-1 state. Using (10), peak current applied to the CSI can be written as, $\bar{I}_i = 2I_{lfA} - I_s$. If this current is selected as β times the average current $\bar{I}_{iA}$ given by (34) and (35),

$$I_{lfA} = I_s/2 + \beta T_s I_m/t_A \tag{37}$$

In order to determine the required values of L, ω and t_s that would yield the required output ac current from the given input current and the CSI operating with a known switching frequency, it is necessary to solve (16)-(19), (26)-(29), (31)-(33), (34)-(37) simultaneously by using a numerical method. Finally, the required capacitance can be determined using (7).

Fig. 6 shows the Sinusoidal waveforms of the I_l and V_c for operation with two dynamic states.

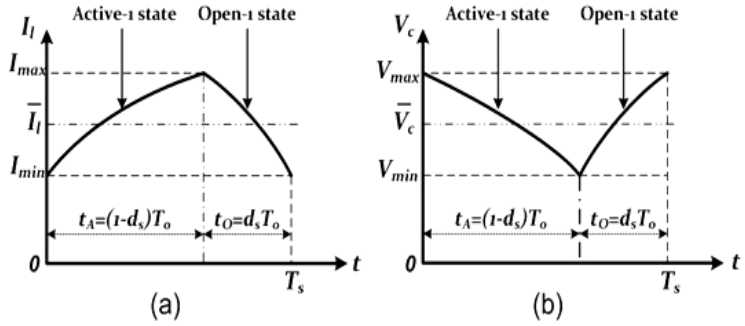

Fig. 6: Sinusoidal wave forms of (a) inductor current and (b) capacitor voltage.

By considering the previous discussion in this section, it can be observed that it is not a simple way to accurately design the component values of the impedance network of the ZSCI.

In following section the approximate method of design is presented by using linearized waveforms which is a simpler method to obtain the component of the impedance network.

Approximate Design with Linearized Waveform:

It is easy to observe that the difference between values obtained by solving 6 nonlinear equations and assumed linear wave form were too little and in practical applications are negligible. Due to the smaller ripple allowed by (21) and (30), the changes in the capacitor voltage and inductor current can be assumed as linear, instead of sinusoidal, for simpler analysis and designing of the ZSCI. Fig. 7 shows the linear waveforms of the capacitor voltage and inductor current for one switching cycle of the dc link. Fig. 5 shows the linearized waveforms of the I_l and V_c for the Active-1 and Open-1 states.

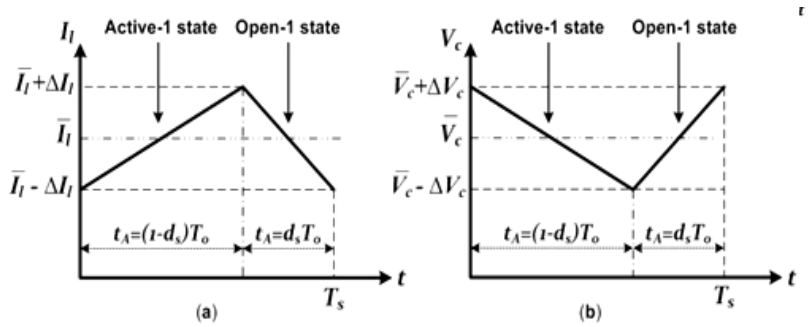

Fig. 7: Linearised waveforms of (a) inductor current and (b) capacitor voltage for small ripples.

By taking the peak ripples and average values of the capacitor voltage and inductor current as ΔV_c, $\overline{V}_c$, ΔI_l and $\overline{I}_l$ respectively, the maximum and minimum values of the two variables can be written as:

$$I_{min} = \overline{I}_l - \Delta I_l = (1 - k_i)\overline{I}_l \quad (38)$$
$$V_{min} = \overline{V}_c - \Delta V_c = (1 - k_v)\overline{V}_c \quad (39)$$
$$I_{max} = \overline{I}_l + \Delta I_l = (1 + k_i)\overline{I}_l \quad (40)$$
$$V_{max} = \overline{V}_c - \Delta V_c = (1 + k_v)\overline{V}_c \quad (41)$$

Where $k_i = \Delta I_l/\overline{I}_l$ and $k_v = \Delta V_c/\overline{V}_c$ are the ripple factors of the two waveforms, and are the two "design variables" for a design based on linear waveforms indeed. With linear variation of waveforms, from (1), ΔV_c and ΔI_l can be expressed as:

$$\Delta I_l = \overline{V}_l(\Delta t/L) \qquad \Delta V_c = \overline{I}_c(\Delta t/C) \quad (42)$$

Considering the Open-1 period

$$L = (\overline{V}_c d_s T_s)/(2\Delta I_l) \qquad C = (\overline{I}_l d_s T_s)/(2\Delta V_c) \quad (43)$$

Since, the average inductor voltage and the average capacitor current over a complete switching cycle in steady state are zero (Peng, 2003)

$$\overline{I_l}/I_s = \overline{V_c}/V_o = \lambda \quad (44)$$

Where, $\lambda = (1 - d_s)/(1 - 2d_s)$.

By expressing the ratio of peak ripples to their average values as k, where $k_i = k_v = k << 1$ for linear waveforms (43) and (44), can be combined as:

$$C = I_s d_s T_s/(2kV_o) \quad L = V_o d_s T_s/(2kI_s) \quad (45)$$

By neglecting the power losses in the inverter and the effects of harmonics on the ac side, the average power transferred from the dc link can be equated to the power delivered to the ac load over one ac cycle as (Shajith and kamaraj, 2011):

$$\overline{I}_{iA} V_o(1 - d_s) = 3/2\ (V_m I_m \cos\varphi) \quad (46)$$
$$V_0 = (3/4)V_m \cos\varphi \quad (47)$$

By substituting for V_0 in (45) from (47):

$$C = (2I_s d_s T_s(1 - d_s))/(3kMV_m \cos\Phi)$$
$$L = (3MV_m d_s T_s \cos\Phi)/\big(8kI_s(1 - d_s)\big) \quad (48)$$

Thus, if I_s, V_m, Φ, d_s and M are known, C and L, for any control strategy, can be calculated from (42) to result in the desired levels of the ripples.

Furthermore, by using (10) and (44):

$$\overline{I}_{iA} = (2\lambda - 1)I_s \implies \overline{I}_{iA} = I_s/(1 - 2d_s). \quad (49)$$

Now, C and L can be found for a typical control method.

***Simple-Boost Control*:**

$$M = 1 - d_s \quad (50)$$

By substituting $\overline{I}_{iA} = 2I_m/M$ in (42) and (43):

$$\lambda = 2I_m/I_s \implies d_s = (2I_m - I_s)/(4I_m - I_s) \quad (51)$$

With the values of λ and d_s it can be found that:

$$\bar{I}_l = 2I_m \qquad \bar{V}_c = 2I_m V_0 / I_s \tag{52}$$

$$C = 2I_s T_s (2I_m - I_s)/3kV_m \cos\varphi\,(4I_m - I_s)$$

$$L = 3V_m T_s \cos\varphi\,(2I_m - I_s)/8kI_s(4I_m - I_s) \tag{53}$$

Therefore, the sizing of the inductance and capacitance can be obtain by (53) for simple-boost control.

The current and voltage of the diode can be determined using (23) and (15) as:

$$I_{Ds} = 2(1+k)\bar{I}_l \qquad V_{Ds} = 2(1+k)(\bar{V}_c - V_o) \tag{54}$$

The current rating of CSI can be derived using (10) as:

$$I_{CSI} = 2(1+k)\bar{I}_l - I_s \tag{55}$$

Determining the Critical Voltages of the Capacitance and Inductance:

As given by (30), the Open state appears when the minimum inductor current I_{min} drop below one-half of the dc source current. The inductor L value that produces the critical condition,

$$I_{min} = I_s/2 \tag{56}$$

is defined as the "critical inductance". It can be determined by the design method described in Section 3 by using (56) to set the value of the design variable I_{min}.

In the same manner, the Active-2 state appears when the minimum capacitor voltage V_{min} drops below one-half of the load voltage V_o, as predicted in (21). The capacitance C that produces the critical condition,

$$V_{min} = V_o/2 \tag{57}$$

is therefore defined as the "critical capacitance". The value of critical inductance can be obtained by using (57) as the related design variable in the design method given in Section 3. When both (56) and (57) are used together, both variables are corresponding to their critical values. Further reduction in L or C will introduce a static state during the operation.

Design Example:

In the selected example, a three-phase $50\,Hz$, $60\,V$ (line) $6\,A$ Y-connected load whit a lagging power factor of 0.8 is supplied by a dc source of 5.5 A through a ZSCI operating at 5 kHz and controlled by simple-boost control. For this case, the circuit parameters required for the design procedure can be Calculated as I_s=5.5A, $T_s = 10^{-4}$ s, $V_m = \sqrt{2} \times 60/\sqrt{3} = 48.98$ V, $I_m = \sqrt{2} \times 6 = 8.485$A. From (44), it can be found that $\lambda = 3.085$, $d_s = 0.41$. Using (45), it can be determined that $\bar{V}_c = 90.62$V and $\bar{I}_l = 16.97$A then from (42), the equivalent dc link current can be found as, $\bar{I}_{iA} = 28.43$A. The input voltage of CSI can be found as, $V_o = (3/4)V_m \cos\varphi = 29.388$ V, the inductor and capacitor values are then given by (53) as $C = 3.77/k\,\mu F$ and $L = 0.107/k$ mH where factor k is chosen to limit the ripples of capacitor voltage and inductor current. In order to demonstrate a design whit low ripple in both capacitor voltage and inductor current a ripple factor of 5% is selected and$L = 2.14$ mH,$C = 76.4\,\mu F$. In this manner, the impedance network can be designed for any chosen value of k. The waveforms of I_l, V_c, I_i, V_i, I_{input}, I_{load}, as achieved from the computer simulation performed using PSIM software for the design with $k = 0.05$ are illustrated in Figures 8,9,10.

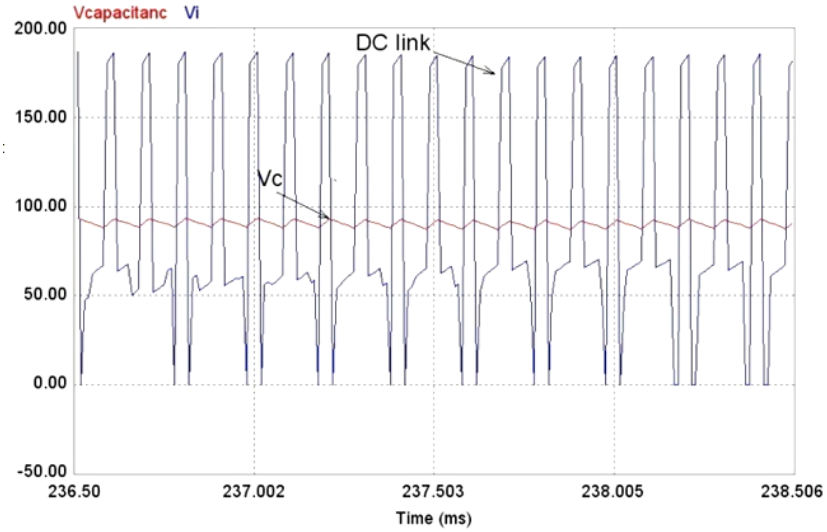

Fig. 8: Waveforms of Vc and Vi as resulted from the simulation for the design whit k=0.05

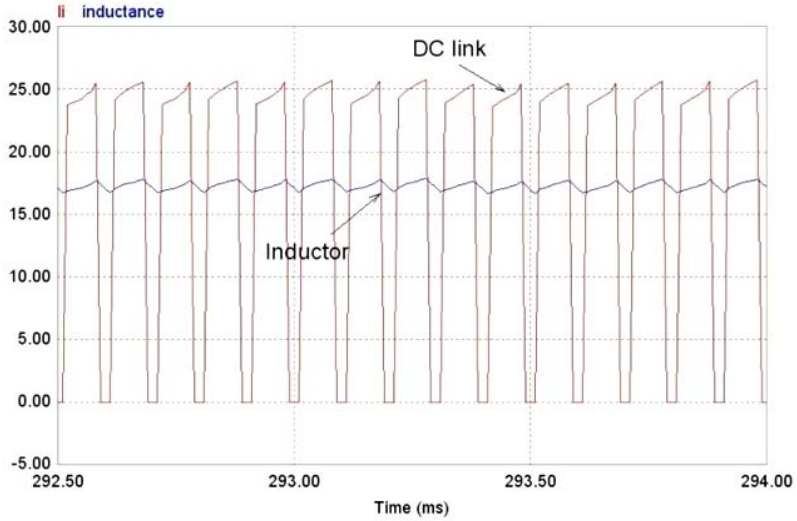

Fig. 9: Waveforms of IL and Ii as resulted from the simulation for the design whit k=0.05

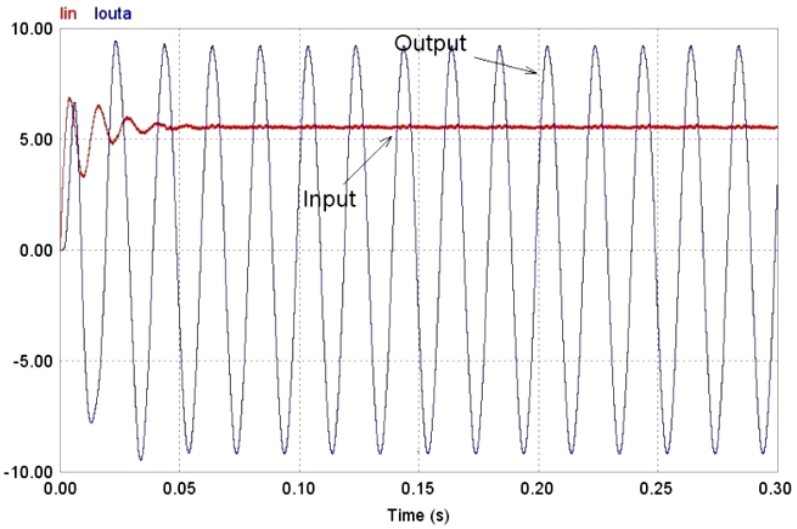

Fig. 10: Waveforms of input current and load current as resulted from the simulation for the design whit k=0.05

It can be seen that, inductor current shown in Fig. 8 has an average value about 17.2 A and a peak ripple of 5%. The capacitor voltage has an average value of 91.32 V and a peak ripple of 5%. The current and voltage rating of the diode from (54) are 35.637 A and 128.59 V respectively and the current rating of CSI from (55) is 30.137A. In this method, the impedance network can be designed for any chosen value of k.

The approximate and accurate values of the capacitor voltage and inductor current with simulation result for $k = 0.05$ are given in Table II.

Table I I: Results For The Design With 5% Ripple

$k = 0.05$	Numerical	Approximate	simulation
L	$2.2\ mH$	$2.14\ mH$	–
C	$75.8\ \mu F$	$76.4\ \mu F$	–
$\bar{I}_l$	$17.45\ A$	$16.97\ A$	$17.2\ A$
$\bar{V}_c$	$89.88\ V$	$90.62\ V$	$91.32\ V$

Simulation was repeated in order to demonstrate the possibility of appearance of static state for larger ripples in same case with$k = 1$, for which the only changes are $C = 3.77\ \mu F$ and $L = 0.107\ mH$ in Fig. 11 and Fig. 12.

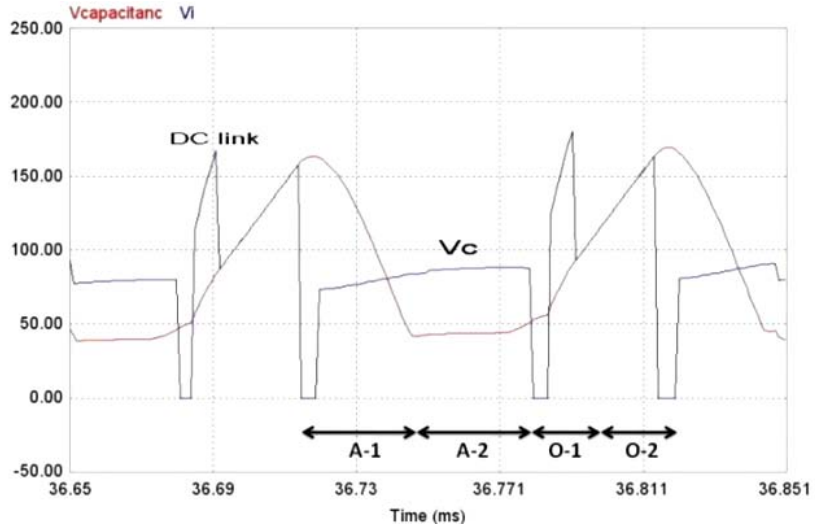

Fig. 11: Simulation results around the critical values of capacitance and dc link voltage.

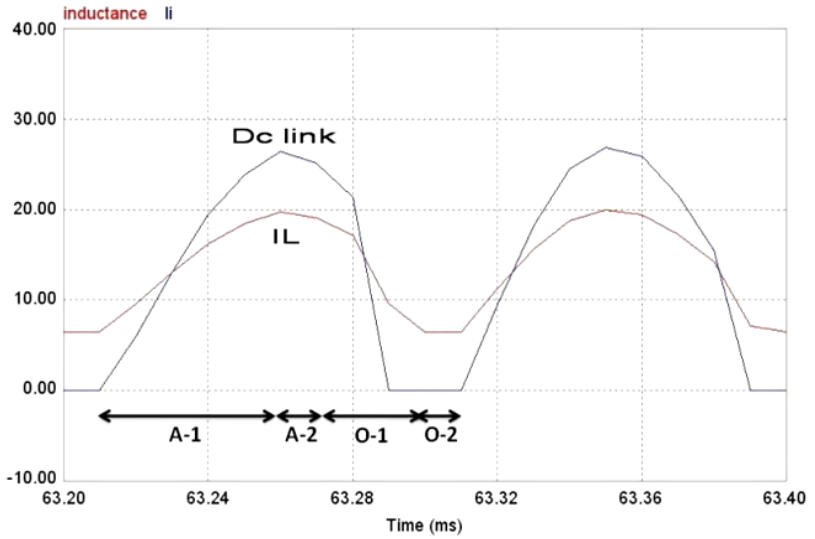

Fig. 12: Simulation results around the critical values of inductance and dc link current.

It can be seen that the there are two additional state, namely Active-2 and Open-2 states. Furthermore, I_l remains constant at $I_s/2 = 2.75$ A in Open-2 state and drops linearly in Active-2 state. SimilarlyV_c remains

constant at $V_o/2 = 14.69$ V during Active-2 state and increases linearly in Open-2 state. The results verify the accuracy of the design process.

The approximate and accurate values of the capacitor voltage and inductor current with simulation result for $k = 1$ are given in Table III.

Table III: Results For The Critical Values Of L & C

$k = 0.05$	Numerical	Approximate	simulation
L	0.135 mH	0.107 mH	–
C	4.58 μF	3.77 μF	–
$\bar{I}_l$	15.3 A	14.62 A	14.93 A
$\bar{V}_c$	81.88 V	78.32 V	61.7 V

Conclusion:

By analysing the steady states of the ZSCI some equations are derived, which by solving these equations in numerical methods accurate values of inductance and capacitance are achieved. Through the analysis it is shown that as the ripples of the inductor current and capacitor voltage become large, three additional static states appear in addition to the commonly used three dynamic states. Due to the high mathematical complexity of the equations, a simpler design method is presented by assuming the ripples to be small and linear. It is evident from the results of the design that the approximate values are very close to the accurate values. Therefore, when low ripple factor are selected, approximate values given by Section IV can be treated as the accurate values without much error. The accuracy of the approximate design method is verified by computer simulations using an illustrative example. In addition, the appearance of the critical values of capacitance and inductance is also demonstrated and the analysis presented is verified by considering a case where the ripples are allowed to be large.

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