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Low-Power, High-Throughput, Unsigned Multiplier Using A Modified Cpl Adder Cellfor Signal Processing Circuit

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Abstract: This paper proposes a full adder circuit that was designed by the Multiplexing Control Input Technique (MCIT) for a sum operation and the Boolean identities used for the carry operation. The proposed adder was implemented into the design of an 8x8-bit array multiplier circuit, specifically Braun, Baugh-Wooley (a 2's complement generator) and Modified Baugh-Wooley (with optimised interconnections) circuits that were designed for unsigned numbers. The 8x8-bit multiplier circuit was schematised by the DSCH2 VLSI CAD tool, whereas their layouts were generated by the Microwind 3 VLSI CAD tool. Output parameters, such as propagation delay, total chip area, and power dissipation are calculated from the simulated results. This paper extends to analyses for Energy Per Instruction (EPI), throughput, and latency by using the BSIM 4 advanced analyser. The power dissipation, EPI, throughput and area were analysed for different feature size. From these analyses of simulated results, it was found that the proposed adder-based multiplier circuit achieves better power dissipation and throughput performance than existing circuits.

Key words: array multiplier, BSIM4, power dissipation, propagation delay, proposed adder, and throughput.

INTRODUCTION

A digital multiplier relies on many different steps in its operation. Consequently, many different approaches have been taken to reduce size, delay and power consumption in the VLSI circuit design. These approaches were implemented in proposed adder cell design. Addition is a crucial operation because it usually involves a carry ripple step that must propagate a carry signal from each bit to its higher bit position. This results in a substantial circuit delay; therefore, a high-speed adder is often desired (Jonathan Ying Fai Tong, 2000). Currently, addition is a frequently used operation in general-purpose systems and application-specific processing systems. Design emphasis has shifted from optimising critical delay paths to minimising the number of transistors in an adder cell while still maintaining high performance (Huy, T., *et al*., 2000). An adder with low power dissipation and a high-speed VLSI can be constructed with different logic styles. The three important considerations for VLSI design are power, chip area and computation speed.

Complementary pass transistor logic is reported as an alternative logic that can enhance circuit performance, specifically in regard to speed (Dimitrios Soudris,). Because of complementary data input, output signals can propagate through the output node simultaneously. The technique of high functionality can reduce the number of transistors, yielding a less critical path. Pass transistor logic threshold voltage loss can be a problem and can be amended using pass transistor logic with an inverter at the output (Dimitrios Soudris,). Basically, pull-up PMOS transistors are necessary for swing restoration. Incomplete turnoff of the PMOSFET in the output inverter will result in a static current. A weak PMOSFET feedback device can be added in the pass transistor logiccircuit to pull the pass transistor outputs to a full supply voltage level. As a pass transistor logic-based circuit can consist of only NMOS transistors, it has a low node resistance path (Marković, D., *et al*., 2000). The PTLlogic enables the construction of a high-speed, reduced-power-dissipation circuit. However, the design aspects consider the implicit of routing overhead of complementary signals in pass transistor logic design.

In this paper, new adder is proposed, which is capable of doing fast multiplication. The 8x8 bit Braun, Baugh-Wooley and Modified Baugh-Wooley multipliers are designed using by adder cell (Huy, T., *et al*., 2000; Dimitrios Soudris). The proposed adder circuit was designed using Pass transistor logic and Boolean identities. The 8x8-bit multiplier circuit are schematized by using DSCH2 CAD tool and layouts are generated with the Microwind 3 VLSI CAD tool. The drain current effect with temperature variation was analysed with a BSIM4 analyser. The proposed modified pass transistor logic adder-based multiplier was simulated and results were compared with a MCIT-based adder cell multiplier, a pass transistor logicadder cell and other published results in terms of power dissipation, Energy Per Instruction (EPI), propagation delay, drain current effect, throughput and total chip area. According to the simulation results, proposed adder-based multiplier circuit achieves better performance than existing circuits.

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MATERIALS AND METHODS

The main concept behind pass transistor logicis the use of an NMOSFET network for the implementation of logic functions by applying a duality principle. The complementary principle of the pass transistor logicadder topology, with inverted pass signals, produces a complementary logic function in pass transistor logic. Pass variables are directly passed from the inputs to outputs; therefore, inversion of the pass variable yields the complementary function (Padmanabhan Balasubramanian, and Ryuta Arisaka, 2007). A CPL circuit also uses the lowest power per gate during logic transition, which makes it suitable for memory circuits. The architecture of three-array shared multipliers was implemented with the proposed adder, which is designed using MCIT Boolean identities.

II.1 Multiplexing Control Input Technique:

According to Boolean identities, we can generate pass transistor functions according to sum and carry equation. Pass transistor functions are represented by input variables when the expression result equals '1', and the pass transistor function is represented by the complement of the input variables when the expression result equals '0' (Marković, D., *et al*., 2000). To generate the pass transistor function for 'n' input variable functions, we use 'n-1' as control input data. (Padmanabhan Balasubramanian, and Ryuta Arisaka, 2007; Behrooz Parhami, 2000). The addition formula for each pair of bits (with carry in) has the same function as a full adder and is given by equations (1) and (2).

$$C_{i+1} = A_i B_i + (A_i \oplus B_i) C_i \tag{1}$$

$$S_i = A_i \oplus B_i \oplus C_i \tag{2}$$

After careful validation of the Boolean equation, the equations (1) and (2) simplified for the design of new full-adder technique.

II.2. Architecture of the proposed adder cell:

The fullest reduction can be achieved by using the Boolean identities, which simplifies logic expression into useful terms with each of the variables involved in the expression. It is particularly useful in multiplexer and complementary pass transistor circuit design. The Boolean equation is applied in conjunction with complementary pass transistor logic where the number of X-OR gates is reduced. A function for the carry bit can be written as:

$$C_{out} = (A \oplus B) C_{in} + AB \tag{3}$$

The Boolean equation is applied using the equations $\overline{A} + B = \overline{A} + AB$ and $A + B = \overline{A}B + A$. The input logic control signals flow vertically and data flow horizontally. The proposed full adder circuit is combined by the MCIT and Boolean theorems. The sum of the full adder circuit is designed using MCIT, and the carry is designed using the Boolean equation theorem shown in Fig 1. Input B and its complement are used as the control signal of the sum circuit. The number of control variables is limited to at most four, and the inverter is added after the input as a buffer (Pawel, P., *et al*., 2007). According to equation (3), the sum circuit needs to use three inputs to avoid the number of transistors increased. In this carry circuit; function *AB* is directly implemented in a NMOSFET, mean's that; pass variables can directly pass from inputs to outputs. Therefore, the number of transistors can be reduced to four in the carry circuit.

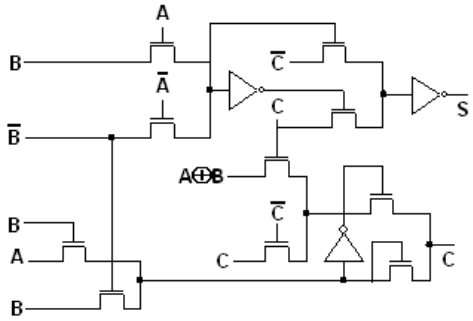

Fig. 1: Proposed adder cell

II.3. Multiplier Designs:

This paper was analysed for three different multipliers that are Braun, the Baugh-Wooley and the modified Baugh–Wooley multiplier circuits (Kiat-Seng Yeo and Kaushik Roy,), which designed by proposed adder circuit. The Braun multiplier, each partial product A and B are generated in parallel with AND gates (Marković, D., *et al*., 2000). The previous sum of the partial product is added with each partial product by a row of adders. Each carry out signal is shifted one bit to the left and then added to the sum of the first adder and the new partial product. The first row of the **Braun multiplier** adder component uses a half adder, which reduces the number of transistors in the whole multiplier circuit, as illustrated in Ref (Kiat-Seng Yeo and Kaushik Roy,). At the next stage of the adder, the carry bits are passed diagonally downward, where there is no horizontal carry propagation for the first rows. Instead, the carry bit is saved for the subsequent adder stage. The architecture of the **Baugh-Wooley multiplier** is based on the Braun Multiplier, illustrated in (Kiat-Seng Yeo and Kaushik Roy). It is designed to be capable of multiplication for both signed and unsigned operands that are represented in the 2's complement number systems. Signed multiplicands must first convert to their 2's complement representation before multiplication can occur with the control line Comp-Sig (Complementary Signal). The Baugh-Wooley core components were designed with the MCIT technique, which results in a reduced number of transistors compared to a conventional circuit. According to Kaushik Roy (Kiat-Seng Yeo and Kaushik Roy), the **Modified Baugh-Wooley multiplier** operates on signed operands with a 2's complement method to ensure that the signs of all the partial products are positive. Note that the last four lines are added for simplification purposes only, adding up to zero and thus not changing the result (Behrooz Parhami, 2000). Real-time, fast-array, share multipliers achieve fast multiplication by utilising AND gates and full adders. Operand sizes are limited by the large size of the array multiplier and by carry propagation in the adder cell. (Kiat-Seng Yeo and Kaushik Roy) Hardware utilisation in array-shared multipliers improves performance gains tremendously.

RESULTS AND DISCUSSION

Three different multiplier circuits (i.e., the Braun, the Baugh-Wooley and the Modified Baugh-Wooley circuits) were designed using the proposed 16T pass transistor logic-based adder and its layout simulated by the Microwind 3 VLSI CAD tool. The proposed modified pass transistor logic adder Simulation results are shown in Table I.

Table 1: PROPOSED 1-b ADDER RESULTS OF POWER DISSIPATION, PROPAGATION DELAY, AREA AND GATE LENGTH

Variable	*0.35µm (3.5V)*	*0.25µm (2.5V)*	*0.18µm (1.8V)*	*0.12µm (1.2V)*
P_D µW	12.47	3.205	1.809	1.799
Delay ps	82.6	23	37	18
Area μm^2	76x39	49x31	38x20	23x17
gate length µm	0.4	0.25	0.2	0.12

These results clearly illustrate that the 16-T pass transistor logic adder achieves low power dissipation. Circuits that require complementary signals like pass transistor logicare sometimes categorised as dual-rail logics. The need of complementary signals, a pass transistor logic circuit is sometimes twice as large as a CMOS circuit, although it is sometimes surprisingly small if a designer succeeds in fully utilising the functionality of a pass-transistor circuit. Results for a very fast and compact pass transistor logicfull adder, a multiplier, and a carry-propagate-chain circuit are reported herein.

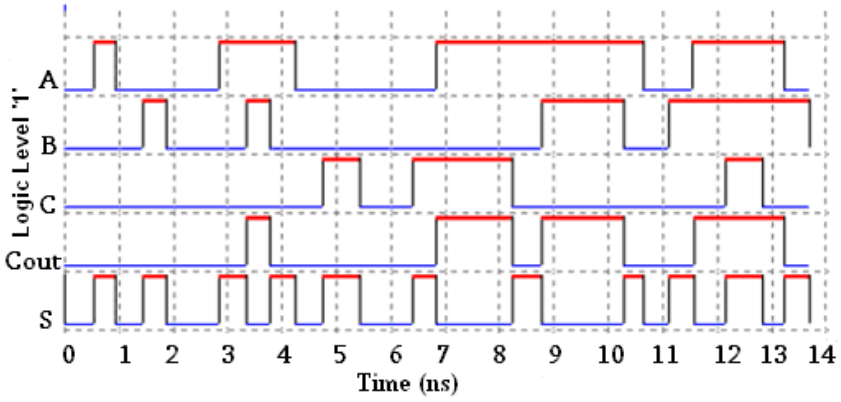

Fig. 2: Timing diagram of proposed full adder circuit

A full adder composed of CMOS logic gates was compared to compose of selectors in pass transistors. Speed and power consumption are significantly improved because of a less critical path in the proposed adder circuit. Another important extension of pass transistor logic is to incorporate CMOS circuits into a logic network (Chip-Hong Chang, *et al*., 2005). Logic networks based on pass transistors do not always have reduced area, delay, and power consumption when compared to CMOS logic networks. They are effective when selectors fit well with the target logic functions. According to selection input, the proposed full adder output is shown in Fig. 2. The proposed 1-bit adder circuit simulation results are compared with Chang *et al.* (2005) and Alioto *et al.* (2002) in terms of power dissipation, propagation delay, power delay product (PDP) and area. The proposed circuit gives better performance, which illustrates in Table II and III. As seen in Table II, proposed 1-bit adder cell has a shorter delay and less PDP than the 1-bit adders of Chang *et al.* (2005) and Alioto *et al.* (2002). The only drawback to proposed adder is that it occupies a large area. In this paper, we argue that 1-bit, full adder cells that function correctly in VLSI CAD tool simulations are validated to have sufficient real-life performance, functionality and reliability.

Table 2:PROPOSED 1-BIT ADDER COMPARISON IN TERMS PROPAGATION DELAY, PDP AND AREA

Adder type	Supply Voltage (V)	Power (μW)	% Reduction	PDP (fJ)	% Reduction	Delay (ns)	% Reduction	Area (μm^2)	% Reduction
This paper	1.2	1.799	---	0.0324	---	0.018	---	---	---
	2.0	1.809	---	0.0669	---	0.037	---	760	---
	2.5	3.205	---	0.0737	---	0.023	---	---	---
	3.5	12.47	---	0.1030	---	0.826	---	---	---
Chang et al. (2005) TGA	2.0	10.0	81.91	2.490	97.31%	0.294	87.41%	134.88	-82.25
	2.4	16.8	80.92	4.125	98.21%	0.250	90.80%	---	---
Chang et al. (2005) 14-T	2.0	18.8	90.38	4.78	98.60%	0.382	90.31%	68.24	-91.02
	2.4	31.0	89.66	7.94	99.07%	0.268	91.42%	---	---
Chang et al. (2005) 10T	2.0	56.5	96.80	160.3	99.96%	3.610	98.98%	70.56	-90.72
	2.4	86.4	96.29	50.5	99.85%	0.584	96.06%	---	---
Alioto et al. (2002) CMOS	1.8	5.472	66.94	7.99	99.16%	1.460	97.47%	---	---
	2.5	11.45	72.01	9.96	99.26%	0.870	97.36%	595	---
	3.3	21.37	41.65	13.68	99.25%	---	---	---	---
Alioto et al. (2002) CPL	1.8	9.62	81.20	10.20	99.34%	1.060	93.61%	---	---
	2.5	18.93	83.07	12.70	99.42%	0.671	93.65%	1091	---
Alioto et al. (2002) LEAP	1.8	5.79	68.76	9.96	99.33%	1.720	97.46%	---	---
	2.5	11.69	72.58	8.81	99.16%	0.753	96.28%	471	---
Alioto *et al*. (2002)LP	1.8	4.72	61.67	2.66	97.48%	0.564	93.44%	---	---
	2.5	10.09	68.24	2.46	97.00%	0.244	90.57%	252.5	---

The Braun multiplier circuit is dependent on the delay of the full adder cell and on the final adder in the last row. In the multiplier array, a full adder with balanced carry and sum delays are desirable because the sum and carry signals are in the critical path. The speed and power of the full adder are very important for large arrays. The worst-case delay is calculated for the inputs from 11111111x10000000. The result for various multiplier circuits (the Braun, the Baugh-Wooley [2's complement generator] and the Modified Baugh-Wooley [optimised interconnection]) are given in Table III. These results clearly suggest that the power consumption requirements and propagation delay are lower than other pass logic circuits, irrespective of gate length. This shows superiority of proposed adder-based multiplier circuit. From Table III, it is clear that the pass transistor logic is superior in terms of power dissipation and propagation delays. As a result of cross-coupling of the inverter in the output node terminal, the pass transistor logic has a logic transition from low to high or high to low that is faster and consumes less energy when compared to other circuit types. The adder and multiplier circuit designed with UDSM, which shrinkage of wire capacitance, load capacitance and stray capacitances. The multiplier circuits that are based on proposed cell also use fewer transistors than other techniques. EPI is a product of the capacitance toggled while processing the instruction and the supply voltage of the corresponding feature size. From Table III, it is clear that the EPI of these three different types of adder-based multipliers are on the order of Pico watts per IPS. If latency increases, the circuit's operating speed also decreases. The proposed adder-based multiplier gives lower latency than other designed multipliers, which designed in different techniques.

Table IV: MULTIPLIER RESULTS OF POWER DISSIPATION, THROUGHPUT, AREA, NUMBER OF TRANSISTOR and EPI OF BRAUN, BAUGH-WOOLEY and MODIFIED BAUGH-WOOLEY CIRCUITS.

Feature Size	Variable	Braun multiplier	Baugh-Wooley multiplier	Modified Baugh-Wooley multiplier
0.35µm	P D (mW)	1.733	3.794	1.494
	Delay ps	366	318	119
	Area μm^2	1126x79	1630x107	1374x91
	Throughput Gbps	1.155	1.222	1.616

	# transistor	256	391	290
	EPI pJ (Watt/IPS)	494.014	568.239	567.843
0.25µm	P D (mW)	0.536	2.808	0.150
	Delay ps	288	708	118
	Area μm^2	704x50	1019x67	859x57
	Throughput Gbps	1.269	0.828	1.618
	# transistor	256	391	290
	EPI pJ (Watt/IPS)	231.719	253.105	253.105
0.18µm	P D (mW)	0.250	0.809	0.394
	Delay ps	288	708	118
	Area μm^2	704x50	1019x67	859x57
	Throughput Gbps	1.420	0.539	1.477
	# transistor	256	391	290
	EPI pJ (Watt/IPS)	98.341	106.303	160.161
0.12µm	P D (mW)	0.020	0.233	0.046
	Delay ps	288	708	118
	Area μm^2	704x50	1019x67	859x57
	Throughput Gbps	1.828	0.968	1.094
	# transistor	256	391	290
	EPI pJ (Watt/IPS)	27.717	28.067	28.067

When implemented by the proposed pass transistor logic adder cell, the modified Baugh-Wooley multiplier circuit is superior than Baugh-Wooley multiplier in terms of power dissipation and propagation delay. The proposed adder-cell-based multiplier circuits were compared with other existing authors' circuits, and proposed circuits achieved better performance than all of these other circuit in terms of power dissipation and throughput. Throughput linearly increases with metal shrinkage, which illustrated in Table 3. In conjunction with ultra-deep, submicron technology for large arithmetic circuits, the length of wiring and area efficiency are prominent cost function elements. In the Micro wind layout simulator, the CMOS 0.35-µmfeature size design used a minimum gate length of 0.4µm. Contact size was decreased because of gate length variation, so a significant gap in interconnect efficiency was created between the submicron process and deep submicron process. This caused a reduction in the supply voltage, which in turn reduced power consumption. Additionally, this forced the I/O to operate at a high voltage for external compatibility and to function with a high immunity to external perturbations (Kiat-Seng Yeo and Kaushik Roy).

Table IV: COMPARISON WITH OTHER PUBLSIHED RESULTS IN TERMS POWER DISSIPATION AND THROUGHPUT

Author	References Types of multiplier	Voltage (V)	Power Dissipation (mW)	%of reduction	Throughput G/bits	%of reduction
proposed adder cells	ModifiedBough Wooley	3.5	1.494	----	1.616	----
		2.5	0.150	----	1.618	----
		1.8	0.394	----	1.477	----
M.Cwen *et.al* (2005)	Row bye pass	3.5	2.25	33.6%	----	----
Leonel *et.al* (2005)	Leonel ordinary	2.5	92	99.83%	----	----
	Leonel Diminished		78	99.80%	----	----
J S Wang *et.al* (2000)	Pipeline multiplier	3.5	----	----	0.625	61.32%
M. Olivier *et.al* (2001)	Pipeline multiplier	3.5	----	----	0.444	72.52%
R.Rogenmoser *et al* (2002)	SIMD Architecture	2.5	----	----	1.000	38.11%
Khatibzabeh and Raahemilier (2005)	Baugh	1.8	52.91	99.26%	---	---
Mudassir and Abid (2005)	Re.Array	3.5	2.633	43.26%	---	---
	Archi-I		1.842	18.19%	---	---
	Archi-II		1.416	-5.5%	---	---
Lee *et al*., (2001)	St.CMOS	2.5	96.99	99.85%	---	---
	St.CMOS	3.5	48.28	96.91%	---	---

The 8x8-bit modified Baugh-Wooley multiplier circuits were compared with published results, which illustrates in table 4. The proposed pass transistor logicadder-based multiplier circuit performed better than the row bypass multiplier circuit developed by M.C. Wen *et al.* (2005). The proposed circuit has 33.6% power reduction when compared with Wen's circuit. This is a result of fewer transistors being used in full-adder design. When proposed adder-based multiplier circuits are compared with those of Leonel *et al.* (2005), circuit gives outperforms in terms of power dissipation by 99.83% and 99.80%. The proposed multiplier circuits' throughput was compared with J.S. Wang *et al.* (2000) pipeline multiplier circuits, proposed adder circuit gives lower power dissipation and high performance than pipeline circuits due to pipeline circuits are used for the reference clock signal needed to communicate from one end to another end. The circuit provides improved

throughout, with rates up to 1.616 Gbps. Because of its pipeline architecture, the circuits of J.S. Wang *et al*. (2000) give lower throughput compared with circuits. When compared to the pipeline multiplier circuit of M. Oliver *et al.* (2001), circuits achieves better performance. As a result of fewer transistors being used in the adder cell, multiplier circuits achieve better throughput when compared to Oliver's circuits. The RSIMD architecture circuit of Rogen Moser *et al.* (2002) was compared with multiplier circuits and circuits achieved better performance because of its pass transistor logic architecture. The circuits achieved a 38.11% increase in throughput when compared with the SIMD architecture of R. Rogenmoser*et al.* The proposed adder based multiplier circuits are compared with the Khatibzabeh and Raahemilier (2005), the Mudassir and Abid (2005), and the Lee *et al.* (2001) circuits. The Khatibzabeh and Raahemilier (2005) circuits were compared with 0.18µm technology. The proposed circuit was also simulated using 0.18µm technology for comparison purposes. In this comparison, circuit give 99.9% lower power dissipation. The 8x8-bit multiplier circuit was compared with the Mudassir and Abid (2005) array, architecture –I and architecture –II circuits. Power dissipation was reduced compared to the array and architecture – I circuits by 43.26% and 18.19%, respectively.

The proposed adder-based multiplier circuit was analysed for parasitic capacitance effects. Parasitic capacitance analysis was achieved by using a BSIM 4 advanced layout design tool for various capacitances. Capacitance versus power dissipation and capacitance versus leakage current graphs are plotted and shown in Fig. 3. As temperature increased, the thermal velocity of carriers increased. Carriers spend less time near the ionised impurity area, resulting in a reduced scattering effect and larger mobility. Maximum drain current is dependent on the duration of the simultaneous on-times of the pull-up and pull-down networks, transistor sizes and power supply voltage levels. The magnitude of the drain current depends on the area of the drain diffusion and the leakage current density, which determines the operating current of the proposed circuit. The dynamic leakage current can be determined by varying the load capacitance value C_L.

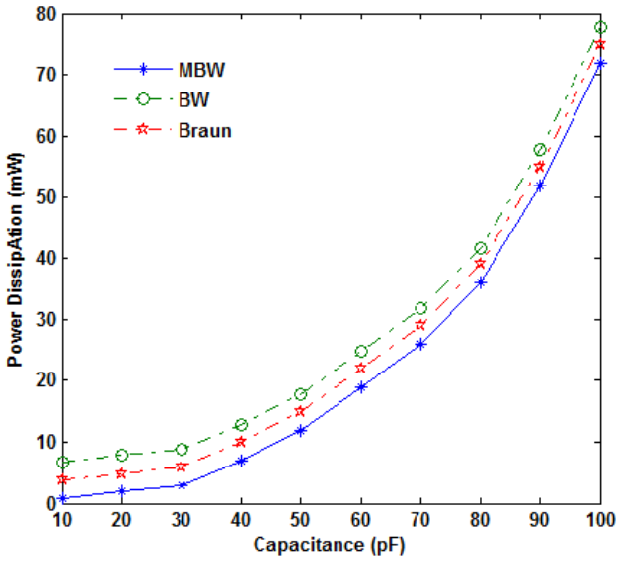

Fig. 3: Capacitance versus Power Dissipation curve for multiplier circuits

Supply voltage versus power dissipation and leakage current were analysed by using the BSIM 4 advanced layout design tool that is shown in Fig. 4 and Fig. 5. As a pass transistor logic -based circuit can consist of only one type of NMOS transistor, it has a low node resistive path. This results shows that the logic 1 transfer and we can use an input voltage $V_{in}=V_{DD.}$ Assuming an initial condition of V_{out} (t=0), the analysis gives

$$V_{out(t)} = V \max\left(\frac{t/2\iota_n}{1+t/2\iota_n}\right) \tag{4}$$

Conducting channels of NMOS transistors consist of electrons, which differs from the complementary metal oxide-semiconductor (CMOS) technology. As a result, proposed pass transistor logic enables a high-speed circuit with less power dissipation. As seen in Fig. 5, as the power supply voltage increases, the maximum operating current of the multiplier circuit increases.

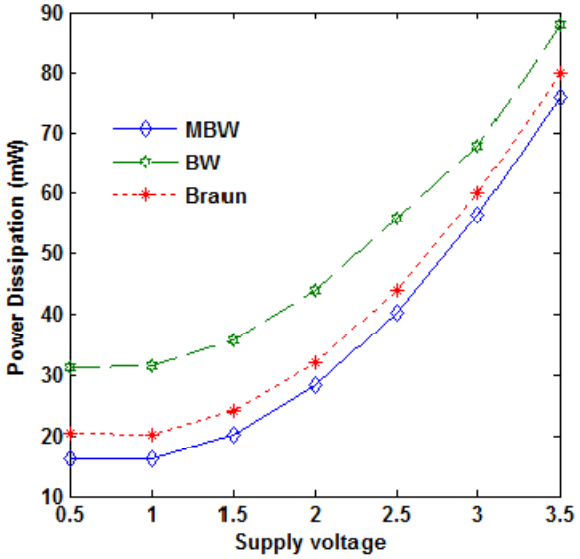

Fig. 4: Supply Voltage versus Power Dissipation curve for multiplier circuits

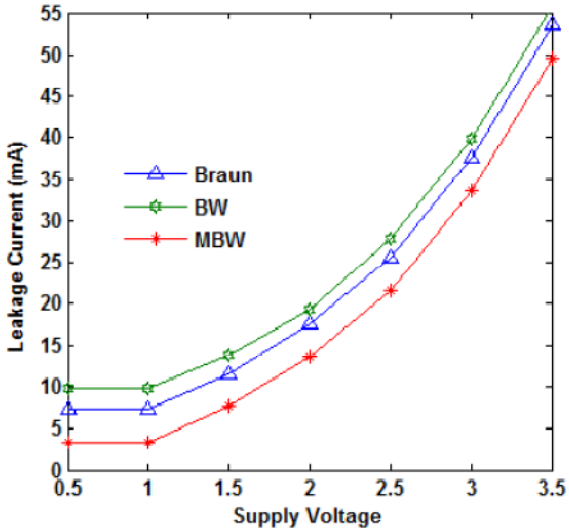

Fig. 5: Supply Voltage versus Leakage Current curve for multiplier circuits

Conclusion:

This paper describes an 8x8-bit multiplier circuit design and provides an analysis of its power dissipation, throughput, EPI and leakage current for different temperatures. The presented 8x8-bit multipliers are logically verified by using CMOS sizes of 0.35µm, 0.25µm, 0.18µm and 0.12µm. This parameter analysis was achieved with a BSIM4 analyser. The modified Baugh-Wooley multiplier circuit gives better performance than the other two multiplier circuits, (Braun and Baugh-Wooley multipliers) in terms of power dissipation, propagation delay, EPI and throughput. The Modified Baugh-Wooley multiplier gives low leakage current at various temperatures. The proposed adder-based multiplier circuits give better improvement than other existing circuit, which may use for signal processing and embedded circuits.

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