Australian Journal of Basic and Applied Sciences, 6(5): 88-96, 2012
ISSN 1991-8178

A Simulation-Based Optimization Of Operational Transconductance Amplifier Using An Evolutionary Algorithm

[1]Roohollah Nakhaei, [2]Alireza Mallahzadeh

[1]Department of Electronics, Behbahan Branch, Islamic Azad University, Behbahan, Iran
[2]Department of Electronics, Bushehr Branch, Islamic Azad University, Bushehr, Iran

Abstract: In this paper we propose a simulation based approach for optimizing the performance of operational transconductance amplifier by use of particle swarm optimization algorithm. There are some trade-offs between Gain, BW, PM, CMRR and PSRR in OTA design which force the designer to accomplish such a long time complicated work to optimize the circuit. In this work the usage of PSO algorithm in automated optimization of OTA has been investigated. The PSO algorithm is implemented in MATLAB which has been linked with an electrical simulator, HSPICE. It gets a netlist as its input while the output is active devices sizes and passive values. Obtained results which compared with three other works prove the effectiveness of this approach.

Key words: folded cascade OTA, PSO, circuit design optimization, evolutionary algorithm, CMOS.

INTRODUCTION

Nowadays, due to increasing demand for system on chip (SoC) productions, high performance analog integrated circuit design such as operational transconductance amplifier (OTA) in CMOS technology becomes more important. The OTA is well known for its high bandwidth in open-loop configuration (Mariano Jimenez-Fuentes *et al*, 2009), which makes it proper for widespread application such as xDSL, 802.11 a/g WLANs, WiMax and DVB (W. Goralski, 2002), (G. Cherubini *et al*., 2002).

. The OTA should provide sufficient transeconductance gain with acceptable linearity and power consumption. Moreover, a proper phase margin which guarantees the stability is needed. Also, CMRR and PSRR are two important specifications of an OTA. Two or more of these specifications are conflicting, i.e. improving one, forces the other(s) to worsen. Therefore there are some tradeoffs between BW, PM, CMRR, PSRR, gain, linearity and power consumption in OTA design (E. Sanchez-Sinencio, 2000; J. Silva-Martinez, 2000).

There are tens of variables in the design of a typical analog integrated circuit (such as an OTA). Designers must manually, continuously and repeatedly tune the designed circuit elements such as active devices parameters and sizes, passive devices parameters, biasing conditions, etc and perform a circuit simulation using an electric computer-aided design (ECAD) software, to achieve the best performance of the designed circuit. It is in general a long time, high complexity and complicated work. As the relation between transistor sizes and circuit specifications is often complex, nonlinear and conflicting, the problem of finding an optimum solution point is difficult to be exactly solvable. A proper automatic optimization technique can be used to overcome this tedious problem.

In this work, we present a simulation based approach for optimizing the performance of folded cascade OTA using particle swarm optimization algorithm. This algorithm has been implemented in MATLAB (http://www.mathworks.com/products/matlab). Hence, a proper link between MATLAB and HSPICE (http://www.synopsys.com/products/mixedsignal/hspice/hspice.htm), an electrical simulator for performance evaluation of circuit, has been established.

This paper is organized as follows: in Section II, the particle swarm optimization concept is explained. The OTA circuit and specifications is described In Section III. In Section IV, we propose the method of optimizing OTA design using PSO and achieved results. Finally, the conclusions are presented in section V.

Related Works:

The design flow for analog circuits consists of a series of design steps from the system level to the device level (G. Gielen, 2000; R. Rutembar, 2000), (R. Sommer *et al*., 2002), (C. Toumazou, 1995; C. Makris, 1995). Most important steps between these hierarchical levels are topology selection, circuit sizing and design verification. Basically, the optimization is accomplished in the circuit sizing level that receives a topology description, a set of performance specifications and technology parameters and produces a sizing solution for the described topology.

Corresponding Author: Roohollah Nakhaei, Behbahan Branch, Islamic Azad University, Behbahan, Iran,
E-mail: r.nakhaei@gmail.com

Two approaches are developed for circuit sizing: knowledge-based and optimization-based. The basic idea of knowledge-based approaches is to capture and emulate the knowledge and experience of designers in the form of rules and thus automate the sizing process. BLADES (F. El-Turky, 1989; E. Perry, 1989), IDAC (M. Degrauwe *et al*., 1987) and OASYS (R. Harjani *et al*., 1989) are some examples of this approach. The dependence on designer experience limits such methods from being easily extensible. For example, in order to design a new circuit or integrate a new component, a large number of analytic equations have to be manually derived. This makes such tools cumbersome for practical usage.

In optimization-based approaches, the circuit sizing is translated into an optimization problem which is an iterative process wherein design variables are updated at each iteration through a numerical method. Essentially, a performance evaluator is introduced in the iterative optimization loop. Optimization-based approaches can be classified based on the class of evaluators they use: equation-based and simulation-based.

In equation-based methods, the performance evaluator is based on equations describing the behaviour of the circuit. Some of the most relevant works are OPASYN (H.Y. Koh *et al*., 1990), STAIC (J.P. Harvey *et al*., 1992), MAULIK (P.C. Maulik, 1991; L.R. Carley, 1991), ASTRX/OBLX (E.S. Ochotta *et al*., 1996) and AMGIE (G. Gielen *et al*., 1995). However, the simplifications and approximations required in deriving equations cause low accuracy and incompleteness in equation-based methods.

Unlike equation-based methods, simulation-based approaches, such as FRIDGE (F. Medeiro *et al*., 1994), DELIGHT.SPICE (W. Nye *et al*., 1988), FASY (A. Torralba *et al*., 1996), ANACONDA (R. Phelps *et al*., 2000), MAELSTROM (M. Krasnicki *et al*., 1999), DARWIN (W. Kruiskamp, 1995; D. Leenaerts, 1995), (Lihong Zhang, 2004; U. Kleine, 2004) and (J.R. Koza *et al*, 1997), use a simulator, usually the ubiquitous SPICE program, as a performance evaluator. Using spice for evaluation guarantees that the design solution obtained is highly accurate. Additionally, manual derivation of performance equations is not required. However, using a simulator at each iteration of the loop makes the optimization procedure a little time consuming, but creating the equations perhaps consumes much more time. Therefore, we use a simulation-based approach in this work.

Apart from evaluation method, different optimization methods such as constrained optimization techniques (P.C. Maulik, 1991; L.R. Carley, 1991), statistical optimization (F. Medeiro *et al*., 1994), fuzzy-logic (A. Torralba *et al*., 1996), geometric programming, convex optimization and genetic algorithm are used for circuit sizing. Limitations of these methods instigate the researchers to utilize novel optimization methods. In the last decade, there has been a growing interest in evolutionary optimization methods. Although the underlying mechanisms are simple, these algorithms have proven themselves as general, robust and powerful search tools (K. Deb, 2001). GA is the most popular evolutionary algorithm used in circuit sizing (Giuseppe Nicosia *et al*., 2008), (M. Barros *et al*., 2006), (C. Goh, 2001; Y. Li, 2001), (J. Koza *et al*., 1997), (M.Barros *et al*., 2007); but its ability and efficiency in search and convergence to global optimum have been criticized, especially when the problem has multiple local optimum. Particle swarm optimization is a new and robust evolutionary optimization method which has an extra ability in solving continues nonlinear optimization problems. In this work, the usage of this method in circuit design optimization has been investigated.

Particle Swarm Optimization:

Particle swarm optimization (PSO), first introduced by Kennedy and Ebehart (J. Kennedy,1995; R.C. Eberhart, 1995), is an evolutionary computation method based on the social behaviour and movement of swarm searching for the optimal and best location in a multidimensional search space and has been found to be robust in solving continues nonlinear optimization problems (J.schneider, 2006;S.kirkpatrick, 2006).

This approach simulates the social behaviour of bird flocking or fish schooling model. Potential solutions of optimization problem are called particles. Each *particle position* is represented by a d-dimensional vector and denoted as $X_i=[x_{i1},x_{i2}, \ldots, x_{id}]$ and is randomly initialized . The set of n particle in the swarm are called *population*: $X=[X_1, X2,\ldots,X_n]$. Each particle is assumed to move around in the so called multidimensional space to reach the best position which has the best fitness value. In each iteration of simulation the fitness function for each particle is evaluated to updates the *best previous position*: $PB_i= [pb_{i1}, pb_{i2},\ldots, pb_{id}]$, which is the location of the best fitness value obtained so far by the particle.. The best position among the population is called *global best position* and described as $GB_i= [gb_1, gb_2,\ldots, gb_d]$.

The rate of position change for each particle is called particle velocity: $V_i = [v_{i1}v_{i2}, \ldots , v_{id}]$. each particle would like to return to its own optimum point, so the velocity has a term proportional to (pb_i-x_i), it would like to follow overall best global optimum point too, so a term proportional to $(gb-x_i)$ is added to velocity. Therefore:

$$v_{id}^{k+1} = wv_{id}^{k} + c_1 rand_1^{k} (pb_{id} - x_i^{k}) + c_2 rand_2^{k} (gb_d^{k} - x_{id}^{k}) \quad (1)$$

Where w is intera weight parameter which controls the trade off between the global and the local search capabilities of the swarm. c_1 and c_2 are acceleration factors and indicate the relative attraction toward *pb* and *gb* respectively. $rand_1$ and $rand_2$ are two random numbers uniformly distributed between 0 and 1, which indicate

the craziness of particles[36]. *k* is the iteration number. The new position of i-th particle is then determined by:

$$x_{id}^{k+1} = x_{id}^{k} + v_{id}^{k+1} \quad (2)$$

Generally PSO has the advantage of being very simple in concept, easy to implement and computationally efficient algorithm. Since updates in algorithm consist of simple adding and multiplication operators and no derivation operation is included, computation time is dramatically decreased compared to other heuristic algorithms. In order to avoid premature convergence, PSO utilizes a distinctive feature of controlling a balance between global and local exploration of the search space which prevents from being stacked to local minima (M. Clerc, 2002).

System Platform:

The purpose of optimization is to achieve the optimal size of MOS transistors (channel length and width) and bias currents of the circuit, in order to meet the desired specifications. This paper proposes a technique that utilizes a simulation-based approach for circuit design optimization.

The system platform is illustrated in Fig. 1. The starting point is a spice-like netlist of the circuit topology, currently entered in the optimization engine as its input. Desired specifications are other inputs. Optimization engine consist of a PSO algorithm written in MATLAB which has been linked with an electrical simulator, HSPICE, as its performance evaluator.

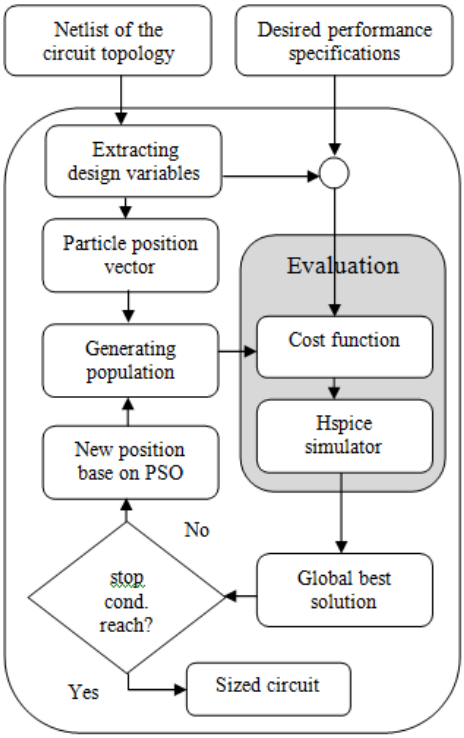

Fig. 1: System platform

Optimization is executed on a vector of design variables of circuit extracted from the netlist. In fact, the particle position vector is the channel length (L) and width (W) of MOS transistors and bias currents.

At first, each particle (i-th particle) position vector is randomly initialized. In each iteration, the algorithm runs the HSPICE for each particle and evaluates a cost function (CF), described in (3):

$$CF = \sum_{i=1}^{k} w_i \left| \frac{f_i(x) - f_{id}}{f_{id}} \right| \quad (3)$$

Which, $f_i(x)$ is i-th design specification, k is the number of specifications, f_{id} is desired value for i-th design specification and w_i are the importance factors that say which specification has more importance for designer

regarding to different especial applications of the circuit. With this approach, the searching algorithm (optimizer) will find the best solution that meets this cost function. Therefore, PB and GB are showing the minimum CF for best previous position and global best position respectively that each particle attempts to reach them. At the end of each iteration, GB gives the best solution of the population.

The end of the optimization process happens when a stop condition is satisfied. The stop condition can be a maximum number of iterations or the minimum variation of the cost function value (evaluation function).

Design Examples And Results:

The performance of described method in analog circuit sizing is tested in design of two popular cases of operational transconductance amplifier.

We have simulated the circuits using CMOS TSMC parameters for 0.18 μm mixed signal and BSIM30 version 3.1 (http://www.mosis.com).

Experiments are conducted in a Pentium IV, 2.4GHz, 4GB RAM with Windows XP Professional OS. The code is developed and implemented in MATLAB 2009a and simulations are performed in HSPICE A-2007.09.

A. A folded cascode OTA design:

The circuit schematic of the folded-cascode OTA is shown in Fig. 2. It consists of two stages: the first one is an NMOS differential pair as input stage; and the second stage is a cascode output stage. An ideal transconductance amplifier is an infinite bandwidth voltage-controlled current source, with an infinite input and output impedance which used to drive small capacitive loads at high frequencies (E. Sanchez-Sinencio, 2000; J. Silva-Martinez, 2000). The folded cascode architecture is used in order to increase the DC gain, common mode rejection ratio and the output resistance.

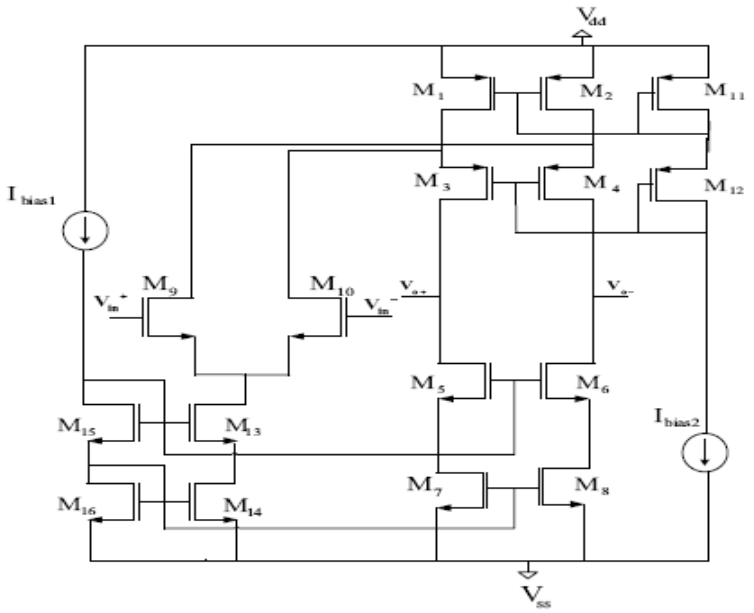

Fig. 2: Folded cascade OTA architecture

The performance specifications of circuit are tabulated in table 1. These specifications are expressed as functions of design parameters such as transistor sizes, passive values and bias conditions which must be optimized during the optimization process discussed in next section.

Table 1: Performance Specifications of FCOTA

No	Specifications	Constrains	Unit
1	DC gain	> 80	db
2	Unity-gain frequency	> 200	MHz
3	CMRR	> 70	db
4	PSRR	> 70	db
5	Slew rate	> 100	V/□s
6	Phase margin	> 50	°
7	Power consumption	< 3	mw

.

The results of performance optimization of folded cascode OTA in comparison with two other works (H. Daoud *et al*, 2008) and (S. Bensalem *et al*, 2008), are listed in table 2. Spice simulation results of the gain, CMRR and PSRR are depicted in fig. 3, 4 and 5 respectively.

Table 2: Optimization Results and Comparison

Specifications	This work	[H. Daoud *et al*]	[S. Bensalem *et al*]
DC gain	84.33	82.89	77.53
Unity-gain frequency	543.3	533.55	430
CMRR	95.6	93.56	114
PSRR	84.37	73.23	46.5
Slew rate	534		
Phase margin	51.34	43	45.5
Power consumption	1.2		

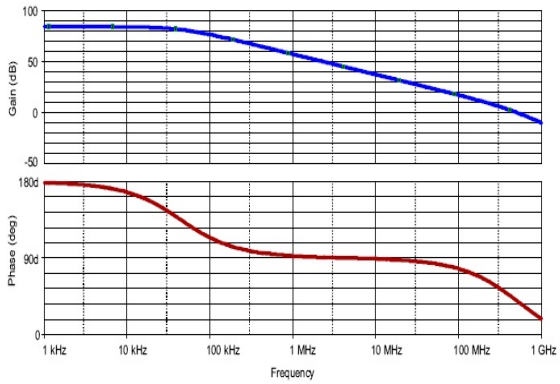

Fig. 3: Gain and phase of FC OTA vs. frequency

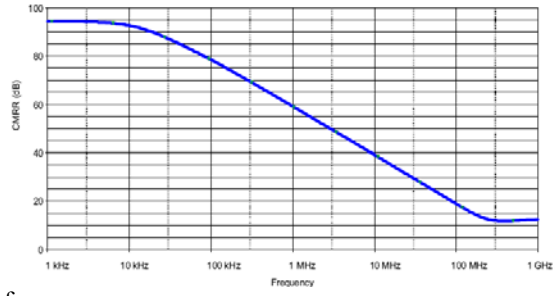

Fig. 4: CMRR of FC OTA vs. frequency

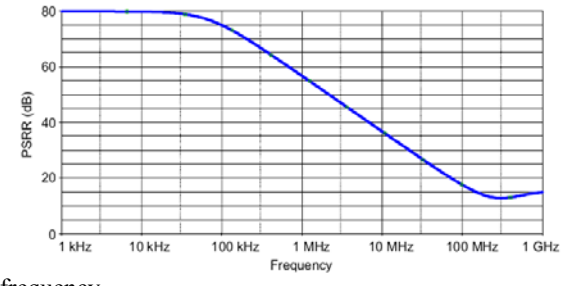

Fig. 5: PSRR of FC OTA vs. frequency

B. A MILLER OTA design:

The Miller OTA amplifier is a two-stage amplifier with a feedback capacitor. This amplifier has the design specifications as in Table 3, which expressed as functions of design parameters that must be optimized during the optimization process.

Table 3: Performance Specifications of miller OTA

No	Specifications	Constrains	Unit
1	DC gain	> 80	db
2	UBW (MHz)	> 10	MHz
3	CMRR	> 70	db
4	PSRR	> 70	db
5	Slew rate	> 1	V/□s
6	Phase margin	> 60	°
7	Power consumption (μw)	< 0.5	mw

Fig.6 describes the topology of the circuit. It has 8 CMOS transistors labeled as M1 to M8, a compensation capacitor (Cc) and a load capacitor. Table 4 presents different design variables, where W1 . . . W8 corresponds to the gate width of transistors M1 . . . M8 respectively.

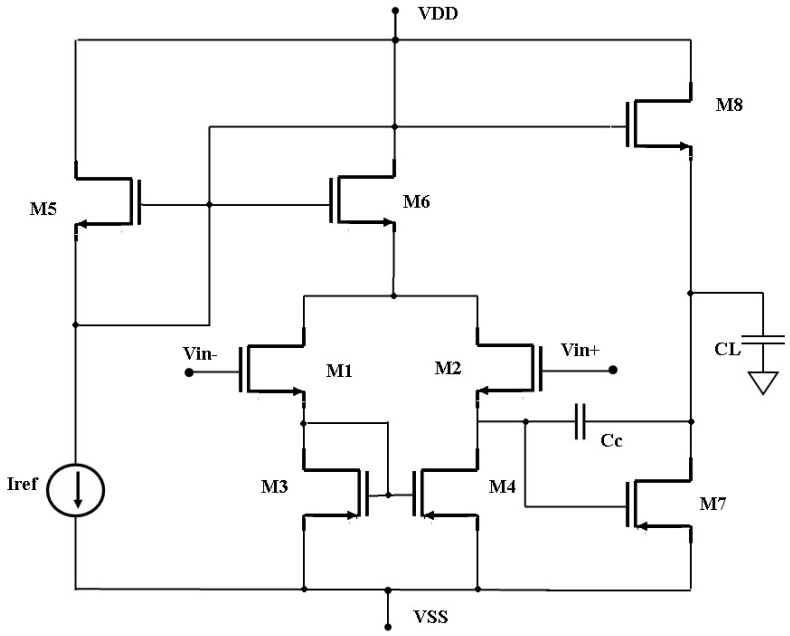

Fig. 6: Miller OTA architecture

Table 4: The design variables

Design variable	min	max	achieved
W1=W2 (μm)	50	150	98.87
W3=W4 (μm)	5	20	14.75
W5=w6 (μm)	5	20	14.62
W8 (μm)	50	150	103.12
W7(μm)	50	300	212.96
C_c (pF)	1	10	2.64
Iref (μA)	1	10	2.23

The results of performance optimization of miller OTA in comparison with two other works (Bo Liu *et al*, 2009), (Alessandro Girardi, 2007; Sergio Bampi, 2007), are listed in table 5. Spice simulation results of the gain, phase and CMRR are depicted in fig. 7, 8 and 9 respectively.

This comparative study shows that the PSO gives better results than the gm/Id methodology (Alessandro Girardi, 2007; Sergio Bampi, 2007). The efficiency and the convergence of PSO in comparison with other evolutionary technique (Bo Liu *et al*, 2009) can be clearly seen, especially, when we deal with more complexes optimization problems containing more variables and constraints.

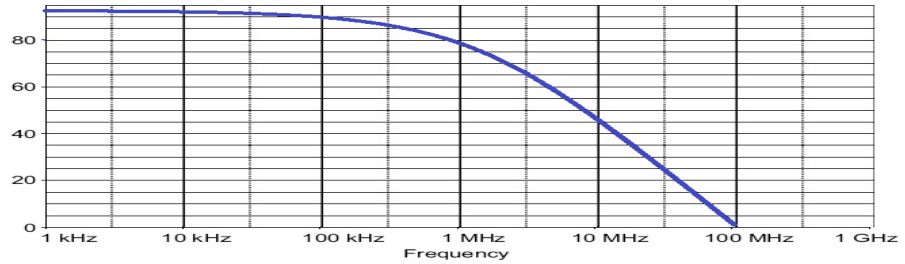

Fig. 7: Gain of Miller OTA vs. Frequency

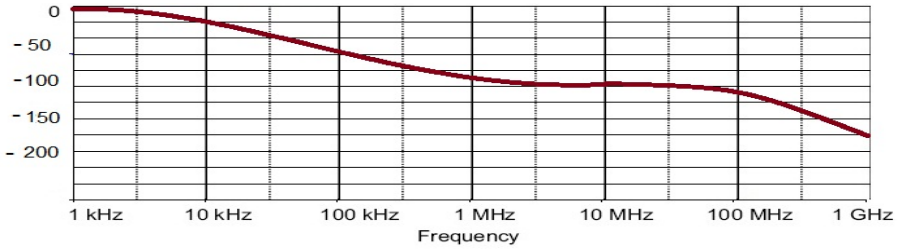

Fig. 8: phase of Miller OTA vs. frequency

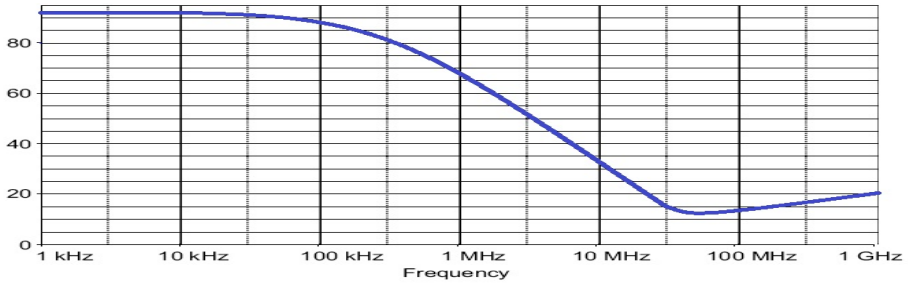

Fig. 9: CMRR of Miller OTA vs. frequency

Table 5: Optimization Results and Comparison

Specifications	This work	[Bo Liu *et al*]	[Alessandro Girardi *et al*]
DC gain	94.29	86.1	95
UBW (MHz)	18.2	2.5	15
CMRR	92.6	80.45	-
PSRR	88.37	86.13	83
Slew rate	1.81	1.97	1.5
Phase margin	61.04	57.74	60
Power consumption (µw)	125	1014	168
Convergence time(s)	7312	11206	-

Conclusions:

In this paper, a PSO based approach for optimal design of operational transconductance circuit has been reported. Electrical specifications of the OTA circuit considered in the optimization process are the gain, unity gain frequency, common mode rejection ratio, power supply rejection ratio, slew rate, phase margin and power consumption. The performance of described method in analog circuit sizing is tested in design of two popular cases of operational transconductance amplifier. The results of this work indicate the effectiveness of this optimization approach that is a time consuming method.

We note that this approach can also be applied to optimize other circuit and can be embedded into any electronic CAD software which improves the process of design and fabrication.

REFERENCES

Alessandro Girardi, Sergio Bampi, 2007. Power Constrained Design Optimization of AnalogCircuits Based on Physical gm/ID Characteristics. Journal Integrated Circuits and Systems v.2 / n.1: 22-28.

Barros, M., G. Neves and N.C. Horta, 2006. AIDA: Analog IC design automation based on a fully configurable design hierarchy and flow. In the Proceedings of the 13th IEEE International Conference on Electronics, Circuits and Systems (ICECS), France, pp: 490-493.

Barros, M., J. Guilherme and N. Horta, 2007. GA-SVM feasibility model and optimization kernel applied to analog Ic design automation. In the Proceedings of the 17th ACM Great Lakes Symposium on VLSI, Italy pp: 469-472.

Bensalem, S., S. Zouari and M. Loulou, 2008. Design of folded cascode OTA in different regions of operation through gm/ID methodology. In the Proceeding of World Academy of Science, Engineering and technology, 35: 45-51.

Bo Liu, YanWang, ZhipingYu, Leibo Liu, Miao Li, Zheng Wang, Jing Lu and Francisco V. Fernandez, 2009. Analog circuit optimization system based on hybrid evolutionary algorithms. INTEGRATION, the VLSI journal, 42: 137-148.

Cherubini, G., E. Eleftheriou, S. Olcer, 2002. Filtered multitone modulation for very high-speed digital subscriber lines. IEEE J. Sel. Areas Commun., 20: 1016-1028.

Clerc, M., 2002. The particle swarm Explosion, stability and convergence in a multidimensional complex space., IEEE Trans. Evol. Comput: pp: 58-73.

Daoud, H., S. Bennour, S.B. Salem and M. Loulou, 2008. Low power SC CMFB folded cascode OTA optimization. In the Proceedings of the IEEE International Conference on Electronics, Circuits and Systems, ICECS, Malta, pp: 12-18.

Deb, K., 2001. Multi-Objective Optimization Using Evolutionary Algorithms. Wiley

Degrauwe, M. *et al*., 1987. IDAC: an interactive design tool for analog CMOS circuits. IEEE J. Solid-State Circuits, 22: 1106-1115.

El-Turky, F., E. Perry, 1989. BLADES: an artificial intelligence approach to analog circuit design. IEEE Trans. Comput. Aided Des., 8: 680-692.

Gielen, G., *et al*., 1995. An analog module generator for mixed analog/digital ASIC design. Wiley Int. J. Circuit Theory Appl., 23: 269-283.

Gielen, G., R. Rutembar, 2000. Computer-aided design of analog and mixed-signal integrated circuits. IEEE Proc., 88(12): 1825-1854.

Giuseppe Nicosia, Salvatore Rinaudo and Eva Sciacca, 2008. An evolutionary algorithm-based approach to robust analog circuit design using constrained multi-objective optimization. Knowledge-Based Systems, 21: 175-183.

Goh, C., Y. Li, 2001. GA automated design and synthesis of analog circuits with practical constraints. IEEE Cong. Evol. Comput., 1: 170-177.

Goralski, W., 2002. ADSL and DSL Technologies, second ed. Osborne/McGraw-Hill, Berkeley.

Harjani, R., R. Rutenbar and L.R. Carley, 1989. OASYS: a framework for analog circuit synthesis. IEEE Trans. Comput. Aided Des., 8: 1247-1265.

Harvey, J.P., M.I. Elmasry and B. Leung, 1992. STAIC: an interactive framework for synthesizing CMOS and BICMOS analog circuits. IEEE Trans. Computer Aided Des., 11(11): 1402-1417.

http://www.mathworks.com/products/matlab

http://www.mosis.com

http://www.synopsys.com/products/mixedsignal/hspice/hspice.htm

Kennedy, J., R.C. Eberhart, 1995. Particle swarm optimization, in the Proceedings of IEEE International Conference on Neural Networks, pp: 1942-1948.

Koh, H.Y., C.H. Sequin and P.R. Gray, 1990. OPASYN: a compiler for CMOS operational amplifiers. IEEE Trans. Comput. Aided Des., 9(2): 113-125.

Koza, J., F. Bennett, D. Andre, M. Keane and F. Dunlap, 1997. Automated synthesis of analog electrical circuits by means of genetic programming. IEEE Trans. Evol. Comput., 1(2): 109-128.

Koza, J.R., F.H. Bennett, D. Andre, M.A. Keane and F. Dunlap, 1997. Automated synthesis of analog electrical circuits by means of genetic programming. IEEE Trans. Evol. Comput. 1(2): 109-128.

Krasnicki, M., R. Phelps, R. Rutenbar and L.R. Carley, 1999. MAELSTROM: efficient simulation-based synthesis for custom analog cells. In the Proceedings of the ACM/IEEE Design Automation Conference (DAC, pp: 945-950.

Kruiskamp, W. and D. Leenaerts, 1995. DARWIN: CMOS opamp synthesis by means of a genetic algorithm. In the Proceedings of the ACM/IEEE Design Automation Conference (DAC), p: 550-553.

Lihong Zhang, U. Kleine, 2004. A novel analog layout synthesis tool. In the Proceedings of the International Symposium on Circuits and Systems, 5: 101-104.

Mariano Jimenez-Fuentes *et al*, 2009. A tunable highly linear CMOS transconductor with 80 dB of SFDR. INTEGRATION, the VLSI journal, 42: 277-285.

Maulik, P.C., L.R. Carley, 1991. Automating analog circuit design using constrained optimization techniques. In Proceeding of Aided Design IEEE International Conference on Computer-Aided Design, pp: 390-393.

Maulik, P.C., L.R. Carley, 1991. Automating analog circuit design using constrained optimization techniques. In the Proceedings of Aided Design IEEE International Conference on Computer-Aided Design, pp: 390-393.

Medeiro, F., *et al*., 1994. A statistical optimization-based approach for automated sizing of analog cells. In the Proceedings of the ACM/IEEE International Conference on Computer-Aided Design (ICCAD), pp: 594-597.

Nye, W., D.C. Riley, A. Sangiovanni-Vincentelli and A.L. Tits, 1996. DELIGHT.SPICE: an optimization-based system for the design of integrated circuits. IEEE Trans. Compute. Aided Des., 7(4): 501-519.

Ochotta, E.S., R.A. Rutenbar and L.R. Carley, 1996. Synthesis of high-performance analog circuits in ASTRX/OBLX. IEEE Trans. Comput. Aided Des., 15(3): 273-294.

Phelps, R., M. Krasnicki, R. Rutenbar, L.R. Carley, J. Hellums, 2000. ANACONDA: simulation-based synthesis of analog circuits via stochastic pattern search. IEEE Trans. CAD 19(6): 703-717.

Sanchez-Sinencio, E., J. Silva-Martinez, 2000. CMOS transconductance amplifiers, architectures and active filters: a tutorial. IEE Proc. Circuits Devices Syst., 147(1): 3-12.

Sanchez-Sinencio, E., J. Silva-Martinez, 2000. CMOS transconductance amplifiers, architectures and active filters: a tutorial. IEE Proc. Circuits Devices Syst., 147(1): 3-12.

schneider, J., S. kirkpatrick, 2006. Stochastic optimization. springer-verlag berlin Heidelborg.

Sommer, R., I. Rugen-Herzig, E. Hennig, U. Gatti, P. Malcovati, F. Maloberti, K. Einwich, C. Clauss, P. Schwarz, and G. Noessing, 2002. From system specification to layout: seamless top-down design methods for analog and mixed-signal applications. In the Proceedings of the Design Automation and Test in Europe Conference and Exhibition, pp: 884-891.

Torralba, A., J. Chavez and L.G. Franquelo, 1996. FASY: a fuzzy-logic based tool for analog synthesis. IEEE Trans. Comput. Aided Des. Integrated Circuits., 15(7): 705-715.

Toumazou, C., C. Makris, 1995. Analog IC design automation: part I-automated circuit generation: new concepts and methods. IEEE Trans. Comput. Aided Des., 14: 218-238.