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Design of a Multi Valued Current Mode Comparator

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Abstract: In this paper, a low-power quaternary comparator circuit using current-mode CMOS multiple-valued logic (MVL) circuits has been presented. Existing MVL comparator circuits consume high power. The circuit presented in this paper low power. It has been simulated with PSPICE using the transistor model parameter values of the BSIM3 NMOS model V3.2 for 0.13μm CMOS process. With a 1.3-volt power supply, simulations show that the proposed quaternary comparator consumes 0.107 mW total average static power and a sampling rate 500MHz. Power and speed for comparators designed in these technologies are discussed. The comparator design is suitable for the needs of mixed-signal integrated circuit design and can be implemented as a conversion circuit for systems based on multiple-valued logic design.

Key words: Quaternary, CMOS, MVL, comparator.

INTRODUCTION

The comparator compares analog signal with another analog signal or reference and outputs a binary signal based on the comparison. The comparator is widely used in the process of converting analog signal to digital signals. It is an important device widely used in Analog to Digital Converter (ADC). Among the many architectures of ADC, Sigma delta, designs are used in a large class of applications ranging from low frequency (Maja, *et al.*, 1994) and audio (Reynolds, *et al.*, 1987) to down converted intermediate frequency and digital video (Wang, *et al.*, 2007). Their property to Trade speed for accuracy makes them more attractive in the context of present CMOS technology evolution (Current, *et al.*, 2008). The multiple valued logic comparator circuit was developed with high power consumption (Temel, *et al.*, 2006; Sheikhaei, *et al.*, 2007). Low power and high speed comparators are the main building blocks in the front-end of a radio-frequency receiver in most of the modern telecommunication systems (Yongheng, *et al.*, 2009). The ever-growing application of portable devices makes the power consumption a very critical constraint for circuit designers. Comparators are used in ADCs, data transmission, switching power regulators, and many other applications.

The comparator design plays an important role in high speed ADCs. Power consumption and speed is key metrics in comparator design (Gray, *et al.*, 1993). For all high speed ADCs, regardless of the architecture, one of the critical performance limiting building blocks is the comparator, which in large measure determines the overall performance of data converters, including the maximum sampling rate, bit resolution, and total power consumption (Nyquist, *et al.*, 1928).

This design proposed the high speed & low power consumption comparators build on radix-4 multiple valued logic design.

Comparator design:

The comparator is a critical part of almost all kind of analog-to-digital (ADC) converters. Depending on the type and architecture of the comparator, the comparator can have significant impact on the performance of the target application. The speed and resolution of an ADC is directly affected by the comparator input offset voltage, the delay and input signal range. Depending on the nature, functionality and inputs, comparators are classified into different types i.e. voltage and current comparators, continuous and discrete time comparators etc. Some basic applications of comparators are analog-to-digital conversion, function generation, signal detection and neural networks etc.

Fig. 1 shows the schematic of a comparator cell. In Fig. 1, transistors M22, M19, M21, M23, M18, and M20 buffer the input current I_{in} which allows the current comparator's inversion current. Transistors M1, M2, M4, and M5 buffer the reference current I_{ref} and provide the gain (of 2) required for scaling the weight of each bit in the digital output. The current comparator, formed by transistors M28, M29, M35, M36, and M30, M31, M32, M33 are simply digital inverters: if I_{ref} is larger than $2I_{in}$, Vc1 and Vc2 tends to increase towards the positive supply, the comparator's output goes low, and the differences current Iref - Iin is steered through M12, M13 to the next cell. Otherwise, Vc1 and Vc2 is low, the comparator's output is high, and the differences current is steered through M12 and the output mirror (composed from transistors M24, M25, M26, M27, M34 and M37) to the next cell. Since the source terminals for both M10, M11, M12, M13, M14, M15, and M16 are

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at Vc1 and Vc2, and their gates are tied together, only one of the two transistors may be on at any given time, preventing the output mirror's input from being tied to its output.

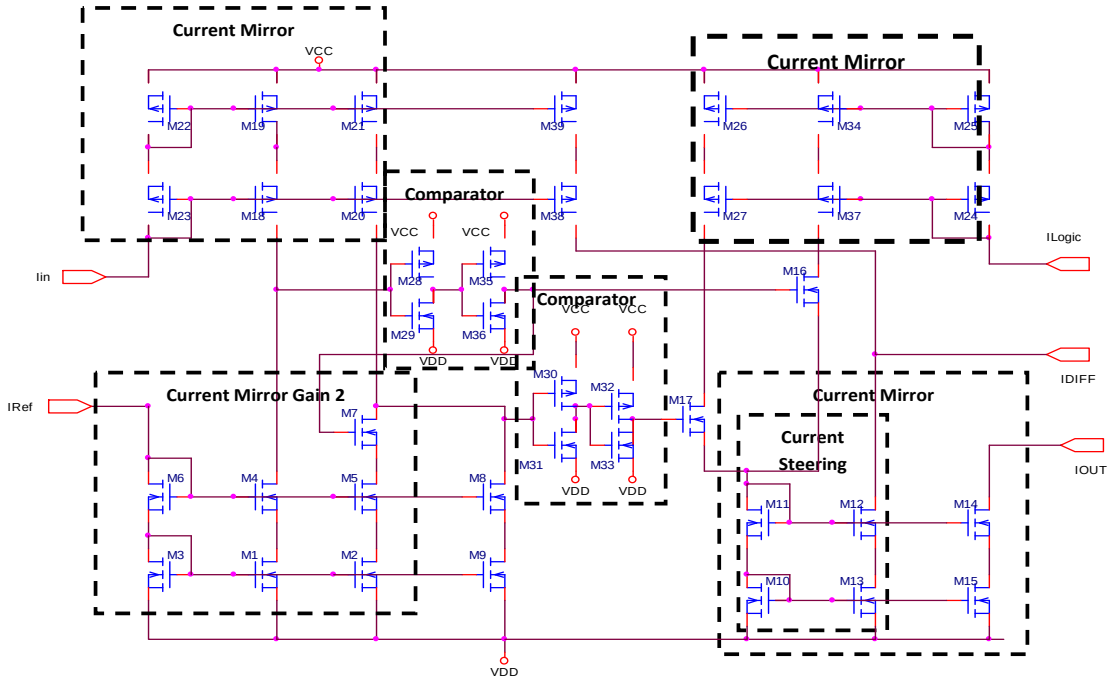

Fig. 1: Comparator Cell Schematic Diagram with different Block.

The working principle of the comparator cell can be explained as follows; the analog input current, Iin is compared with twice the reference current I_{Ref}, this determines if the I_{in} is within the upper or lower half of the full conversion current range. The comparator used here is a cascode current mirror comparator. The result of the comparison controls a MOS switch thus allowing or disallowing the flow to the output of a current two times the logic level current, I_{Logic}. This means that if the input current, I_{in}, is greater than half the full scale current range (which is equivalent to two times I_{Ref}), the current value which is two times the logic current level will be allowed to flow to the output. This operation generates two discrete current output levels with respect to the analog input current, I_{in}. In order to obtain the remaining two higher output levels, the difference of between $2*I_{Ref}$ and Iin is compared with I_{Ref} to decide on the more precise level in which the input current can be judged to be within the upper half or lower half of the full scale current range. If I_{in} is less than $2*I_{Ref}$, the subtraction will not be needed and Iin is simply compared with I_{Ref}. However if Iin is greater than $2*I_{Ref}$, then the difference of Iin – $2*I_{Ref}$ will be compared with I_{Ref} instead. A MOS switch is turned on/off in the cases of which one of the two options on subtraction is ultimately necessary. The result of this comparison will also control a MOS switch that allows or disallows the flow of the logic current level, ILogic to the output. Hence an output current of four possible discrete levels is obtained by adding the resulting current that has been allowed/disallowed based on the outcome of the preceding two comparisons for use in the succeeding stage in the cell series. This output current defines which quarter of the full scale current range that the analog input current Iin falls in. Note that the value of IRef is the same as I_{Logic}. In the circuit in Fig. 1, inverters have been used to strengthen the signals obtained from the two comparison stages before it is passed on to the MOS switch. In order to obtain the I_{Diff} output of the comparison block, both the input current, Iin and output current I_{Out} are mirrored and subtracted from each other. Due to the differencing technique employed in determining the output levels for a comparator cell, there is a prospect in extending the design of the comparator block for generating higher discrete output current levels.

The below mentioned operation of the comparator can be expressed in terms of flow as shown in Fig. 2.

RESULT AND DISCUSSION

The simulation is done using PSPICE BSIM3 NMOS model V3.2 for 0.13µm CMOS technology.

The reference current is chosen 2µA and triangular input current is applied to the current. The response of the comparator cell is shown in Fig. 3. A propagation error is found in Fig. 3.

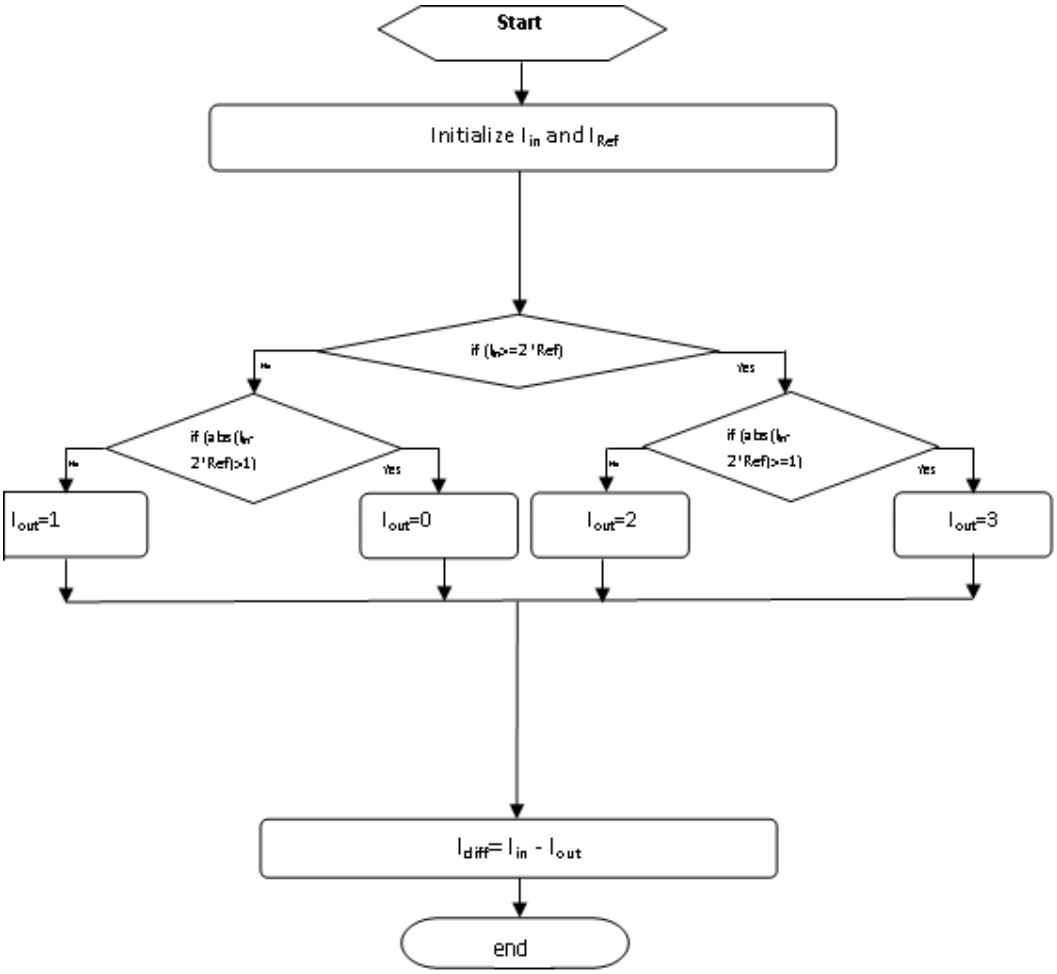

Fig. 2: Flow Diagram of Comparator Operation.

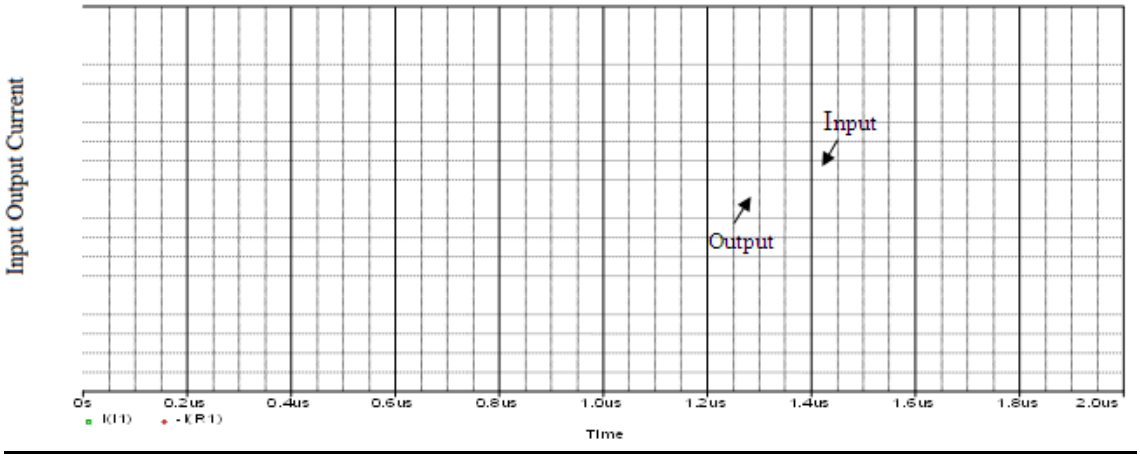

Fig. 3: Comparator Functionality Test.

The comparator is used to design a multi-valued quaternary Analog to Digital Converter (ADC) and block diagram is shown in Fig. 4.

Fig. 5 shows the digital current output resulting from a full-scale analog input current that is varying from 0 to 4μA for conversion stage realizing a four level digitized output. For a design with an output of three quaternary digits within the range of 0 to 4μA, there are 41 (4) possible output states with a code width of

4000nA between each interval while a design with quaternary digit will have 41 (4) possible output state. The sampling frequency of the comparator is 500 kHz at a power supply voltage of 1.3V and the measured average

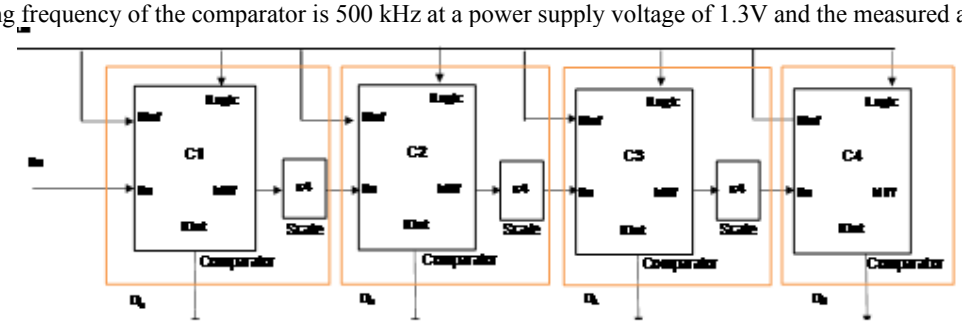

Fig. 4: Block Diagram of ADC Architecture.

power dissipated is also 0.107mW for the conversion. This is considered to be quite low and satisfactory compared to other MVL comparator designs. Table 1 shows a performance comparison for the proposed comparator design. Table 2 shows the comparison with the other research works.

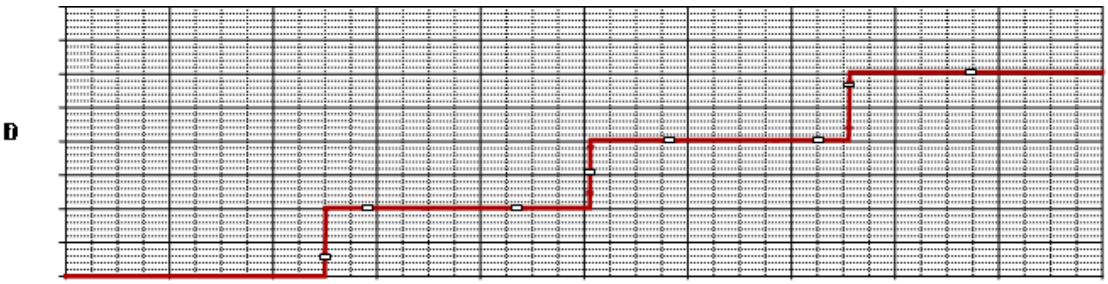

Fig. 5: Full scale quaternary digitize output.

Table 1: Summarized performances of the MVL Comparator.

Technology	0.13µm
Resolution	1-digit 4 level
Logic Level (I_{logic})	1uA
Code Width	4000 nA
Rise Time	0.583 uS
Sampling Rate	500 kHz
Power Consumption	0.107 mW
Power Supply	1.3 V

Table 2: Comparison between Other Works.

	(Current, 2008) (MVL)	(Temel, 2006) (MVL)	This research (MVL)
Technology	3-µm	90-nm	0.13-µm
Resolution	6-bit	9.4-bit	4-bit
Sampling Rate	500kHz	5MHz	500 kHz
Supply Voltage	5V	1.2-V	1.3-V
Power	4.65mW	1.44mW	0.107mW

Conclusion:

In this paper, a design has presented for current-mode circuits of comparator. The proposed MVL comparator is designed based on BSIM model V3.2 0.13µm CMOS process. A comparator cell is constructed using this current mirror technique. The design implements multiple valued logic output instead of the conventional binary output. The use of multiple-valued logic outputs for comparator design offers the possibility of an overall reduction in circuit complexity and size. A performance analysis test on the design using the model parameters for a 0.13µm standard CMOS process shows the design obtaining desirable parameters in terms of rise time, speed, power consumption and extensibility of design. The circuit parameters such as length and width are optimized for better response and performance. It is then found that the length of the comparator circuit is found as 0.25µm although the process length is 0.13µm. The circuit is supplied by 1.3 V which consume 0.107mW power. The designed circuit digital output consists of 0 to 3 levels in one digit with radix-4 without any error propagation. Comparator forms an important interface between analog and digital domain. Digital

wireless communication applications such as ultrawideband (UWB) and wireless personal area network (WPAN) need low-power high-speed MVL comparator using in ADC to convert RF/IF signals into digital form for baseband processing.

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